AN-1332
APPLICATION NOTE

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Architecting a Direct, 3-Phase Energy Meter with Shunts Using the ADE7912/ADE7913

by Petre Minciunescu and Dave Smith

INTRODUCTION

The ADE7912/ADE7913 3-channel, isolated, Σ-Δ analog-to-digital converters (ADCs) target polyphase energy metering applications using shunt current sensors. This application note expands the Applications Information section of the ADE7912/ADE7913 data sheet. It provides in depth explanations on how to use the ADE7912/ADE7913 when developing a direct, 3-phase meter with shunts.

ARCHITECTING A DIRECT 3-PHASE METER USING THE ADE7912/ADE7913

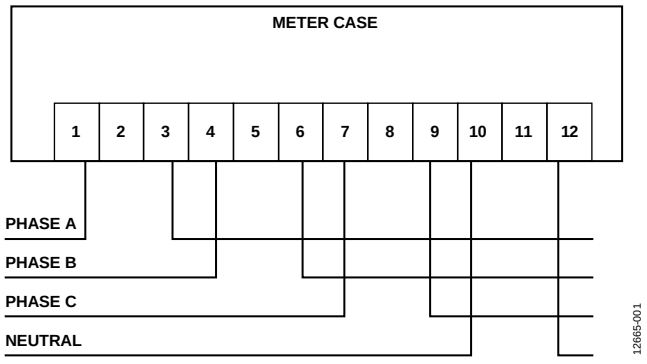

Figure 1. Three-Phase, 4-Wire Direct Meter Connections

Figure 1 shows how a direct, 3-phase energy meter is connected in a 3-phase, 4-wire system. The Phase A line connects to Terminal 1 and Terminal 3 of the meter, Phase B connects to Terminal 4 and Terminal 7, Phase C connects to Terminal 7 and Terminal 9, and the neutral line connects to Terminal 10 and Terminal 12. Typically, Terminal 2, Terminal 5, and Terminal 8 of the meter are used for the voltage sensing connections. In the case of the direct, 3-phase energy meter, they are internally connected to Terminal 1, Terminal 4, and Terminal 7, respectively. These are the points of the meter where the lines of Phase A, Phase B, and Phase C enter the meter.

Figure 2 shows the architecture of a meter using the ADE7912/ADE7913. Three shunts connect to the meter terminals where the 3-phase, 4-wire connections are made. Each ADE7912/ADE7913 manages one phase through an interface circuitry. The reference terminal of the shunt becomes the ground of the isolated side of the ADE7912/ADE7913. GND_A is the ground of the Phase A ADE7912/ADE7913 isolated side, GND_B is the ground of the Phase B ADE7912/ADE7913 isolated side, and GND_C is the ground of the Phase C ADE7912/ADE7913 isolated side. The resistor dividers, R1_x and R2_x, sense the voltage between the Phase A, Phase B, and Phase C lines and the neutral line. The current channel ADC of each ADE7912/ADE7913 measures the voltages across the shunts, while the V1 voltage channel ADC measures the voltages across the R1_A, R1_B, and R1_C resistors.

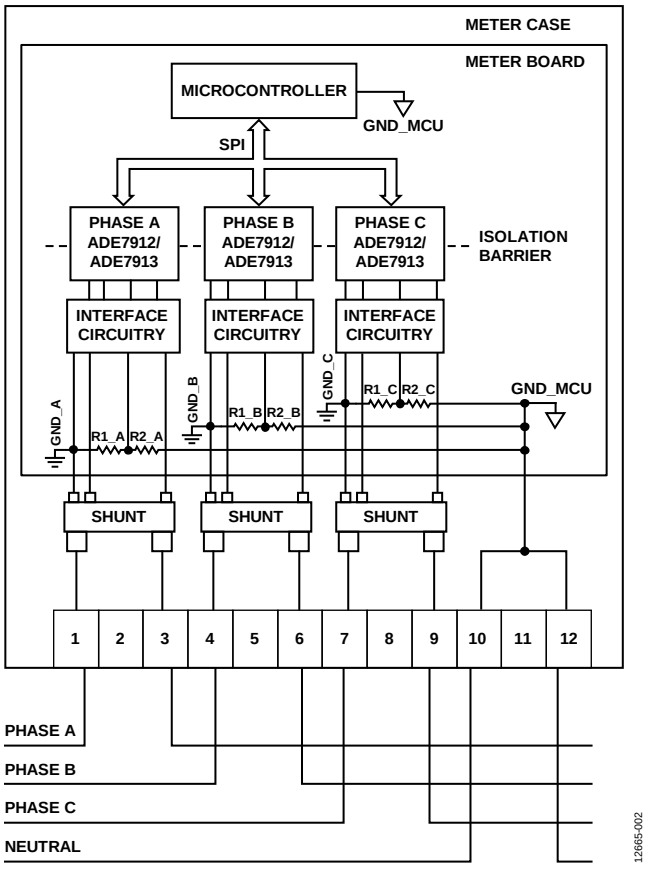

Figure 2. Shunt-Based, Direct, 3-Phase Meter Architecture

Note that when the meter is based on the ADE7912/ADE7913, Terminal 2, Terminal 5, and Terminal 8 of the meter are not used. The reference terminals of the shunts (GND_A, GND_B, and GND_C), being directly connected to the phase lines, become the reference points for the voltage sensing resistor dividers.

There is some interface circuitry between the shunts, the voltage dividers, and the ADE7912/ADE7913 devices that is discussed in the Interfacing the ADE7912/ADE7913 with the Shunt and the Resistor Divider section.

The neutral line determines the ground of the microcontroller (GND_MCU) that manages the ADE7912/ADE7913 devices. This is the same ground of the primary side of the ADE7912/ADE7913. The microcontroller uses one serial port interface (SPI) to communicate with the ADE7912/ADE7913s. This means that the power supply of the meter must provide a supply voltage to the microcontroller and the ADE7912/ADE7913s that has the GND_MCU ground on the neutral line.

The neutral line current is not monitored in the meter presented in Figure 2. Figure 3 presents the architecture of a direct, 3-phase meter in which the neutral current is monitored. The only difference is an additional ADE7912 (Phase N) that senses only the neutral line current using a shunt. The voltage channel of this chip is not used.

The microcontroller and the primary side of the ADE7912/ADE7913s have a GND_MCU isolated ground from the neutral line. This means the power supply of the meter must provide a supply voltage to the microcontroller and the ADE7912/ADE7913s that is isolated from the neutral line.

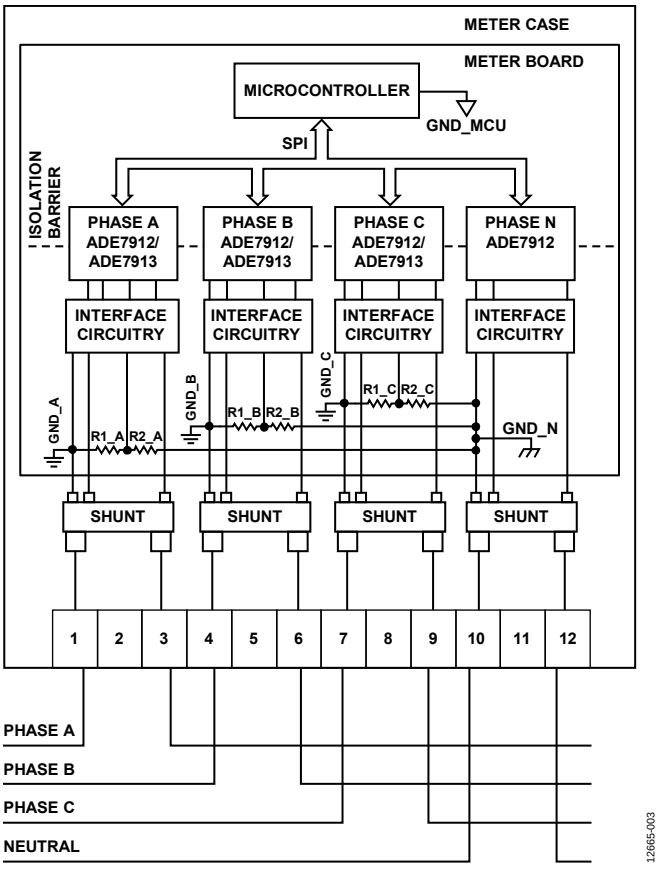

Figure 3. Shunt-Based, 3-Phase Meter Architecture with Monitored Neutral Line

INTERFACING THE ADE7912/ADE7913 WITH THE SHUNT AND THE RESISTOR DIVIDER

All the ADE7912/ADE7913s that monitor the phase lines have the same interface circuitry. This circuitry is composed of two paths: one that interfaces the ADE7912/ADE7913 with the shunt (see Figure 4), and one that interfaces the ADE7912/ADE7913 with the voltage divider (see Figure 5).

The Phase A, B, C, or N current is sensed with a shunt (see Figure 4). The antialiasing filters, R/C (1 kΩ/33 nF), between the IP and IM pins and the shunt terminals have a corner at 4.8 kHz ($1/(2 \times \pi \times 10^3 \times 33 \times 10^{-9})$). The AGND_ADC ground point where the filter capacitors are biased is connected to the reference terminal GND_A, GND_B, GND_C, or GND_N of the shunts.

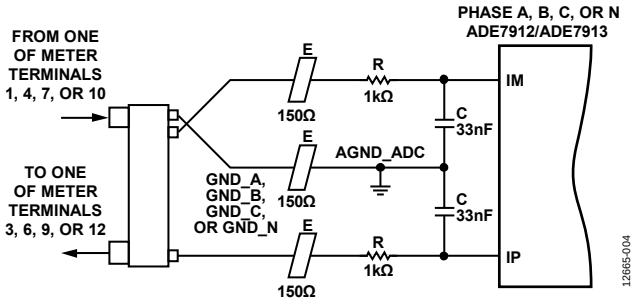

Figure 4. Interfacing the ADE7912/ADE7913 with a Shunt

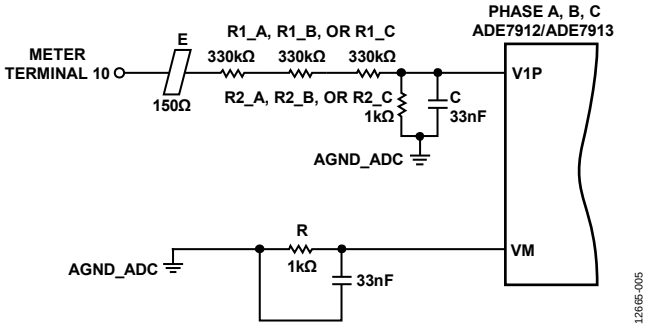

Figure 5. Interfacing the Phase A ADE7912/ADE7913 with a Voltage Divider

The Phase A, B, or C to neutral voltages are sensed with the voltage dividers R1_x and R2_x. The resistor R1_x is composed of three 330 kΩ resistors, and R2_x is equal to 1 kΩ. This ensures a full scale voltage equal to the following equation, which is sufficient to monitor 230 V, 3-phase systems:

$$\frac{0.5}{\sqrt{2}} \times \frac{3 \times 330\ K + 1\ K}{1K} = 350.37\ \text{V}$$

Capacitor C (33 nF), in parallel with R2_x, creates the antialiasing filter in the V1P pin path. Between the AGND_ADC ground point derived from the ground terminal GND_x of the shunt (see Figure 4) and the VM pin of the ADE7912/ADE7913, there is an identical antialiasing filter, R/C (1 kΩ/33 nF). Note that the antialiasing filters in both current and voltage paths are the same. This ensures that the delays introduced in the phase current and voltage measurements are similar.

The E ferrite beads (150 Ω at 100 MHz) are placed in the shunt and voltage divider connections to filter the high frequency noise that may be induced into the wires during electrical fast transient (EFT) tests.

As the meter architectures considered in Figure 2 and Figure 3 do not present any additional voltages to measure besides the phase to neutral voltages, Figure 5 does not present the circuitry required to interface the V2P pin of the ADE7913. However, if additional voltages are monitored, the V2P circuitry is identical to the V1P circuitry. The V2P functionality is available only on the ADE7913. The V2P functionality is not available on the ADE7912.

PROVIDING CLOCK SIGNAL TO ADE7912/ADE7913

The ADE7912/ADE7913 data sheet provides extensive detail on ways to provide the clock to the ADE7912/ADE7913 devices of a 3-phase energy meter.

If the microcontroller is able to generate a clock signal with a frequency between 3.6 MHz and 4.21 MHz over the −40°C to +85 °C temperature range, then clock all the ADE7912/ADE7913s of the meter from it. If the microcontroller cannot generate the clock, then clock one ADE7912/ADE7913 device from a crystal and use it to provide clock to the other ADE7912/ADE7913s of the energy meter. Use the power-up procedure detailed in the data sheet to accomplish this.

Both clocking schemes ensure all isolated ADCs function synchronously: they sample signals simultaneously and provide coherent ADC output samples. See the ADE7912/ADE7913 data sheet for details.

COMMUNICATING WITH THE ADE7912/ADE7913

The ADE7912/ADE7913 has an SPI interface, and the corresponding data sheet provides extensive details on the protocol used to read and write the device registers.

In this section, a system perspective of the microcontroller managing three or four ADE7912/ADE7913s in a 3-phase energy meter is proposed.

Suppose that the microcontroller is connected to the ADE7912/ADE7913s as shown in Figure 6 or Figure 7. The SPI port of each ADE7912/ADE7913 is selected using three (see Figure 6) or four (see Figure 7) input/output (I/O) lines of the microcontroller: CS_A, CS_B, CS_C, and CS_N. The CLKOUT/$\overline{\text{DREADY}}$ pin of Phase C of the ADE7912/ADE7913 is connected to an I/O pin of the microcontroller on which the microcontroller can receive an external interrupt.

The microcontroller communicates with the ADE7912/ADE7913s at the maximum allowed SPI serial clock frequency of 5.6 MHz.

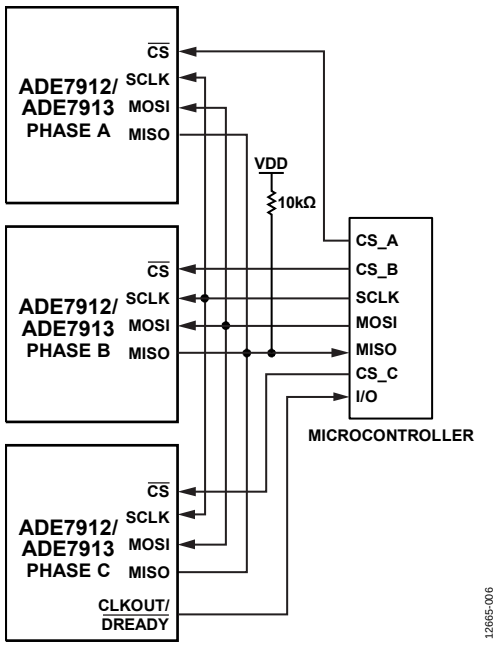

Figure 6. Connections Between Three ADE7912/ADE7913s and the Microcontroller

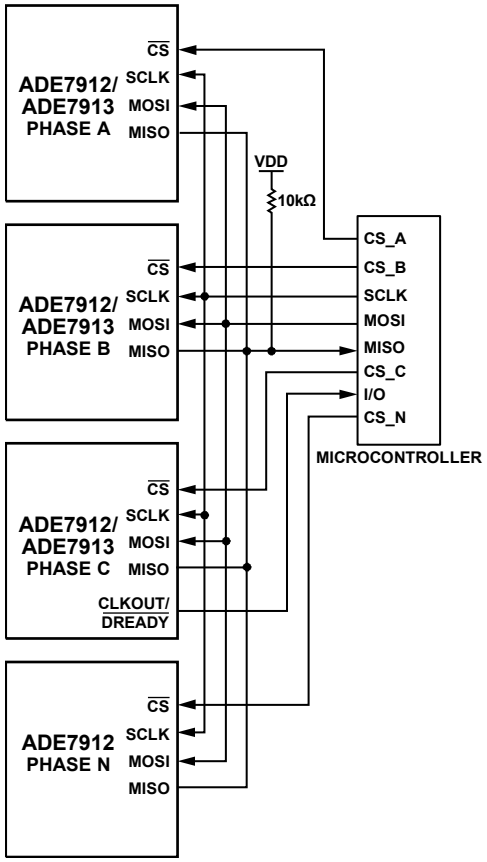

Figure 7. Connections Between Four ADE7912/ADE7913s and the Microcontroller

The ADE7912/ADE7913s are set to provide the ADC outputs at 8 kHz, that is, a 125 µs period. Set Bits[5:4] (ADC_FREQ) in the CONFIG register (Register 0x8) to 00 on all ADE7912/ADE7913s.

All the ADE7912/ADE7913s function synchronously, that is, the ADCs sample simultaneously on all three phases and the ADC outputs are coherent.

$\overline{\text{DREADY}}$ functionality is selected at Phase C on the ADE7912/ADE7913 CLKOUT/$\overline{\text{DREADY}}$ pin: Bit 0 (CLKOUT_EN) in the CONFIG register cleared to 0. Every 8 kHz, the CLKOUT/$\overline{\text{DREADY}}$ pin goes low for 64 CLKIN cycles (15.625 µs at CLKIN = 4.096 MHz).

Figure 8 presents the result of the microcontroller receiving an external interrupt because the CLKOUT/$\overline{\text{DREADY}}$ pin of the ADE7912/ADE7913 managing Phase C has a high to low transition.

The microcontroller executes a burst read of the ADE7912/ADE7913 output registers: IWV, V1WV, V2WV (if ADE7913 is used), ADC_CRC, STATUS0, and CNT_SNAPSHOT. Reading ADC_CRC, STATUS0, and CNT_SNAPSHOT is not obligatory, but they are included in the calculation as the worst-case scenario.

The time to read these registers from three ADE7912/ADE7913s (see the case shown in Figure 6) is

$$3 \times \frac{8 + 3 \times 24 + 16 + 8 + 16}{5.6 \times 10^6} \cong 65\ \mu s$$

In reality, this timing is usually longer because the microcontroller management of the SPI communication includes some C programming inefficiency, but there are 125 – 65 = 60 µs left to accommodate them every ADC output period.

Figure 3 presents the case of an energy meter containing four ADE7912/ADE7913s. Considering that the ADE7912 managing Phase N senses only the neutral line current, the time to read these registers from all ADE7912/ADE7913s is

$$4 \times \frac{8 + 3 \times 24 + 16 + 8 + 16}{5.6 \times 10^6} \cong 86\ \mu s$$

The timing is well within the 125 µs allotted time. In this case, 125 – 86 = 39 µs are available to accommodate eventual C programming inefficiencies.

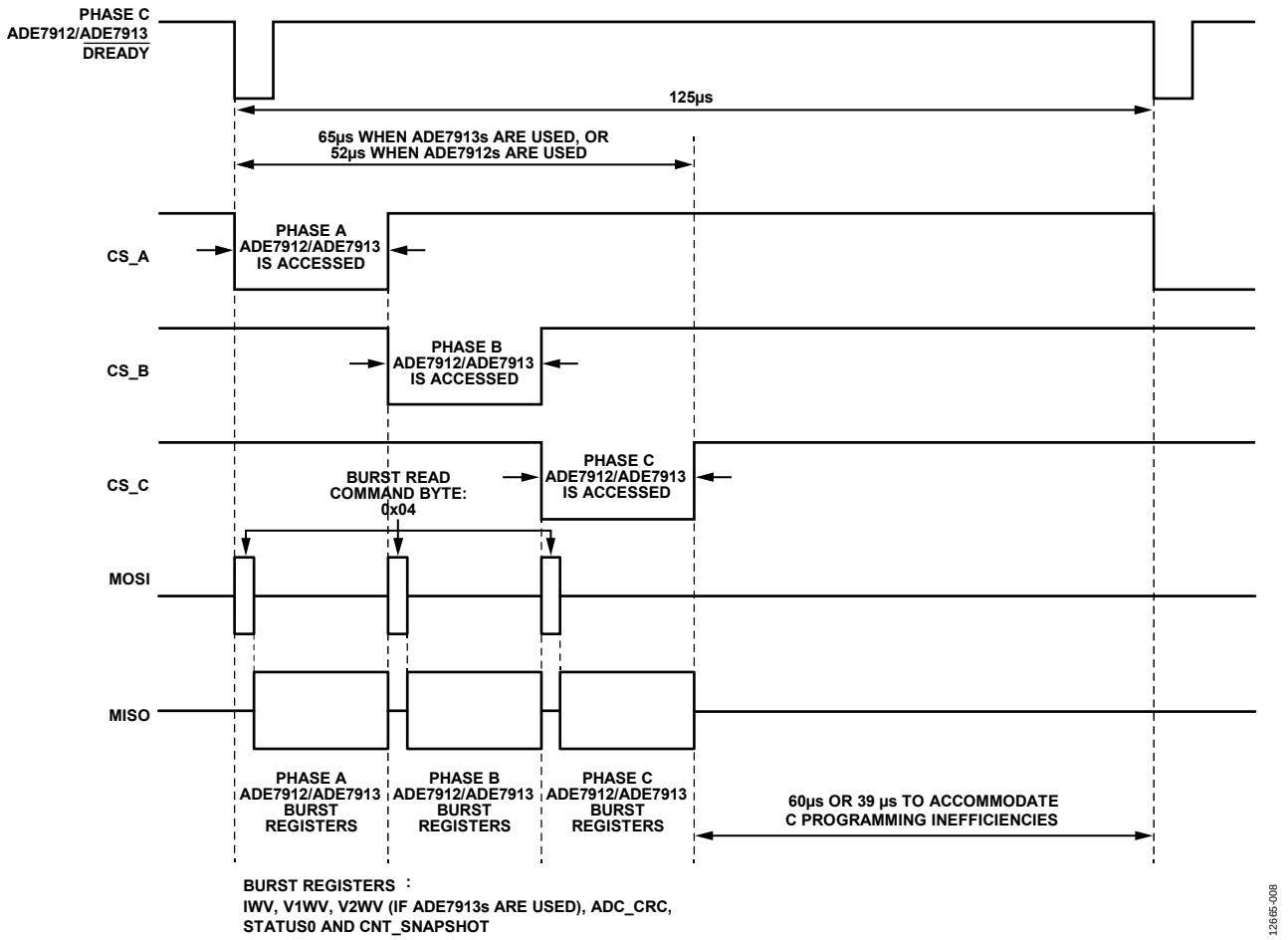

Figure 8. System Perspective of Communication Between the Microcontroller and ADE7912/ADE7913s in an Energy Meter

ENERGY METERING SOFTWARE PROGRAM REMARKS

This section contains observations related to the ADE7912/ADE7913. It is recommended that the energy metering program residing in the microcontroller take these observations into account.

Use the power-up and initialization procedure outlined in the ADE7912/ADE7913 data sheet to ensure all ADE7912/ADE7913s the board start correctly and function synchronously.

The ADE7912/ADE7913 specifications table of the data sheet states that the current channel ADC offset error is typically −2 mV and the voltage channels ADC offset error is typically −35 mV. The ADC offset drift over temperature is ±500 ppm/°C, maximum. The ac energy metering calculations need to eliminate this offset. Because the offset drifts with temperature, implement a high-pass filter (HPF) to eliminate it. A simple offset calibration at room temperature is not recommended as it does not fully compensate the temperature influence.

Independent of how the shunts are mounted on the printed circuit board (PCB), their electric circuits introduce a phase error in the metrology calculations. Therefore, it is recommended to use a phase compensation procedure that aligns the currents and voltages on each phase.

LAYOUT GUIDELINES

Figure 10 presents the schematic of the metrology section of a direct, 3-phase meter using three ADE7913s, identical to the schematic of the ADE7913 evaluation board. The second voltage channel, V2, is shown with a voltage divider in order to provide the most comprehensive layout example possible.

A 4-layer PCB is required when using ADE7912/ADE7913. A 3-phase meter using three ADE7913s passes the Class B CISPR22 standard specification with a sufficient margin only when a 4-layer PCB is used (see the Radiated Emission Tests Results section for details on these results).

The top and bottom layers are identical to a 2-layer PCB design, and the inner layers create a stitching capacitor. The presence of the stitching capacitor is essential in order to reduce the emissions generated by the ADE7912/ADE7913 dc-to-dc converter, and to meet the standard requirements.

Figure 9 presents the structure of the 4-layer PCB. The top layer contains the components. The second layer creates one plate of the stitching capacitor using the GND_{ISO} isolated ground of the ADE7912/ADE7913s. The third layer creates the other plate of the stitching capacitor using the GND_MCU primary ground of the ADE7912/ADE7913s. Note that the PCB thickness between the plates is 0.5 mm. Because the standard IEC 62052-31 requires a minimum thickness of 0.4 mm when line to neutral voltages are below 300 V, a thickness of 0.5 mm is used to allow any PCB production variation.

It is not recommended to invert the second and third layers, that is, setting the GND_MCU plane on the second layer and the GND_{ISO} plates on the third layer, because the GND_MCU plane creates a parasitic capacitance with the shunt related PCB traces on the top layer. This parasitic capacitance creates a voltage that adds to the voltage across the shunt and is proportional and in phase with the voltage between the GND_{ISO} and GND_MCU. This also affects the accuracy of the metrology measurements. By setting the GND_{ISO} plates on the second layer and GND_MCU plane on the third, the GND_{ISO} plates shield the GND_MCU plane and remove the coupling to the shunt IP and IM PCB traces on the top layer.

Figure 11, Figure 12, Figure 13, and Figure 14 present the recommended 4-layer layout of the metrology section from Figure 10. It is the layout implemented in the ADE7913 evaluation board.

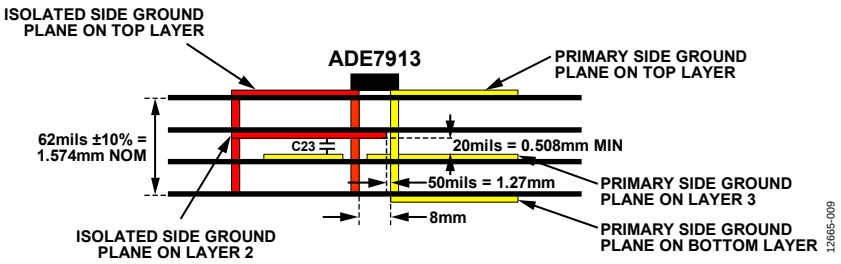

Figure 9. Four-Layer Structure with Stitching Capacitor

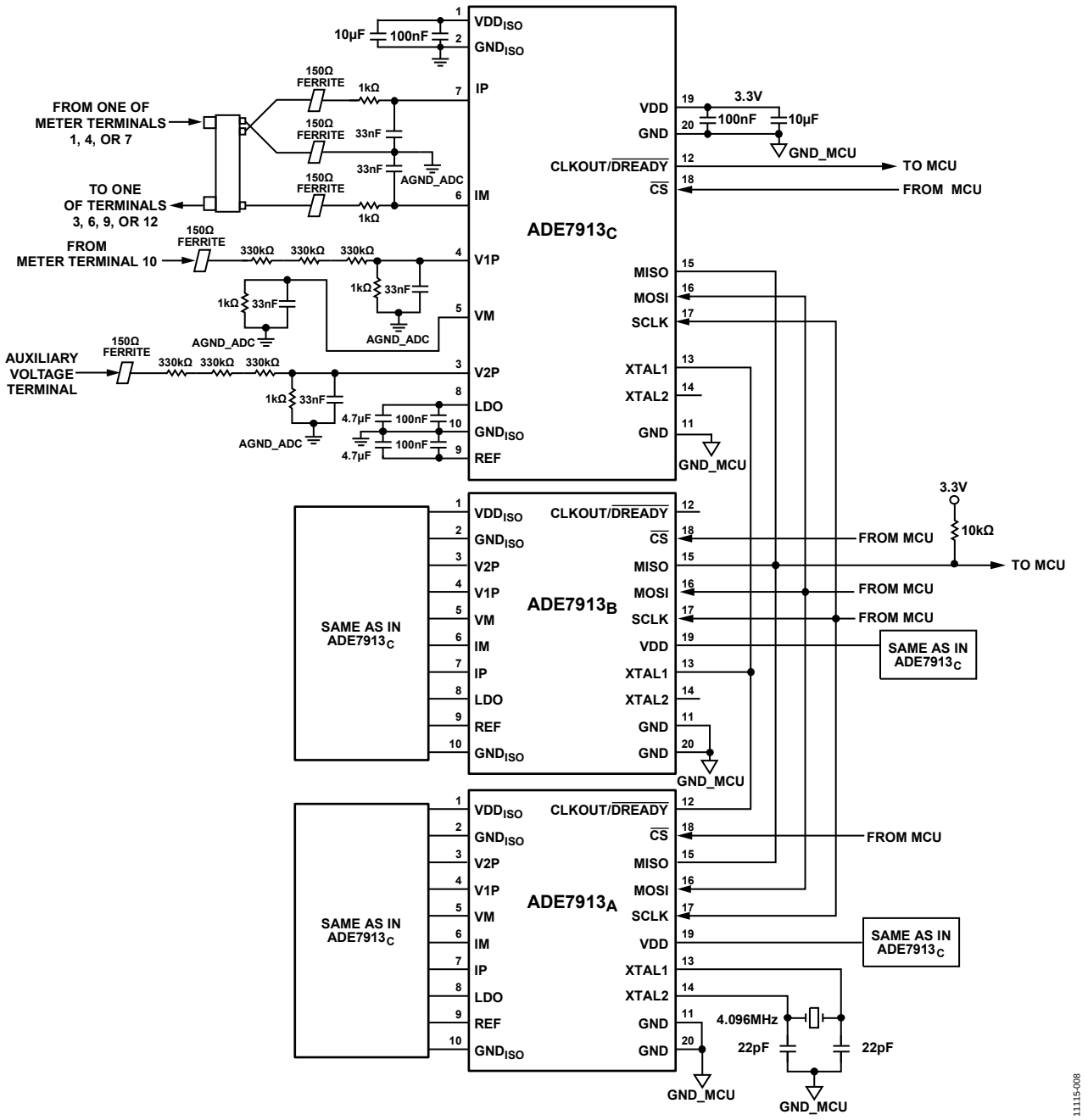

Figure 10. Direct, 3-Phase Meter Schematic of Metrology Section

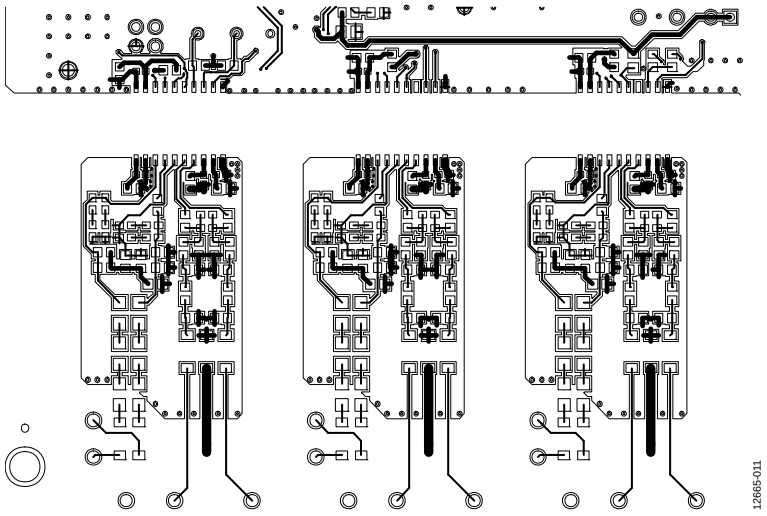

Figure 11. Top Layer Layout of the Direct, 3-Phase Meter Metrology Section

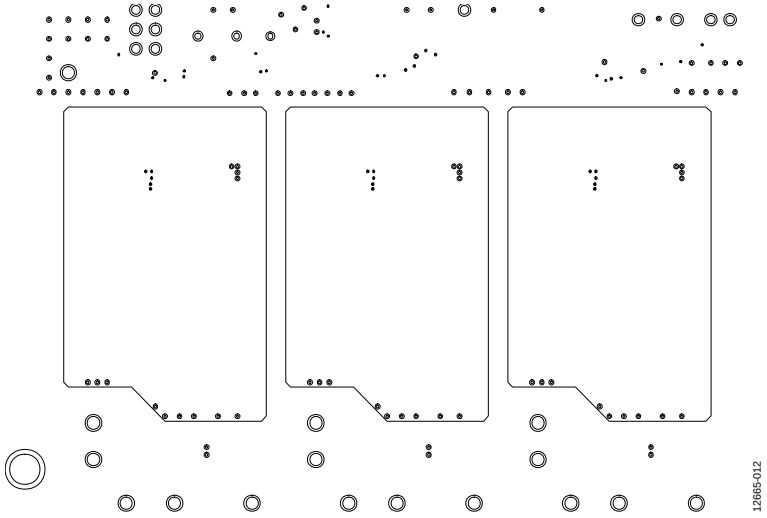

Figure 12. Layer 2 Layout of the Direct, 3-Phase Meter Metrology Section

Figure 13. Layer 3 Layout of the Direct, 3-Phase Meter Metrology Section

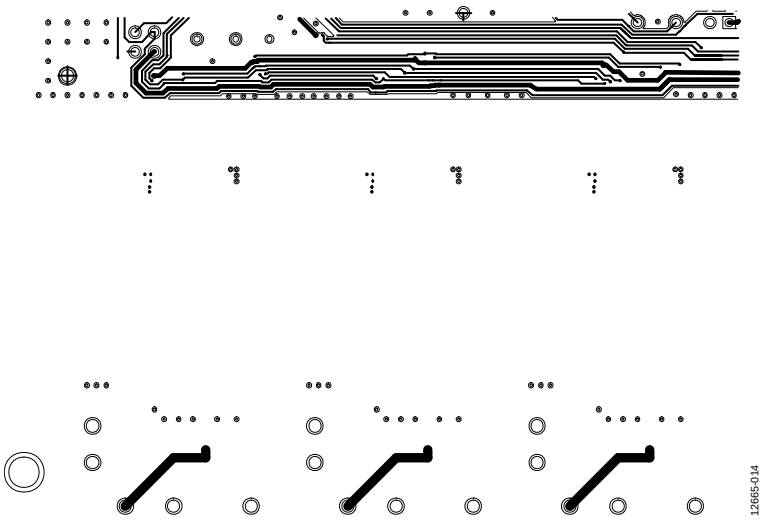

Figure 14. Bottom Layer Layout of the Direct, 3-Phase Meter Metrology Section

In the following sections, the various parts of the schematic are analyzed and commented upon, relative to their associated layout.

Decoupling Capacitors Layout Guidelines

Follow these recommendations for the decoupling capacitors between the VDD and GND (10 µF and 100 nF), VDD_{ISO} and GND_{ISO} (10 µF and 100 nF), LDO and GND_{ISO} (4.7 µF and 100 nF), and REF and GND_{ISO} (4.7 µF and 100 nF) pins of the ADE7912/ADE7913:

- Place the 100 nF capacitors closest to the chip.
- Make the connections between the capacitors and the VDD, VDDISO, LDO, and REF pins as short as possible.
- Make the connections between the capacitors and the GND, GND_{ISO}, LDO, and REF pins as short as possible.

This improves the electromagnetic compatibility (EMC) immunity of the chips and lowers the emissions generated by the ADE7912/ADE7913 dc-to-dc converter.

Figure 15, Figure 16, Figure 17, and Figure 18 present the various layouts of these capacitors.

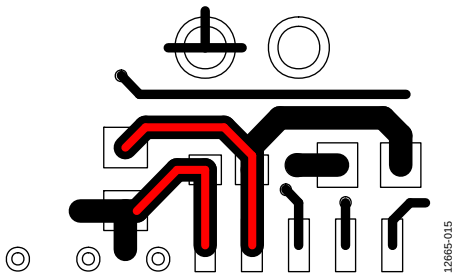

Figure 15. Layout of Capacitors Between the VDD and GND Pins

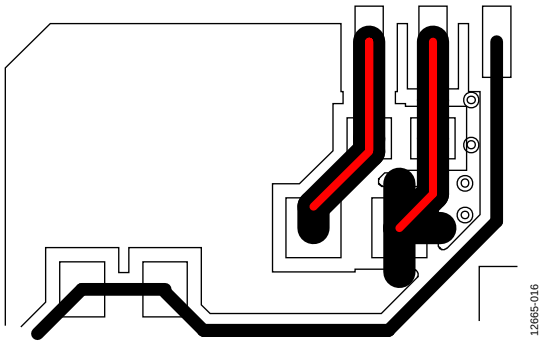

Figure 16. Layout of Capacitors Between the VDD_{ISO} and GND_{ISO} Pins

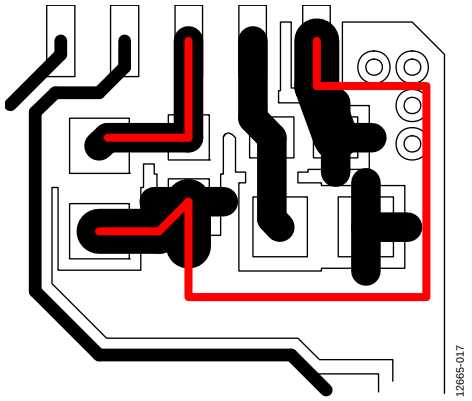

Figure 17. Layout of Capacitors Between the LDO and GND_{ISO} Pins

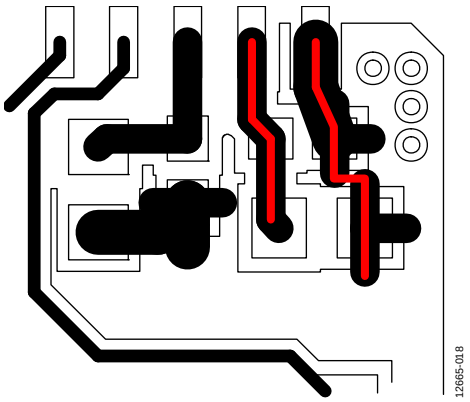

Figure 18. Layout of Capacitors Between the REF and GND$_{ISO}$ Pins

Crystal and Load Capacitors Layout Guidelines

The crystal load capacitors must be placed closest to the Phase A ADE7912/ADE7913 to improve the EMC immunity of the chip, whereas the crystal can be placed in close proximity (Figure 19). The distance between the crystal and the load capacitors is not as critical as the distance between the capacitors and the XTAL1 and XTAL2 pins.

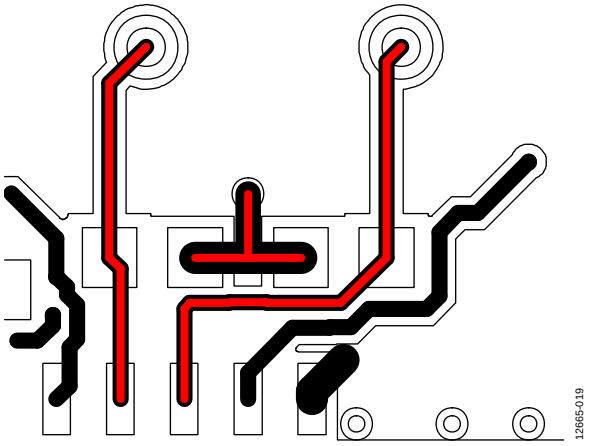

Figure 19. Layout of Crystal and Load Capacitors

Isolated Ground Layout Guidelines

The ADE7912/ADE7913 have two GND$_{ISO}$ isolated ground pins. They are connected through a ferrite bead to the reference terminal of the shunt and determine the isolated ground plane on the top layer of the PCB. The connections between the GND$_{ISO}$ pins and the isolated ground plane must be very short. The vias used to connect the isolated ground plane from the top layer to the stitching capacitor plate on the second layer need to be close to the GND$_{ISO}$ pins in order to have the lowest inductance possible. Limit the number of vias to the minimum as they take area from the stitching capacitor plates and reduce its capacitance.

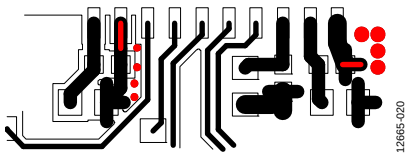

Figure 20. Layout of the GND$_{ISO}$ Connections to the Isolated Ground Plane and Related Vias

The stitching capacitor is created by plates on the second and third PCB layers. Figure 21 shows the layout of one plate created underneath the Phase A ADE7912/ADE7913. The vias within the red circles connect this plate to the GND$_{ISO}$ plane from the top layer. Figure 22 shows the layout of the GND_MCU plane in the third layer. It creates the plate of three stitching capacitors, one for each ADE7912/ADE7913. The vias within the red circles are the GND$_{ISO}$ vias. There is more than 1 mm of space between these vias and the GND_MCU plate in order to comply with the IEC 62052-31 standard that requires a 0.4 mm minimum distance between adjacent conductors when the line to neutral voltages are below 300 V.

The minimum stitching capacitor area recommended to pass Class B CISPR22/EN-55022 standard specification is 825 mm^2, giving a capacitor value of 63 pF (see the Radiated Emission Tests Results section for more details). The expression used to compute this 63 pF capacitor value is:

$$C = \varepsilon_0 \times \varepsilon_r \times \frac{A}{d}$$

where:
ε_0 = 8.854 × 10^{-12} F/m and is the vacuum permittivity.
ε_r = 4.3 and is the relative permittivity of the PCB FR4 material.
A = 825 mm^2 and is the area of the capacitor plates.
d = 0.5 mm and is the distance between the plates.

The larger the area of the plates, the larger the capacitor value, the greater the margin in passing the Class B CISPR22/EN-55022 standard. In the ADE7913 evaluation board, a distance of 2.54 mm is designed between the GND$_{ISO}$ plates of various ADE7913s on Layer 2, although the IEC 62052-31 standard requires a 0.4 mm minimum distance between adjacent conductors when the line to neutral voltages are below 300 V (see Figure 23). The capacitor value is 84 pF for an area of the plates equal to 1100 mm^2.

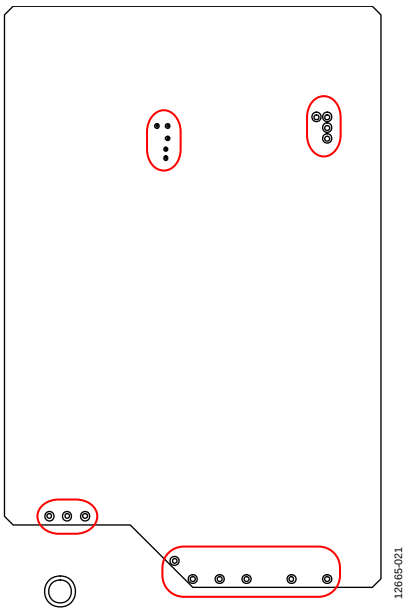

Figure 21. Section of PCB Layer 2 Creating Stitching Capacitor GND$_{ISO}$ Plate

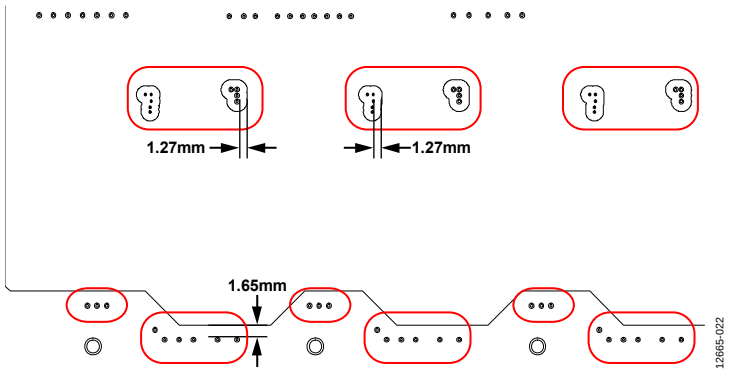

Figure 22. Section of Layer 3 Creating Stitching Capacitor GND_{MCU} Plate

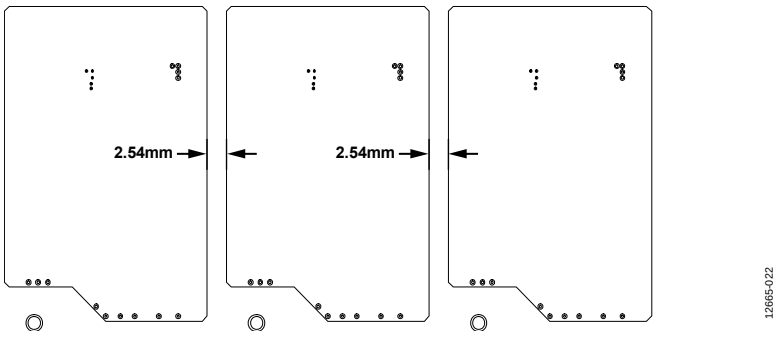

Figure 23. Section of Layer 2 Showing All Three Stitching Capacitors

RADIATED EMISSION TESTS RESULTS

We tested the ADE7913 evaluation board for compliance with the Class B CISPR22 standard. The board has been placed in a three phase meter case and was powered from a battery. A 5 m, 3-phase cable without termination was mounted on the meter and then placed under the floor in the anechoic chamber (Figure 24).

Measurements of the radiated emissions were executed for frequencies between 30 MHz and 1 GHz and between 1 GHz and 2 GHz.

With a stitching capacitor of 84 pF (1100 mm^2 plates), a minimum 10 dBµV/m quasi peak margin to Class B CISPR22 limits was obtained for frequencies between 30 MHz and 1 GHz (Figure 25). For frequencies between 1 GHz and 2 GHz, a minimum 11 dBµV/m average results margin to Class B CISPR22 limits was obtained (Figure 26).

To test the radiated emissions when the stitching capacitor is smaller, we built an ADE7978 evaluation board with a stitching capacitor of 63 pF (825 mm^2). As an ADE7933 isolated ADC used on this board is equivalent to an ADE7913 from emissions perspective, we may say the ADE7978 evaluation board behaves in the same way as an equivalent ADE7912/ADE7913 based design. This board passed Class B CISPR22 specification by a 9 dBµV/m quasi peak margin for frequencies between 30 MHz and 1 GHz (Figure 26) and 7 dBµV/m average results margin for frequencies between 1 GHz and 2 GHz (Figure 28).

As already stated, we do not recommend PCB designs that have stitching capacitors smaller than 63 pF (that is with the area of the plates smaller than 825 mm^2). For example, with a stitching capacitor of 42 pF (that is an area of the plates of 550 mm^2), an ADE7978 evaluation board was over the Class B CISPR22 limit by 4 dBµV/m at 380 MHz.

Figure 24. Three-Phase Meter with Battery in the Anechoic Chamber

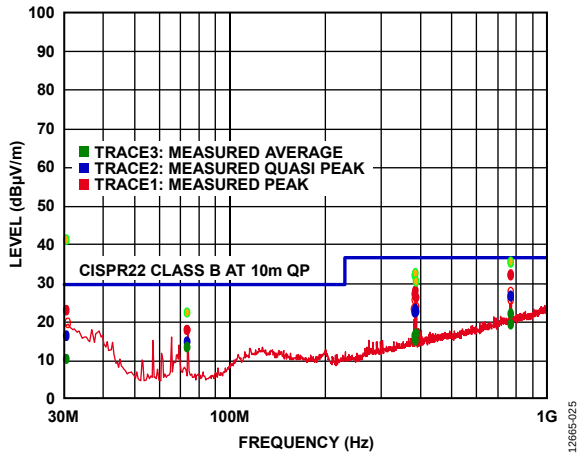

Figure 25. Anechoic Chamber Emissions from the ADE7913 Evaluation Board, 84 pF Stitching Capacitor (Quasi Peak Points are in Blue, 30 MHz to 1 GHz)

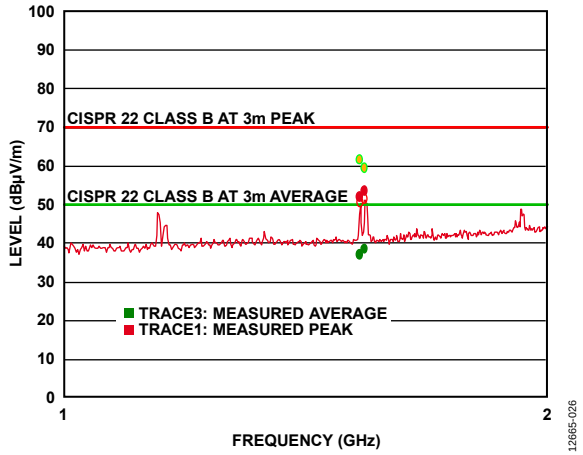

Figure 26. Anechoic Chamber Emissions from the ADE7913 Evaluation Board, 84 pF Stitching Capacitor (Average Points are in Green, 1 GHz to 2 GHz)

CONCLUSION

This application note has shown how to develop a direct three phase meter with shunts using the ADE7912/ADE7913 isolated ADC. It provided recommendations on the schematic and layout in order to pass the Class B CISPR22 radiated emissions specification by at least 10 dBµV/m margin. It showed how much bandwidth a microcontroller has to reserve to managing the SPI communication with up to four ADE7912/ADE7913s.

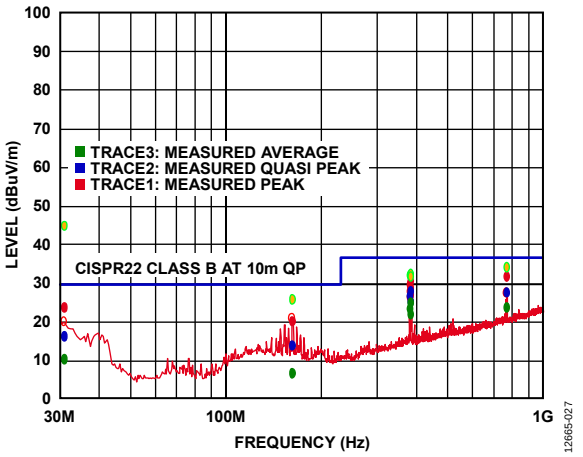

Figure 27. Anechoic Chamber Emissions from ADE7978 Evaluation Board, 63 pF Stitching Capacitor (Quasi Peak Points are in Blue, 30 MHz to 1 GHz)

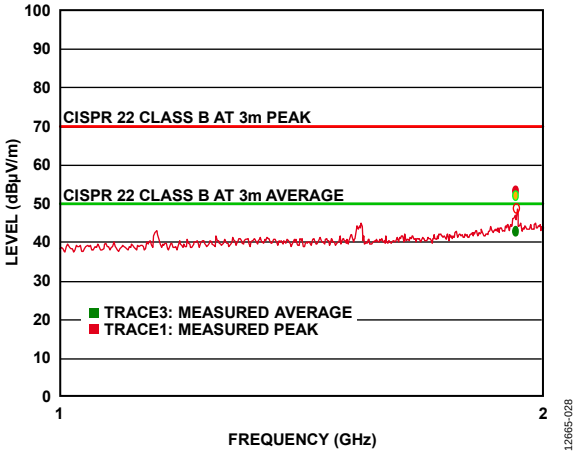

Figure 28. Anechoic Chamber Emissions from ADE7978 Evaluation Board, 63 pF Stitching Capacitor (Average Points are in Green, 1 GHz to 2 GHz)

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).