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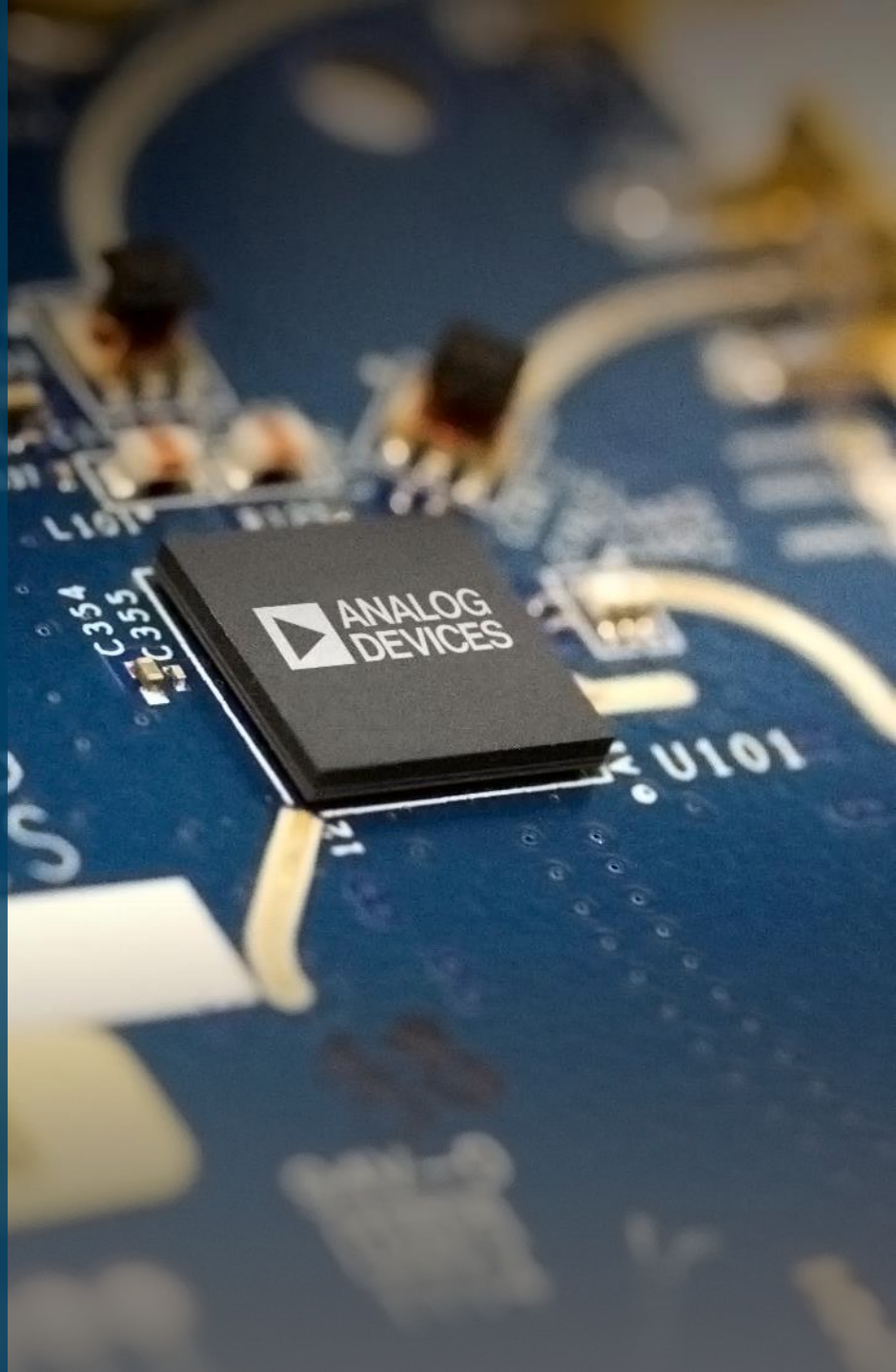
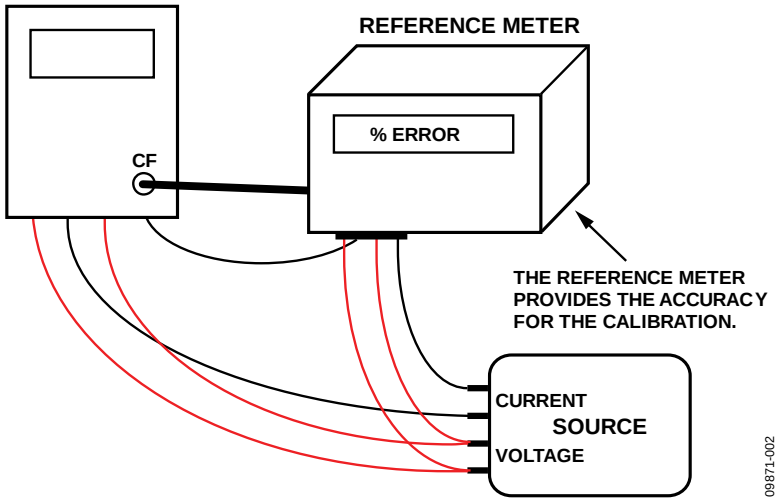
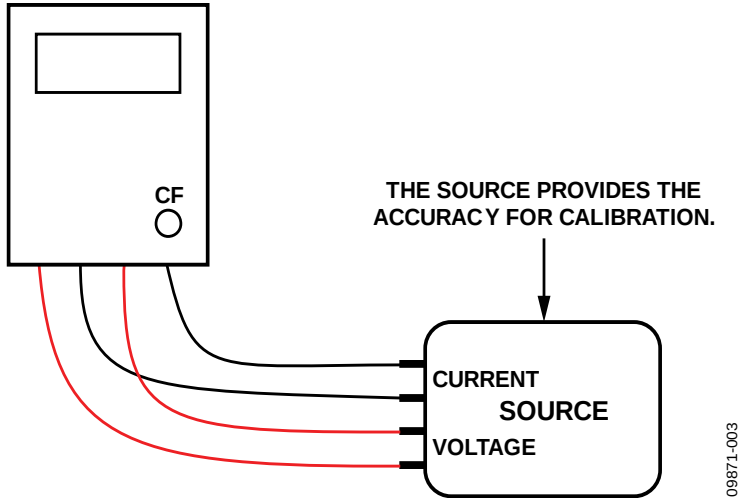
# ADE9078 QUICK START & GUIDE for CALIBRATION TOOL



# Typical Calibration Setups

- **Reference meter**
  - Suitable for calibration using CF outputs
- **Accurate Source**
  - Suitable for calibration using internal registers

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# Calibration Techniques

- **CF outputs**
  - Error output from reference meter using CF readings
  - Impulse/kWHr output from reference meter using CF readings
- **Reading internal energy registers**
- **Download ADE9078 calibration tool: http://www.analog.com/media/en/engineering-tools/design-tools/ADE9078-Calibration-Tool.zip**

# Calibration Flow using CF outputs

- **Setup initialization registers.**
  - Set PGA Gain, HPF_CRN, INTEN (&DICOEFF=0xFFFFE000), VLEVEL as described in ADE9078 datasheet.(See appendix)
  - Set RUN=1.
- **Select desired Impulses/kWhr**
- **Using ADE9078_calibration_sheet compute CFxDEN. Configure CF registers.**
  - Set CFMODE and COMPMODE registers as needed in application.
  - Set WTHR = VARTHR = VATHR=0x100000.
  - Program calculated CFxDEN.
  - If desired, configure CF_LCFG register.
- **Apply Nominal Voltage and Current.**
- **If accurate RMS readings are required.**
  - Perform voltage and current gain (xVGAIN and xIGAIN) calibration using internal register read method.
  - Perform offset calibration if high accuracy is desired at lower end of dynamic range.
- **Calibrate the Energy.**
  - Perform phase(xPHCAL) calibration by recording CF/ Active Energy error/Active Energy impulses/kWHr at PF=1 and PF=0.5 lagging.
  - Perform Power Gain calibration at PF=1.
  - Perform Power Offset calibration if high accuracy is desired at lower end of dynamic range.

# Calibration Flow using CF outputs: Using the ADE9078_calibration_tool.xlsm

**Enter Input Conditions.The tool will calculate CFxDEN. Write the value to CF1DEN/CF2DEN/CF3DEN/CF4DEN.**

| Step 1: Input Conditions | |
|---|---|
| Select Channel Being Calibrated | Channel A |
| Enter Line Frequency(Hz) | 50 |
| Select Current Sensor | Current Transformer |
| Select Voltage Sensor | Resistor divider |
| Enter Nominal RMS Input Voltage(Vrms) | 220 |
| Enter Nominal RMS Input Current(Arms) | 20 |
| Enter Meter Constant(impulses/kWHr) | 3000 |
| Enter Energy Accumulation Time(sec) | 10 |
| | |
| **Step 2: Seting up CF pulses** | |
| Enter CT Turns ratio | 2500 |
| Enter Total CT Burden Resistor(Ohm) | 20 |
| Current Transfer Function(V/A) | 0.008 |
| Enter Top Leg (R1) of Divider Resistor (KOhm) | 990 |
| Enter Bottom Leg (R2)of Divider Resistor (kOhm) | 1 |
| Voltage Transfer Function(V/V) | 0.001009082 |
| Expected CF at Nominal Conditions(Hz) | 3.666666667 |
| Program xTHR to Recommended Value( xTHR=0x00100000) | 100000 |
| Nominal Voltage percentage of full scale | 31.40% |
| Nominal Current percentage of full scale | 22.62% |
| CFxDEN Register(hex) | C06 |
| K Coefficient for Voltage Channel(Codes in decimal/Vrms) | 75443.99383 |
| K Coefficient for Current Channel(Codes in decimal/Irms) | 598119.9831 |
| K Coefficient for Power Channel(Codes in decimal/Watt) | 336.2041736 |
| Energy Coefficient for xxTTHR_HI (Codes in decimal/ | 1.69209E-06 |

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# Calibration Flow using CF outputs: Using the ADE9078_calibration_tool.xlsm

- **Select calibration technique for rms voltage and current calibration.**
  - If accurate RMS readings are not required, this step can be skipped. xIGAIN & xVGAIN affects power datapath, hence xIGAIN & xVGAIN is performed before xPGAIN
  - If accurate RMS readings are required, use the tool to calculate xIGAIN and xVGAIN register values.

| Step 3:Voltage and Current Gain Calibration | |
|---|---|
| Select Calibration technique | Calibrate using Register values |
| Enter Measured xIRMS register value(hex) | B69000 |
| Enter Measured xVRMS register value(hex) | FD9200 |
| Expected xIRMS register value(hex) | B68820 |
| Expected xVRMS register value(hex) | FD42AF |
| AIGAIN Register(hex) | FFFFA7A9 |
| AVGAIN Register(hex) | FFFD7F64 |
| Enter Measured xIRMS register value after calibration(hex) | |
| Enter Measured xVRMS register value after calibration(hex) | |
| Current Error after Compensation | -100.00% |
| Voltage Error after Compensation | -100.00% |

| Step 3.1: RMS offset calibration | |
|---|---|
| Enter Offset Calibration Current(Arms) | |
| Enter Offset Calibration Voltage(Vrms) | |
| Enter Measured xIRMS register value(hex) | |
| Enter Measured xVRMS register value(hex) | |
| AIRMSOS Register(hex) | 0 |
| AVRMSOS Register(hex) | 0 |

# Calibration Flow using CF outputs: Using the ADE9078_calibration_tool.xlsm

- **Phase calibration**
  - Performed at 2 points, PF=1 and PF=0.5 lagging (when the active and reactive powers are positive) with the nominal inputs entered in step 1.
  - Enter measured CF/Error/Imp/kWhr in the input fields for PF=1 and PF=0.5.
  - Program calculated xPHCAL0 register

| Step 4: Phase calibration | Done With Active Energy parameters at PF=1 and Lagging PF = 0.5(Active and Reactive Energies are Positive) |
|---|---|
| Select Calibration technique | Calibrate using CF |
| Enter Calibrating Angle between V and I(°)(positive angle for lagging PF) | 60 |
| Expected CF for Active Energy(Hz) at PF=1 | 3.6667 |
| Expected CF for Active Energy(Hz) at calibrating angle | 1.8333 |
| Enter Measured CF for Active Energy(Hz) at PF=1 | 3.7500 |
| Enter Measured CF for Active Energy(Hz) at calibrating angle | 1.8000 |
| Desired Phase Error Compensation(°) | 1.322954191 |
| APHCAL0 Register(hex) | 1612E09 |

# Calibration Flow using CF outputs: Using the ADE9078_calibration_tool.xlsm

- **With nominal inputs entered in step 1, perform gain calibration**
  - Enter measured CF/Error/Imp/kWhr in the input field. Program the calculated xPGAIN register
- **Perform offset calibration if high accuracy at low dynamic range is required**

| Step 5: Power Gain Calibration | Done at lagging PF = 0.5, or PF=1 |
|---|---|
| Select Calibration technique | Calibrate using CF |
| Enter Angle between V and I(°) | 0 |
| Enter Measured CF for Active Energy(Hz) | |
| Expected CF for Active Energy(Hz) | 3.6667 |
| Expected CF for Reactive Energy(Hz) | 0.0000 |
| APGAIN Register(hex) | #DIV/0! |
| Enter Measured CF for Active Energy(Hz) after xPGAIN Calibration | |
| Active Energy Error after xPGAIN Calibration | -100.00% |

| Step 5.1: Power offset calibration | PF=1/0 for active/reactive respectively. Nominal voltage |
|---|---|
| Select Calibration technique | |
| Enter Accumulation Time for Offset calibration(sec) | |
| Enter Calibration Current(Arms) | |
| Enter Measured imp/kWHr for Active Energy | |
| Enter Measured imp/kWHr for Reactive Energy | |
| Enter Measured imp/kWHr for Fundamental Reactive Energy | |
| AWATTOS Register(hex) | 0 |
| AVAROS Register(hex) | 0 |
| AFVAROS Register(hex) | 0 |
| | |

# Calibration Flow using Internal Registers

- **Setup initialization registers.**
  - Set PGA Gain, HPF_CRN,INTEN(&DICOEFF=0xFFFFE000),VLEVEL as described in ADE90078 datasheet. Setup and enable energy accumulation (EP_CFG). Set RUN=1.
- **Apply Nominal Voltage and Current.**
- **If accurate RMS readings are required, calibrate RMS.**
  - Perform voltage and current gain (xVGAIN and xIGAIN) calibration.
  - Perform RMS offset calibration if high accuracy is desired at lower end of dynamic range.
  - After calibration, convert register values to electrical parameters using the following equations:
    - *Voltage(V)= xVRMS / Voltage Conversion Constant*
    - *Current(I)= xIRMS / Current Conversion Constant*
- **Calibrate the Energy.**
  - Perform Phase calibration(xPHCAL) at PF=0.5 lagging by recording active and reactive energy register values.
  - Perform Power Gain (xPGAIN) calibration at PF=1. After calibration,
    - *Power(Watt/VAR/VA) = Power register reading / Power Conversion Constant*
    - Energy(kWHr) = *Energy register reading* /Energy *Conversion Constant*
  - Perform Power offset calibration if high accuracy is desired at lower end of dynamic range.

# Calibration flow using internal registers: Using the ADE9078_calibration_tool.xlsm

- **The tool calibrates the ADE9078 using the ideal full scale codes mentioned in the datasheet.**

| Step 2: Seting up CF pulses | |
|---|---|
| Enter CT Turns ratio | 2500 |
| Enter Total CT Burden Resistor(Ohm) | 20 |
| Current Transfer Function(V/A) | 0.008 |
| Enter Top Leg (R1) of Divider Resistor (KOhm) | 990 |
| Enter Bottom Leg (R2)of Divider Resistor (kOhm) | 1 |
| Voltage Transfer Function(V/V) | 0.001009082 |
| Expected CF at Nominal Conditions(Hz) | 3.666666667 |
| Program xTHR to Recommended Value( xTHR=0x00100000) | 100000 |
| Nominal Voltage percentage of full scale | 31.40% |
| Nominal Current percentage of full scale | 22.63% |
| CFxDEN Register (hex) | [illegible] |
| K Coefficient for Voltage Channel(Codes in decimal/Vrms) | 75443.99383 |
| K Coefficient for Current Channel(Codes in decimal/Irms) | 598119.9831 |
| K Coefficient for Power Channel(Codes in decimal/Watt) | 336.2041736 |
| Energy Coefficient for xxTTHR_HI (Codes in decimal/kxHr) | 1.69209E-06 |

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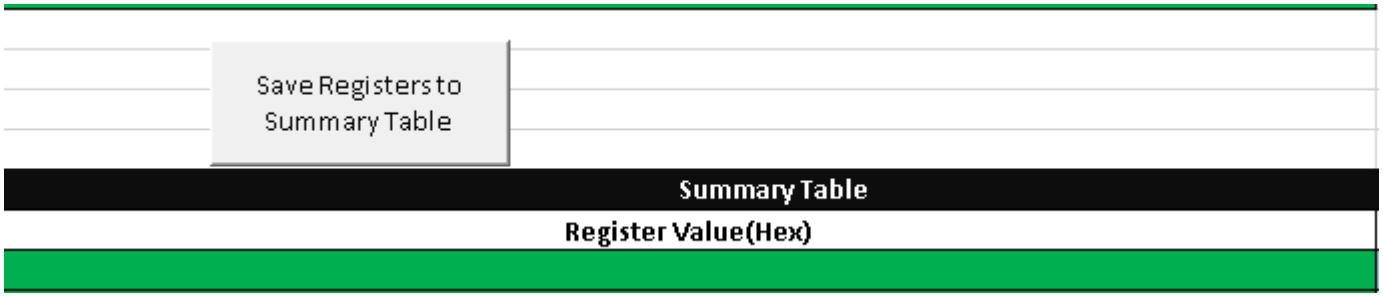
# Save

**Save Calibration values:**

- Press the save button after calibrating each channel.
- This populates the Summary Table



# Appendix: Register Details

| Register Address | Register Name | Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|---|---|
| 0x060 | CONFIG0 | [31:14] | RESERVED | | Reserved. | 0x0 | R |
| | | 13 | DISRPLPF | | Set this bit to disable the low-pass filter in the total reactive power datapath. | 0x0 | R/W |
| | | 12 | DISAPLPF | | Set this bit to disable the low-pass filter in the total active power datapath. | 0x0 | R/W |
| | | 11 | ININTEN | | Set this bit to enable the digital integrator in the Neutral Current channel. | 0x0 | R/W |
| | | 10 | VNOMC_EN | | Set this bit to use the nominal phase voltage rms, VNOM, in the computation of Phase C total apparent power, CVA. | 0x0 | R/W |
| | | 9 | VNOMB_EN | | Set this bit to use the nominal phase voltage rms, VNOM, in the computation of Phase B total apparent power, BVA. | 0x0 | R/W |
| | | 8 | VNOMA_EN | | Set this bit to use the nominal phase voltage rms, VNOM, in the computation of Phase A total apparent power, AVA. | 0x0 | R/W |
| | | 7 | RESERVED | | Reserved. | 0x0 | R |
| | | 6 | ZX_SRC_SEL | | This bit selects whether data going into the zero-crossing detection circuit comes before the high-pass filter, integrator, and phase compensation or afterwards. | 0x0 | R/W |
| | | | | 0 | After the high-pass filter, integrator, and phase compensation. | | |
| | | | | 1 | Before the high-pass filter, integrator, and phase compensation. | | |
| | | 5 | INTEN | | Set this bit to enable the integrators in the phase current channels. The neutral current channel integrator is managed by the ININTEN bit in the CONFIG0 register. | 0x0 | R/W |
| | | 4 | MTEN | | Set this bit to enable multipoint phase and gain compensation. If enabled, an additional gain factor, xIGAIN0 through xIGAIN4, is applied to the current channel based on the xIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values. | 0x0 | R/W |
| | | 3 | HPFDIS | | Set this bit to disable high-pass filters in all the voltage and current channels. | 0x0 | R/W |
| | | 2 | RESERVED | | Reserved. | 0x0 | R |
| | | [1:0] | ISUM_CFG | | ISUM Calculation configuration. | 0x0 | R/W |
| | | | | 00 | ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation). | | |
| | | | | 01 | ISUM = AI_PCF + BI_PCF + CI_PCF + NI_PCF (to determine mismatch between neutral and phase currents). | | |
| | | | | 10 | ISUM = AI_PCF + BI_PCF + CI_PCF - NI_PCF (to determine mismatch between neutral and phase currents). | | |
| | | | | 11 | ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation). | | |

# Appendix: Register Details

| Register Address | Register Name | Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|---|---|
| 0x4AF | CONFIG2 | [15:13] | RESERVED | | Reserved. | 0x0 | R |
| | | 12 | UPERIOD_SEL | | Set this bit to use a user configured line period, in USER_PERIOD, for the resampling calculation. If this bit is clear, the phase voltage line period selected by the LP_SEL[1:0] bits in the ZX_LP_SEL register is used. | 0x0 | R/W |
| | | [11:9] | HPF_CRN | | High-pass filter corner (f3dB) enabled when the HPFDIS bit in the CONFIG0 register = 0. | 0x6 | R/W |
| | | | | 000 | 38.695 Hz. | | |
| | | | | 001 | 19.6375 Hz. | | |
| | | | | 010 | 9.895 Hz. | | |
| | | | | 011 | 4.9675 Hz. | | |
| | | | | 100 | 2.49 Hz. | | |
| | | | | 101 | 1.2475 Hz. | | |
| | | | | 110 | 0.625 Hz. | | |
| | | | | 111 | 0.3125 Hz. | | |
| | | [8:0] | RESERVED | | Reserved. | 0x0 | R |
| | | | | | | | |
| 0x480 | RUN | [15:0] | Write this register to 1 to start the measurements. | | | 0x0000 | R/W |
| | | | | | | | |
| 0x40F | VLEVEL | [31:24] | RESERVED | | Reserved. | 0x0 | R |
| | | [23:0] | VLEVEL_VAL | | Register used in the algorithm that computes the fundamental reactive power. | 0x45D45 | R/W |

# Appendix: Register Details

| Register Address | Register Name | Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|---|---|
| 0x481 | CONFIG1 | 15 | EXT_REF | | Set this bit if using an external voltage reference. | 0x0 | R/W |
| | | [14:13] | RESERVED | | Reserved. | 0x0 | R |
| | | 12 | IRQ0_ON_IRQ1 | | Set this bit to combine all the interrupts onto a single interrupt pin, IRQ1, instead of using two pins, IRQ0 and IRQ1. Note that the IRQ0 pin still indicates the enabled IRQ0 events while in this mode and the IRQ1 indicates both IRQ1 and IRQ0 events. | 0x0 | R/W |
| | | 11 | BURST_EN | | Set this bit to enable burst read functionality on the registers from Address 0x500 to Address 0x6FF. Note that this bit disables the CRC being appended to SPI register reads. | 0x0 | R/W |
| | | 10 | RESERVED | | Reserved. | 0x0 | R |
| | | [9:8] | PWR_SETTLE | | These bits configure the time for the power and filter based rms measurements to settle before starting the power, energy and CF accumulations. | 0x0 | R/W |
| | | | | | 0: 64 ms. | | |
| | | | | | 1: 128 ms. | | |
| | | | | | 2: 256 ms. | | |
| | | | | | 3: 0 ms. | | |
| | | [7:6] | RESERVED | | Reserved. | 0x0 | R |
| | | 5 | CF_ACC_CLR | | Set this bit to clear the accumulation in the digital to frequency converter and CFDEN counter. Note that this bit automatically clears itself. | 0x0 | W |
| | | 4 | RESERVED | | Reserved. | 0x0 | R |
| | | [3:2] | CF4_CFG | | These bits select which function to output on the CF4 pin. | 0x0 | R/W |
| | | | | 00 | CF4, from digital to frequency converter. | | |
| | | | | 01 | CF4, from digital to frequency converter. | | |
| | | | | 10 | EVENT. | | |
| | | | | 11 | DREADY. | | |
| | | 1 | CF3_CFG | | This bit selects which function to output on the CF3 pin. | 0x0 | R/W |
| | | | | 0 | CF3, from digital to frequency converter. | | |
| | | | | 1 | Zero Crossing output selected by the ZX_SEL bits in the ZX_LP_SEL register. | | |
| | | 0 | SWRST | | Set this bit to initiate a software reset. Note that this bit is self clearing. | 0x0 | W |

# Appendix: Register Details

| Register Address | Register Name | Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|---|---|
| 0x425 | CF_LCFG | [31:23] | RESERVED | | Reserved. | 0x0 | R |
| | | 22 | CF4_LT | | If this bit is set, the CF4 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz. | 0x0 | R/W |
| | | 21 | CF3_LT | | If this bit is set, the CF3 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz. | 0x0 | R/W |
| | | 20 | CF2_LT | | If this bit is set, the CF2 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz. | 0x0 | R/W |
| | | 19 | CF1_LT | | If this bit is set, the CF1 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz. | 0x0 | R/W |
| | | [18:0] | CF_LTMR | | If the CFx_LT bit in CF_LCFG register is set, this value determines the active low pulse width of the CFx pulse. | 0x0 | R/W |
| | | | | | | | |
| 0x490 | CFMODE | 15 | CF4DIS | | CF4 output disable. Set this bit to disable the CF4 output and bring the pin high. Note that when this bit is set, the CFx bit in STATUS0 is not set when a CF pulse is accumulated in the digital to frequency converter. | 0x0 | R/W |
| | | 14 | CF3DIS | | CF3 output disable--see CF4DIS. | 0x0 | R/W |
| | | 13 | CF2DIS | | CF2 output disable--see CF4DIS. | 0x0 | R/W |
| | | 12 | CF1DIS | | CF1 output disable--see CF4DIS | 0x0 | R/W |
| | | [11:9] | CF4SEL | | Type of energy output on the CF4 pin. Configure TERMSEL4 in the COMPMODE register to select which phases are included. | 0x0 | R/W |
| | | | | 000 | Total active power. | | |
| | | | | 001 | Total reactive power. | | |
| | | | | 010 | Total apparent power. | | |
| | | | | 100 | Fundamental reactive power. | | |
| | | | | 110 | Total active power. | | |
| | | | | 111 | Total active power. | | |
| | | [8:6] | CF3SEL | | Selects type of energy output on CF3 pin--see CF4SEL. | 0x0 | R/W |
| | | [5:3] | CF2SEL | | Selects type of energy output on CF2 pin--see CF4SEL. | 0x0 | R/W |
| | | [2:0] | CF1SEL | | Selects type of energy output on CF1 pin--see CF4SEL. | 0x0 | R/W |

# Appendix: Register Details

| Register Address | Register Name | Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|---|---|
| 0x4B0 | EP_CFG | [15:13] | NOLOAD_TMR | | This register configures how many 4 kSPS samples to evaluate the no load condition over. | 0x0 | R/W |
| | | | | 000 | 64. | | |
| | | | | 001 | 128. | | |
| | | | | 010 | 256. | | |
| | | | | 011 | 512. | | |
| | | | | 100 | 1024. | | |
| | | | | 101 | 2048. | | |
| | | | | 110 | 4096. | | |
| | | | | 111 | Disable no load threshold. | | |
| | | [12:8] | RESERVED | | Reserved. | 0x0 | R |
| | | 7 | PWR_SIGN_SEL | | Selects whether the REVRPx bit follows the sign of the total or fundamental reactive power. | 0x0 | R/W |
| | | | | 0 | Total reactive power. | | |
| | | | | 1 | Fundamental reactive power. | | |
| | | 6 | RESERVED | | Reserved. | 0x0 | R |
| | | 5 | RD_RST_EN | | Set this bit to enable the energy register read with reset feature. If this bit is set, when one of the xWATTHR, xVAHR, xVARHR and xFVARHR register is read, it is reset and begins accumulating energy from zero. | 0x0 | R/W |
| | | 4 | EGY_LD_ACCUM | | If this bit = 0, the internal energy register is added to the user accessible energy register. If the bit is set, the internal energy register overwrites the user accessible energy register when the EGYRDY event occurs. | 0x0 | R/W |
| | | [3:2] | RESERVED | | Reserved. | 0x0 | R |
| | | 1 | EGY_TMR_MODE | | This bit determines whether energy is accumulated based on the number of 4 kSPS samples or zero crossing events configured in the EGY_TIME register. | 0x0 | R/W |
| | | | | 0 | Accumulate energy based on 4 kSPS samples. | | |
| | | | | 1 | Accumulate energy based on the zero crossing selected by the ZX_SEL bits in the ZX_LP_SEL register. | | |
| | | 0 | EGY_PWR_EN | | Set this bit to enable the energy and power accumulator, when the run bit is also set. | 0x0 | R/W |

# Appendix: Register Details

| Register Address | Register Name | Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|---|---|
| 0x491 | COMPMODE | [15:12] | RESERVED | | Reserved. | 0x0 | R |
| | | [11:9] | TERMSEL4 | | Phases to include in CF4 pulse output. Set the TERMSEL4[2] bit to one to include Phase C in the CF4 pulse output. Similarly, set TERMSEL4[1] to include Phase B and TERMSEL4[0] for Phase A. | 0x0 | R/W |
| | | [8:6] | TERMSEL3 | | Phases to include in CF3 pulse output--see TERMSEL4. | 0x0 | R/W |
| | | [5:3] | TERMSEL2 | | Phases to include in CF2 pulse output--see TERMSEL4. | 0x0 | R/W |
| | | [2:0] | TERMSEL1 | | Phases to include in CF1 pulse output--see TERMSEL4. | 0x0 | R/W |
| | | | | | | | |
| 0x494 | CF1DEN | [15:0] | CF1 denominator register. | | | 0xFFFF | R/W |
| 0x495 | CF2DEN | [15:0] | CF2 denominator register. | | | 0xFFFF | R/W |
| 0x496 | CF3DEN | [15:0] | CF3 denominator register. | | | 0xFFFF | R/W |
| 0x497 | CF4DEN | [15:0] | CF4 denominator register. | | | 0xFFFF | R/W |
| | | | | | | | |
| 0x492 | ACCMODE | [15:9] | RESERVED | | Reserved. | 0x0 | R |
| | | 8 | SELFREQ | | This bit is used to configure the IC for a 50 Hz or 60 Hz system. This setting is used in the fundamental reactive power measurement and to set the default line period used for resampling calculations if a zero crossing is not present. | 0x0 | R/W |
| | | | | 0 | 50 Hz. | | |
| | | | | 1 | 60 Hz. | | |
| | | 7 | ICONSEL | | Set this bit to calculate the current flowing through IB from the IA and IC measurements. If this bit is set, IB = −IA − IC. | 0x0 | R/W |
| | | [6:4] | VCONSEL | | Three-wire and four-wire hardware configuration selection. | 0x0 | R/W |
| | | | | 000 | 4-wire wye. | | |
| | | | | 001 | 3-wire delta. VB' = VA − VC. | | |
| | | | | 010 | 4-wire wye, non-Blondel compliant. VB' = −VA − VC. | | |
| | | | | 011 | 4-wire delta, non- Blondel compliant. VB' = −VA. | | |
| | | | | 100 | 3-wire delta. VA' = VA − VB; VB' = VA − VC; VC' = VC − VB. | | |
| | | [3:2] | VARACC | | Total and fundamental reactive power accumulation mode for energy registers and CFx pulses. | 0x0 | R/W |
| | | | | 00 | Signed accumulation mode. | | |
| | | | | 01 | Absolute Value accumulation mode. | | |
| | | | | 10 | Positive accumulation mode. | | |
| | | | | 11 | Negative accumulation mode. | | |
| | | [1:0] | WATTACC | | Total and fundamental active power accumulation mode for energy registers and CFx pulses--see VARACC. | 0x0 | R/W |