



EV-ADF4155EB1Z (08-038558) Rev. A - Component Side View.
Drill Drawing

SIZE	QTY	SYM	PLATED	TOL
1.778	4	✕	YES	+/-0.08
1	14	◇	YES	+/-0.08
0.4	84	⊗	YES	+/-0.08
1.0414	14	⊠	YES	+/-0.08
0.25	635	⊕ ^A	YES	+/-0.08
0.5	41	⊕ ^B	YES	+/-0.08

1. Material: Four layer, R04003C/FR4 combination - See stackup diagram below.
Finished Board shall be RoHS compliant.
2. Plated thru holes and the conductive pattern electroplated with 25uM min. thick copper. Terminal areas and plated thru holes to be ENIG plated.
3. Datum for (x,y) co-ordinate drill files at LLH corner.
4. Processing tolerances:
A. Conductive pattern front to back registration within 0.1mm total.
B. Minimum annular ring surrounding holes: 0.05mm
C. Finished conductive pattern within 0.05mm of true size.
5. Warp and twist within 1%.
6. Dimensions are for the finished part.
7. Solder Mask: Liquid photo imagable solder mask over bare copper (SMOBC), colour green, both sides using the patterns provided. No mask is permitted on the terminal areas. Soldermask to etch registration within 0.127mm total.
8. Screening: Screen using mask provided on component side only.
Use indelible white ink. Nomenclature shall be legible
Screen to etch registration within 0.2mm total.
9. The stackup and trace/gap widths below are designed to achieve 50-ohm impedance controlled traces on Layer 1 & 4 using "Grounded Co-Planar Waveguide" technology.
Trace Width: 0.381mm (0.015") traces on Layer 1 (Component Side).
Trace/copper gap: 0.3048mm (0.012")
Dielectric Material - 0.008" Rogers 4003C
Er of Material: 3.38
10. The bare board manufacturer shall provide proof of measurement of impedance and also provide test coupons with the bare boards.
12. Manufacturer to add Ident, UL number & Date Code in this area on Silkscreen
(Use YY/WW for Datecode)

4-LAYER ROGERS R04003C/FR4 COMBINATION
50 OHM IMPEDANCE CONTROLLED STACKUP (0.062" +/-0.003")

