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Evaluation Board for the ADF4157 Fractional-N PLL Frequency Synthesizer

FEATURES

- Self-contained evaluation board, including frequency synthesizer, VCO, TCXO for reference frequency, and loop filter
- Designed for 10 MHz PFD frequency, minimum charge pump current, and a 20 kHz loop bandwidth
- Accompanying software allows complete control of synthesizer functions from a PC

EVALUATION KIT CONTENTS

- EV-ADF4157SD1Z board
- CD that includes
  - Self-installing software that allows users to control the board and exercise all functions of the device
  - Electronic version of the ADF4157 data sheet
  - Electronic version of the UG-393 user guide

ADDITIONAL EQUIPMENT

- PC running Windows XP or more recent version
- SDP-S board (system demonstration platform, serial only)
- Spectrum analyzer
- Oscilloscope (optional)

DOCUMENTS NEEDED

- ADF4157 data sheet
- UG-393 user guide

REQUIRED SOFTWARE

- Analog Devices Frac-N PLL software (Version 4 or higher)
- ADIsimPLL

GENERAL DESCRIPTION

This evaluation board allows the user to evaluate the performance of the ADF4157 frequency synthesizer for phase-locked loops (PLLs). The SDP-S controller board allows software programming of the frequency synthesizer. Figure 1 shows the board, which contains the ADF4157 synthesizer, the power supplies, a TCXO reference, and an RF output signal. There is also a loop filter (20 kHz), a VCO (Z-Communications, Inc., V940ME03-LF), and an external reference SMA input. The evaluation board is set up for a 10 MHz PFD frequency.

Figure 1 shows the board with all necessary components inserted.

EVALUATION BOARD

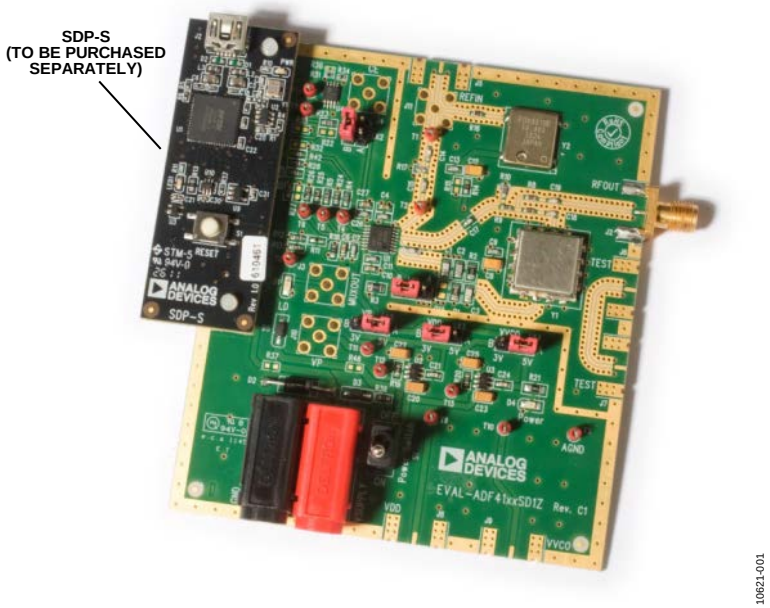

Figure 1. EV-ADF4157SD1Z with SDP-S

TABLE OF CONTENTS

REVISION HISTORY

7/12—Revision 0: Initial Version

QUICK START GUIDE

Follow these steps to evaluate the ADF4157 frequency synthesizer after ensuring that the on-board links are correct with reference to Table 1:

1. Install the Analog Devices Frac-N PLL software.
2. Connect the SDP-S motherboard to the PC and to the EV-ADF4157SD1Z.
3. Follow the hardware driver installation procedure that appears if you are using Windows® XP.
4. Connect the power supplies to banana connectors (6 V to 12 V).
5. Run the Frac-N PLL software.
6. Select the SDP board and the ADF4157 device in the **Select Device and Connection** tab of the main window.
7. Click the **Main Controls** tab, and then update all registers.
8. Connect the spectrum analyzer to J2.
9. Measure the results.

EVALUATION BOARD HARDWARE

The evaluation board requires the use of an SDP-S motherboard to program the device. The SDP-S is not included with the evaluation board. The EV-ADF4157SD1Z schematics are shown in Figure 21 to Figure 23.

POWER SUPPLIES

The board is powered from external banana connectors. The voltage can vary between 6 V and 12 V. The power supply circuit provides 3.0 V to the V_{DD} of the ADF4157 and allows the user to choose either 3.0 V or 5 V for the V_P of the ADF4157 frequency synthesizer. The default settings for V_{DD} and V_P are 3.0 V and 5 V, respectively. Note that V_{DD} should never exceed 3.3 V because exceeding this voltage level may damage the device.

External power supplies can be used to directly drive the ADF4157 frequency synthesizer. In this case, the user must insert SMA connectors as shown in Figure 2.

INPUT SIGNALS

A 10 MHz TCXO reference source from Fox Electronics is fitted as the default option. An external reference generator can also be used as the reference input. A low noise, high slew rate reference source is required to achieve the specified performance of the ADF4157 frequency synthesizer. An SMA connector fitted to J11 can be connected to an external reference generator and used as the reference source. Alternatively, the edge mount connector, J5, can be inserted and used instead of J11. To use any external reference option, remove the 0 Ω R16 and R14 links.

Digital SPI signals are supplied through the SDP connector, J1. The SDP-S board is recommended. The SDP-Blackfin (SDP-B) board can also be used, but Resistor R57 must be removed from the SDP-B board. Some additional spurious low frequencies may appear if the SDP-B connector is used.

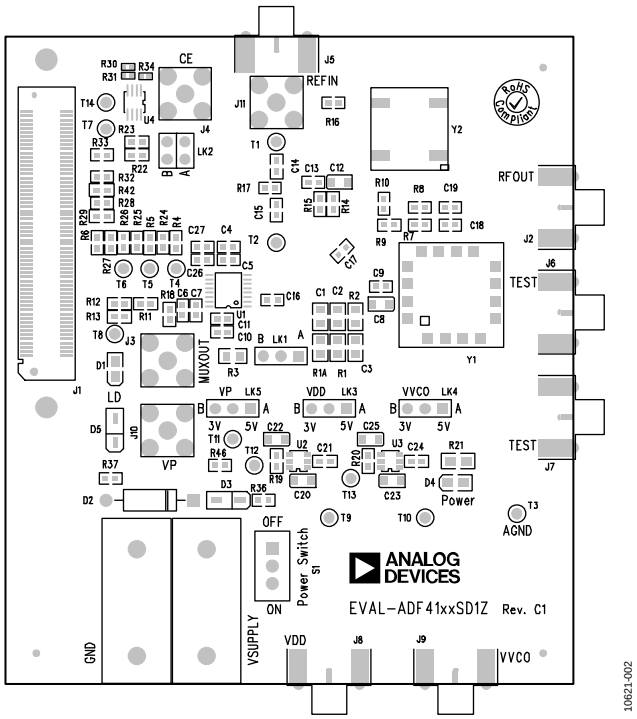

Figure 2. Evaluation Board Silkscreen

OUTPUT SIGNALS

All components necessary for local oscillator (LO) generation are on the board. The PLL comprises the ADF4157 frequency synthesizer, a passive loop filter, and the VCO. A 5.8 GHz VCO from Z-Communications is supplied with the evaluation board. A 20 kHz low-pass filter is inserted between the charge pump output and the VCO input. The 0.31 mA charge pump current setting is used. The VCO output is available at RFOUT through a standard SMA connector, J2. The MUXOUT signal can be monitored at Test Point T8 or at SMA Connector J3.

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

Link positions and their respective functions are outlined in Table 1.

Table 1. Link Positions and Functions

Link	Position	Options	Description
LK1	A	R1A	Not used
	B	RSET	Normal operation
LK2	A	GND	Hardware power-down
	B	VDD	Normal operation
LK3 (V_{DD})	A	5 V	Not used
	B	3 V	Normal operation
LK4 (V_{VCO})	A	5 V	VCO supply (5 V)
	B	3 V	VCO supply (3 V)
LK5 (V_P)	A	5 V	V_P supply (5 V)
	B	3 V	V_P supply (3 V)

SYSTEM DEMONSTRATION PLATFORM (SDP)

The system demonstration platform (SDP) is a series of controller boards, interposer boards, and daughter boards that can be used for easy, low cost evaluation of Analog Devices, Inc., components and reference circuits. It is a reusable platform whereby a single controller board can be reused in various daughter board evaluation systems.

Controller boards connect to a PC via a USB 2.0 high speed port and provide a range of communication interfaces on a 120-pin connector. The pinout for this connector is strictly defined. A receptacle for this 120-pin connector is included on all SDP daughter boards, component evaluation boards, and Circuits from the Lab® reference circuit boards. There are two controller boards in the platform: the SDP-B, which is based on the Blackfin® ADSP-BF527, and the SDP-S, which is a serial interface only controller board. The SDP-S has a subset of the SDP-B functionality.

Interposer boards route signals between the SDP 120-pin connector and a second connector. When the second connector is also a 120-pin connector, the interposer can be used for signal monitoring of the 120-pin connector signals. Alternatively, the second connector allows SDP platform elements to be integrated into a second platform, for example, the BeMicro SDK. More information on the SDP can be found at www.analog.com/sdp.

EVALUATION BOARD SETUP PROCEDURE

INSTALLING THE FRAC-N PLL SOFTWARE

Use the following steps to install the SDP drivers and the Analog Devices Frac-N PLL software.

1. Install the Frac-N PLL software by double-clicking **ADI_PLL_Frac-N_Setup.msi**.
   If you are using Windows XP, follow the instructions in the Windows XP Frac-N PLL Software Installation Guide section (see Figure 3 to Figure 7).
   If you are using Windows Vista or Windows 7, follow the instructions in the Windows Vista and Windows 7 Frac-N PLL Software Installation Guide section (see Figure 8 to Figure 12).
   Note that the software requires Microsoft Windows Installer and Microsoft .NET Framework 3.5 (or higher). The installer connects to the Internet and downloads Microsoft .NET Framework automatically. Alternatively, before running **ADI_PLL_Frac-N_Setup.msi**, both the installer and .NET Framework can be installed from the CD provided in the evaluation board kit.
2. Connect your SDP board (black) to a PC using the supplied USB cable.
   If you are using Windows XP, follow the steps in the Windows XP SDP-S Board Driver Installation Guide section (see Figure 13 to Figure 16).
   If you are using Windows Vista or Windows 7, the drivers install automatically.

Windows XP Frac-N PLL Software Installation Guide

1. Click **Next**.

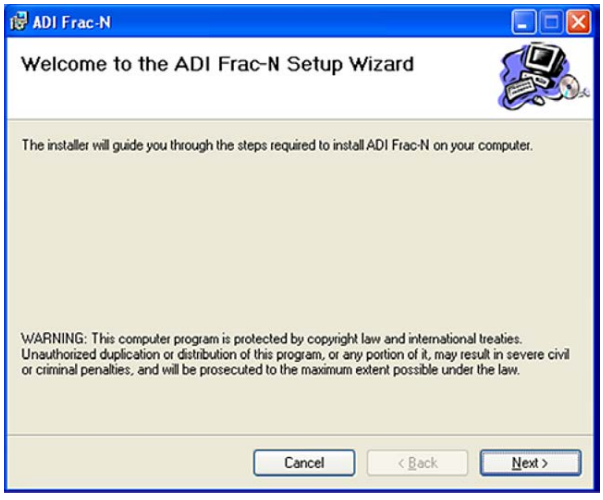

Figure 3. Windows XP Frac-N PLL Software Installation, Setup Wizard

2. Choose an installation directory and click **Next.**

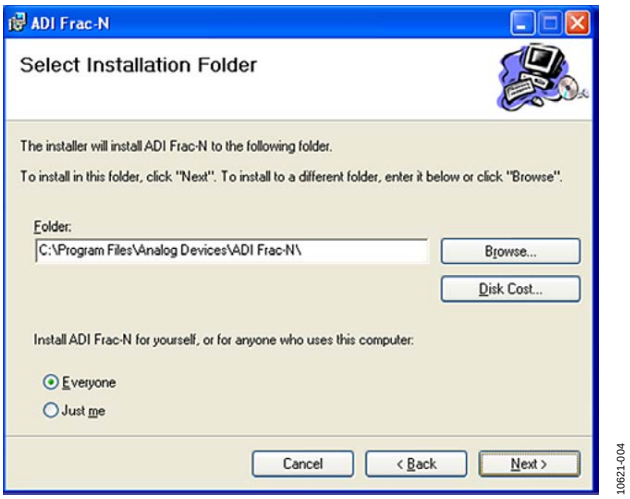

Figure 4. Windows XP Frac-N PLL Software Installation, Select Installation Folder

3. Click **Next.**

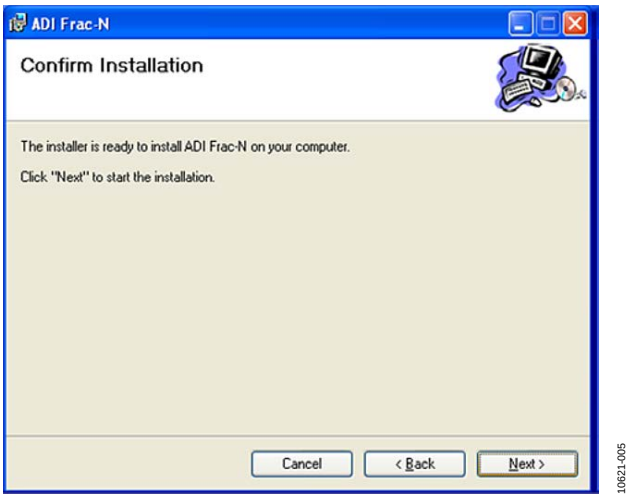

Figure 5. Windows XP Frac-N PLL Software Installation, Confirm Installation

4. Click **Continue Anyway**.

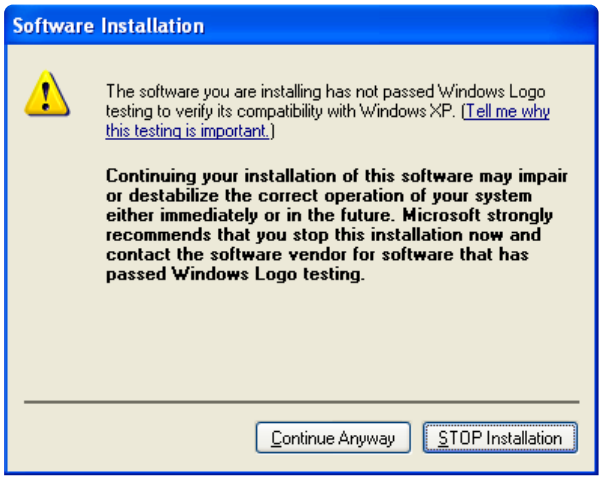

Figure 6. Windows XP Frac-N PLL Software Installation, Logo Testing

5. Click **Close.**

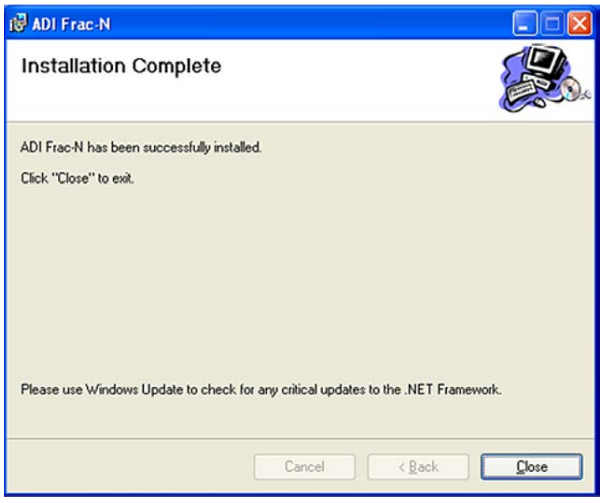

Figure 7. Windows XP Frac-N PLL Software Installation, Installation Complete

Windows Vista and Windows 7 Frac-N PLL Software Installation Guide

1. Click **Next**.

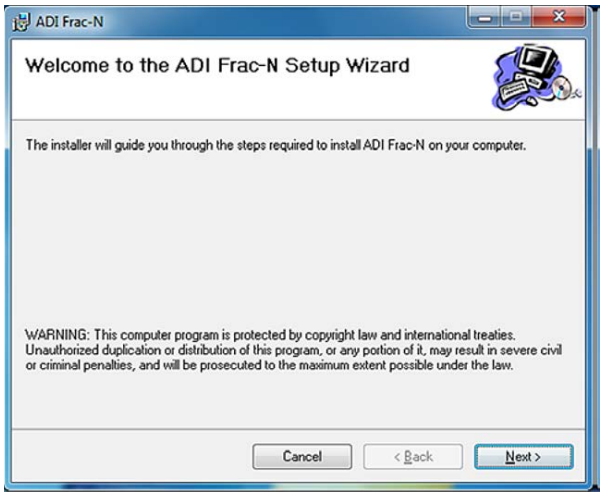

Figure 8. Windows Vista/Windows 7 Frac-N PLL Software Installation, Setup Wizard

2. Choose an installation directory and click **Next.**

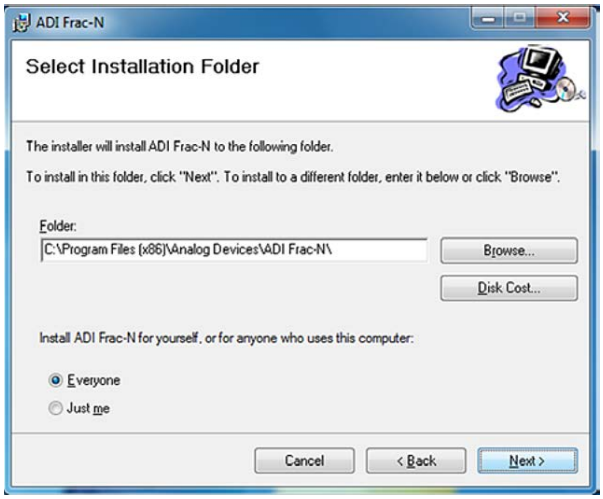

Figure 9. Windows Vista/Windows 7 Frac-N PLL Software Installation, Select Installation Folder

3. Click **Next**.

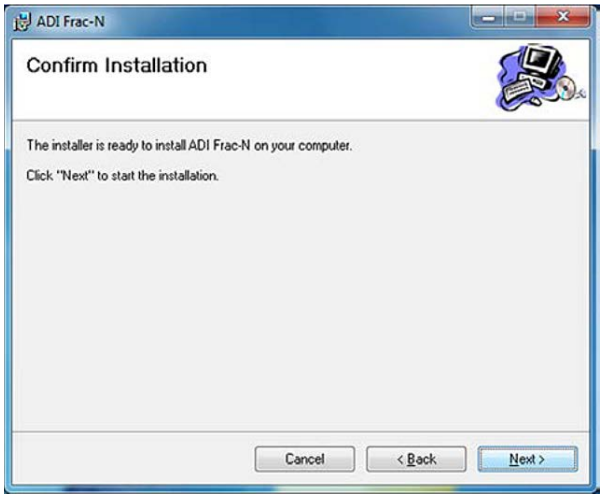

Figure 10. Windows Vista/Windows 7 Frac-N PLL Software Installation, Confirm Installation

4. Click **Install**.

Figure 11. Windows Vista/Windows 7 Frac-N PLL Software Installation, Start Installation

5. Click **Close**.

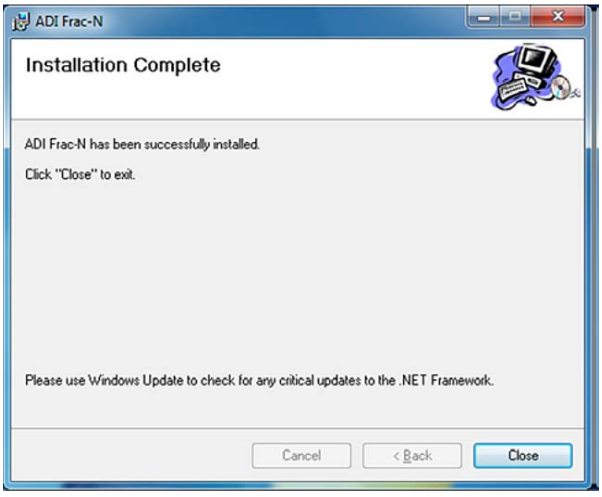

Figure 12. Windows Vista/Windows 7 Frac-N PLL Software Installation, Installation Complete

Windows XP SDP-S Board Driver Installation Guide

1. Choose **Yes, this time only**, and click **Next**.

Figure 13. Windows XP SDP-S Board Driver Installation, Found New Hardware Wizard

2. Click **Next**.

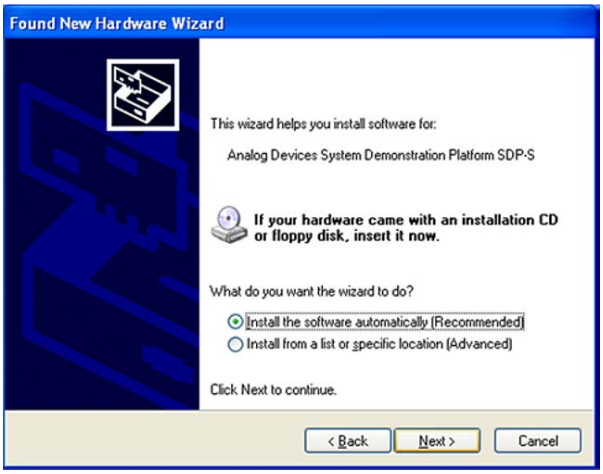

Figure 14. Windows XP SDP-S Board Driver Installation, Installation Options

3. Wait for the installation program to copy all the necessary files.

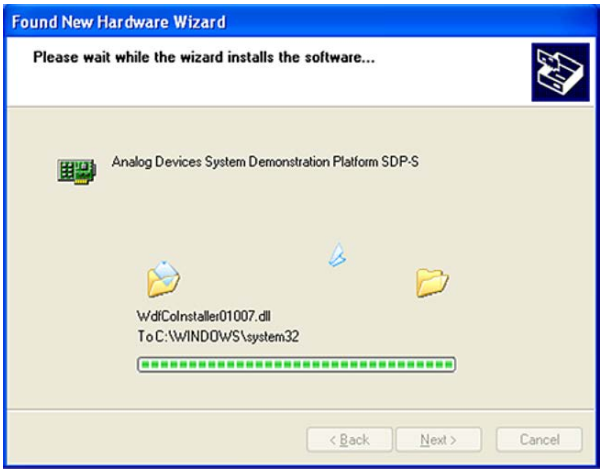

Figure 15. Windows XP SDP-S Board Driver Installation, Logo Testing

4. Click **Finish**.

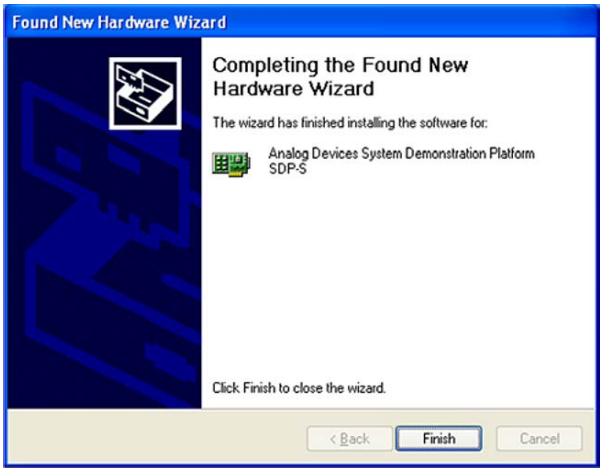

Figure 16. Windows XP SDP-S Board Driver Installation, Complete Installation

EVALUATION BOARD SOFTWARE

The control software for the EV-ADF4157SD1Z is provided on the CD included in the evaluation board kit. To install the software, see the Installing the Frac-N PLL Software section.

To run the software, click the **ADI Frac-N** file on the desktop or from the **Start** menu.

On the **Select Device and Connection** tab, choose the device and connection method, and then click **Connect.**

Confirm that **SDP board connected** is displayed at the bottom left of the window (see Figure 17). If this message is not displayed, the software cannot connect to the evaluation board.

Note that when the SDP board is connected, there is about a 5 sec to 10 sec delay before the status label changes.

From the **File** menu, the current settings can be saved to and loaded from a text file.

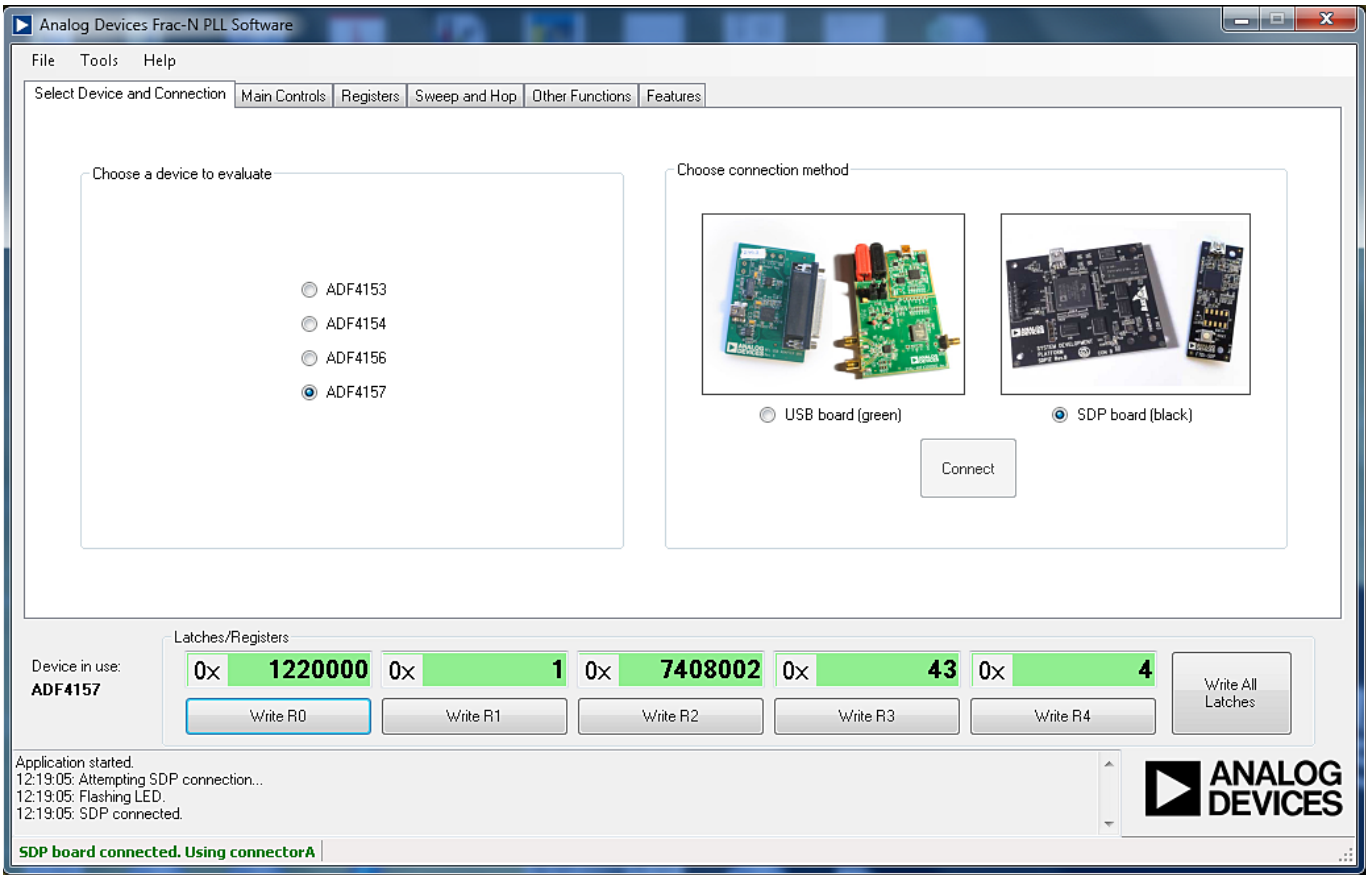

Figure 17. Frac-N PLL Software, Main Window—Select Device and Connection

The **Main Controls** tab controls the PLL settings (see Figure 18).

Use the **Reference Frequency** text box to set the correct reference frequency and the reference frequency divider. The default reference frequency in this box is 10 MHz.

Use the **RF Settings** section to control the output frequency. You can type the desired output frequency in the **RF VCO Output Frequency** text box (in megahertz).

In the **Registers** tab, you can manually input the desired value to be written to the registers.

In the **Sweep and Hop** tab, you can make the device sweep a range of frequencies or hop between two set frequencies.

In the **Latches/Registers** section at the bottom of the **Main Controls** tab of the main window, the values to be written to each register are displayed. If the background on the text box is green, the value displayed is different from the value actually on the device. Click **Write Rx** (where x = 0 to 4) to write the value displayed to the device.

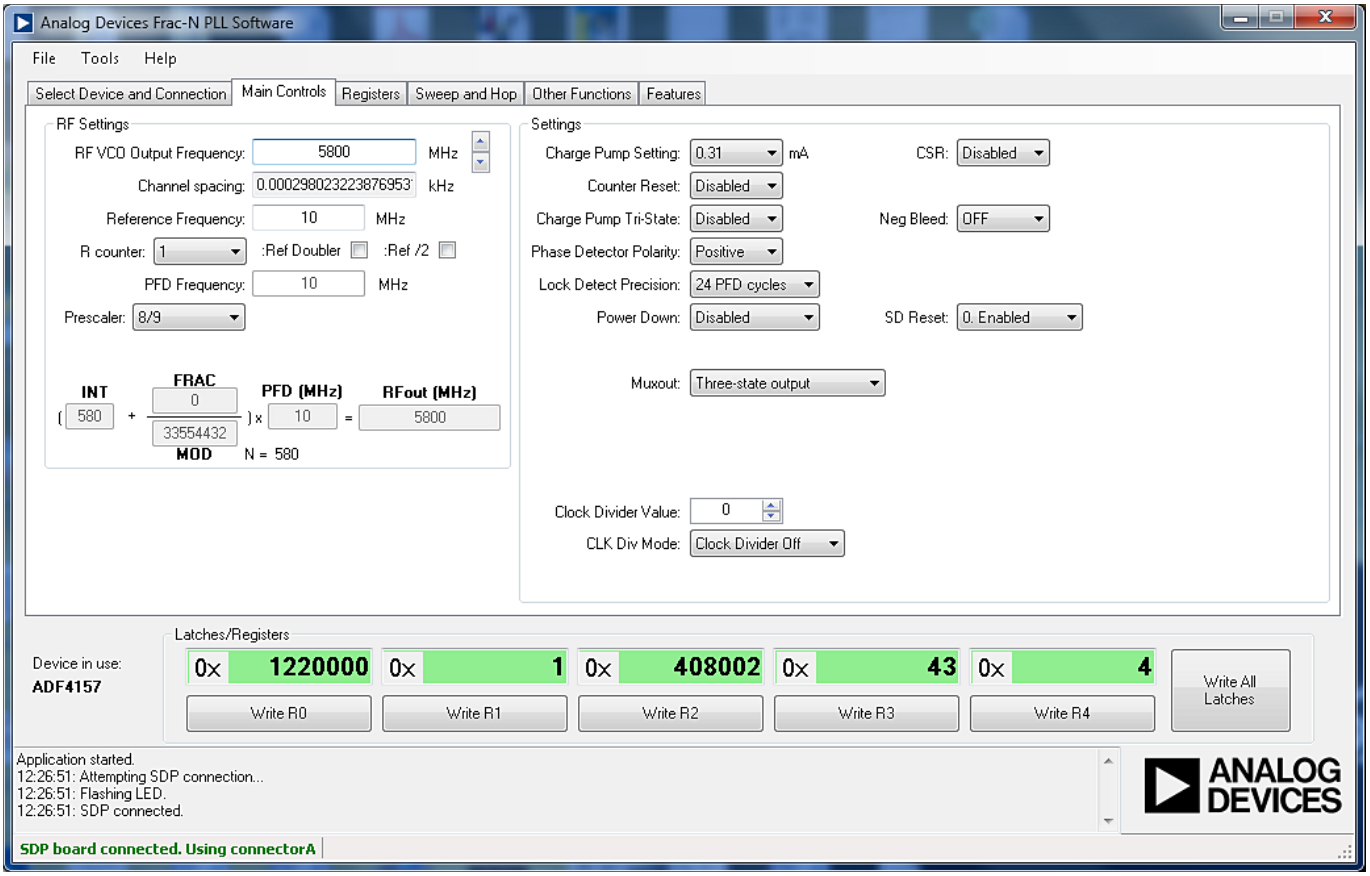

Figure 18. Frac-N PLL Software, Main Window—Main Controls

EVALUATION AND TEST

To evaluate and test the performance of the ADF4157 frequency synthesizer, use the following procedure:

1. Install the Frac-N PLL software.
2. Connect the SDP-S connector to the EV-ADF4157SD1Z.
3. Connect the SDP board to a PC using the supplied USB cable.
4. Follow the hardware driver installation procedure that appears if you are using Windows XP.
5. Connect the power supplies to banana connectors (6 V to 12 V) and ensure that the power switch is in the on position.
6. Connect the spectrum analyzer to Connector J2.
7. Run the Frac-N PLL software.
8. Select the SDP board and the ADF4157 device in the **Select Device and Connection** tab in the main window of the evaluation board software.
9. In the **Main Controls** tab in the main window of the evaluation board software, set the VCO center frequency in the **RF VCO Output Frequency** text box (the example in Figure 19 uses a 5800 MHz VCO). Set the **PFD Frequency** text box to 10 MHz, and program the **Reference Frequency** value to equal 10 MHz. The current listed in the **Charge Pump Setting** text box should equal 0.31 mA. See Figure 20 for the suggested setup.
10. Measure the output spectrum. Figure 19 shows a 5800 MHz output.

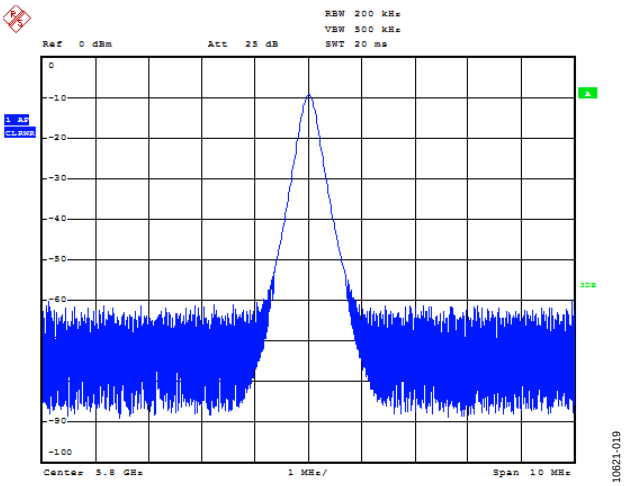

Figure 19. Spectrum Analyzer Display

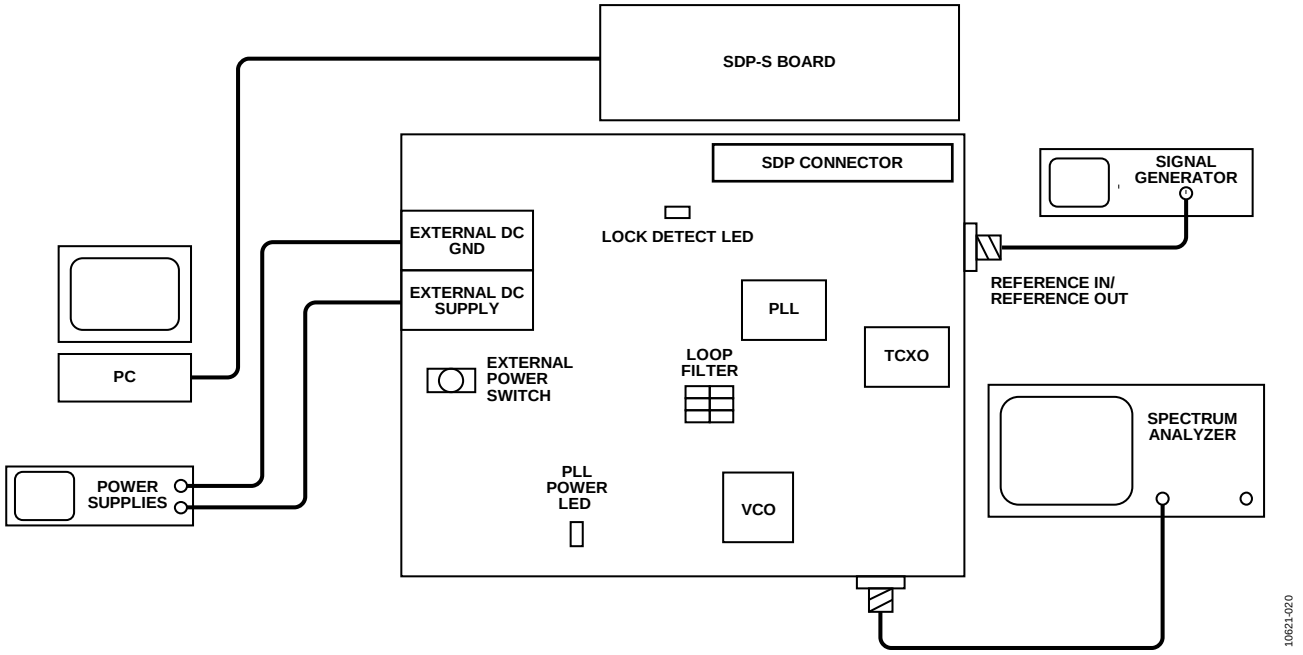

Figure 20. Typical Evaluation Setup

EVALUATION BOARD SCHEMATICS AND ARTWORK

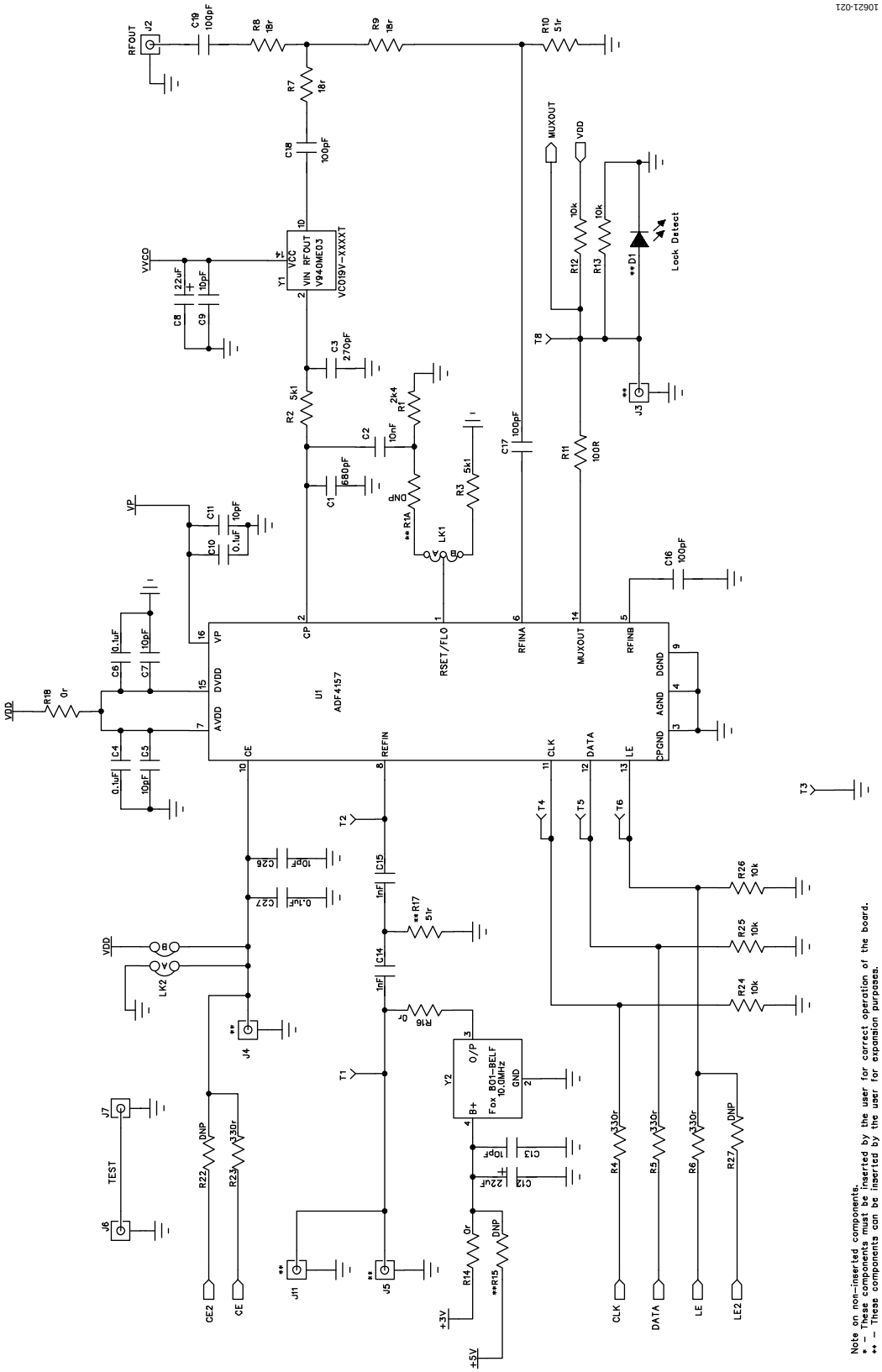

Figure 21. Evaluation Board Schematic (Page 1)

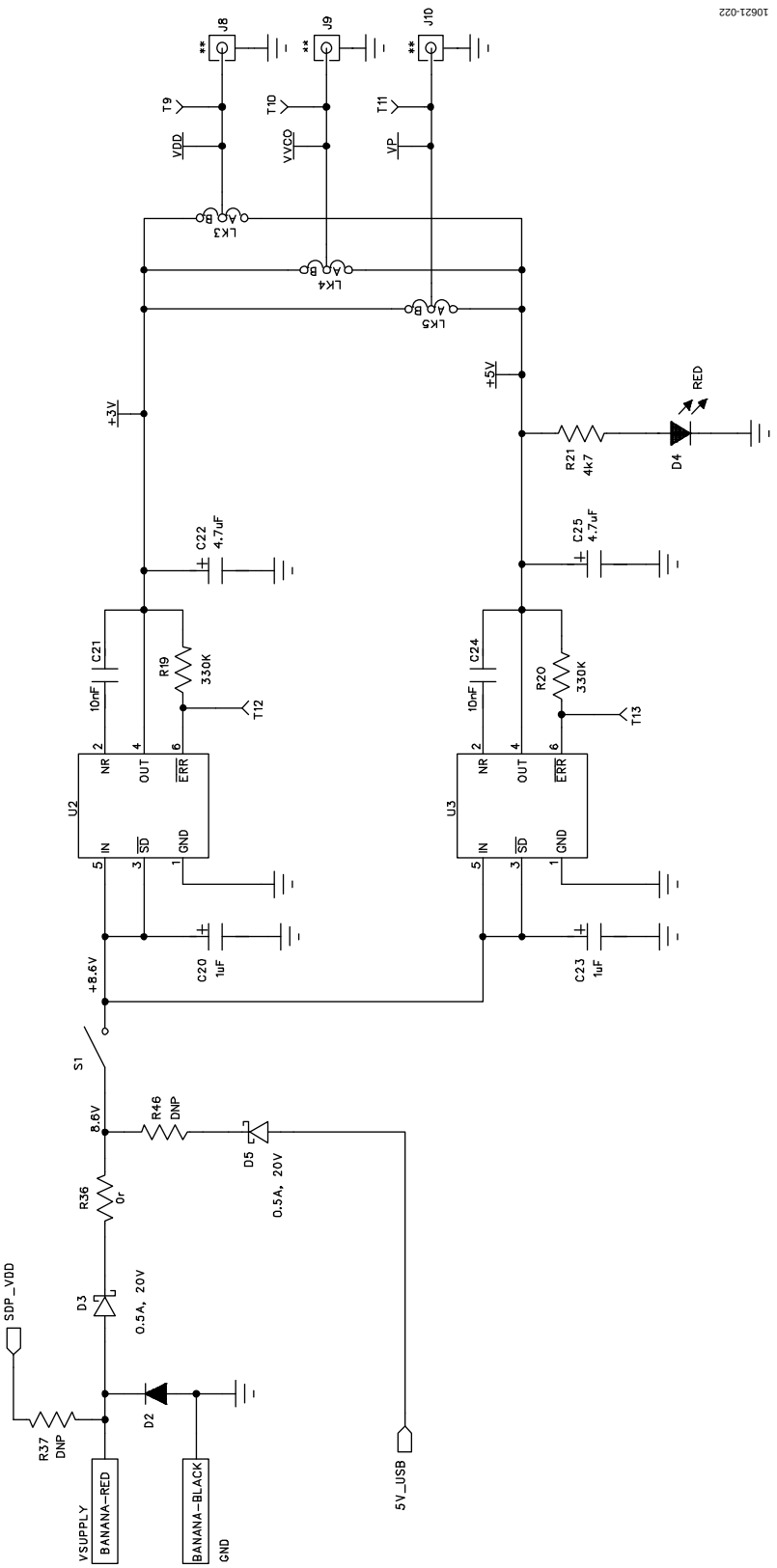

Figure 22. Evaluation Board Schematic (Page 2)

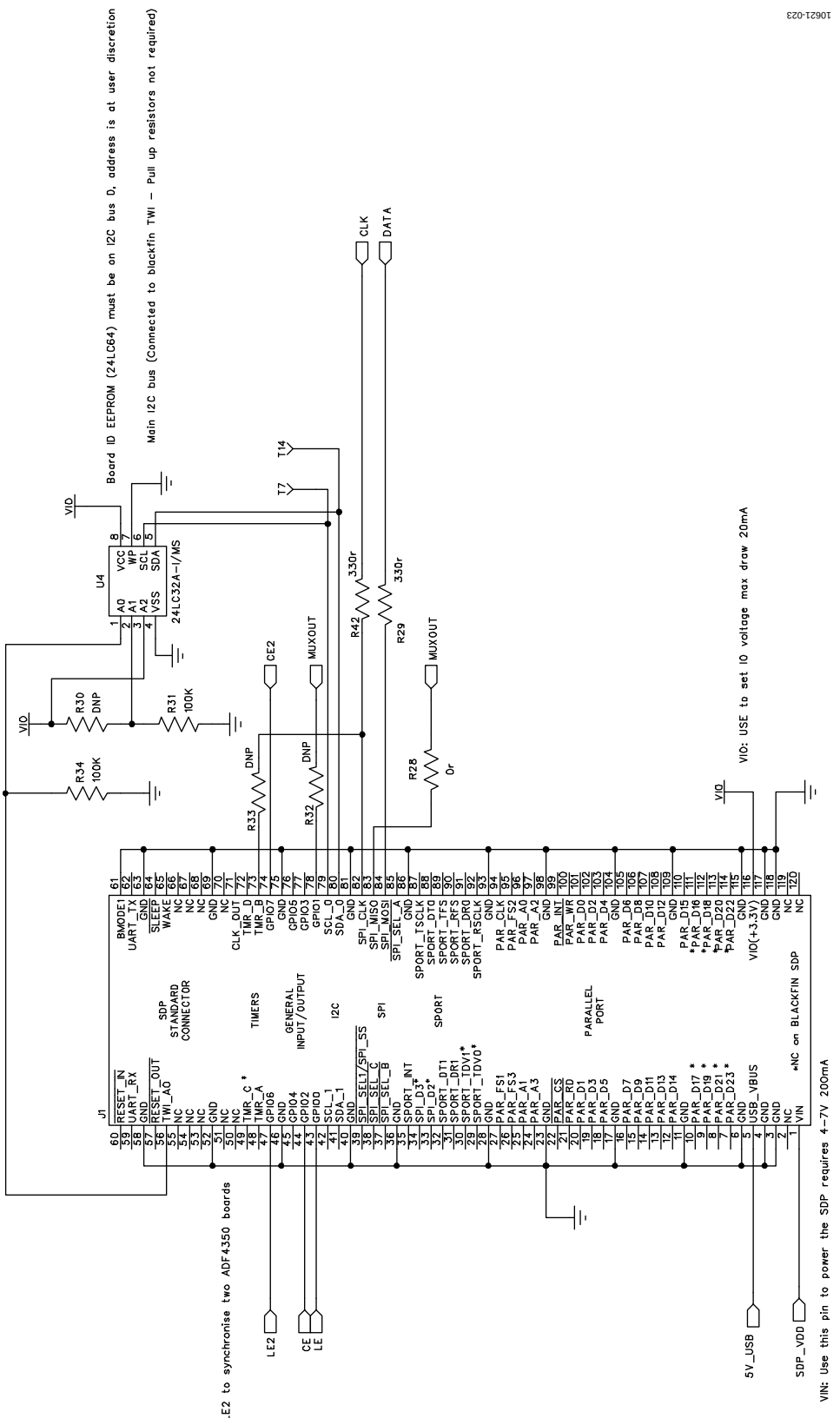

Figure 23. Evaluation Board Schematic (Page 3)

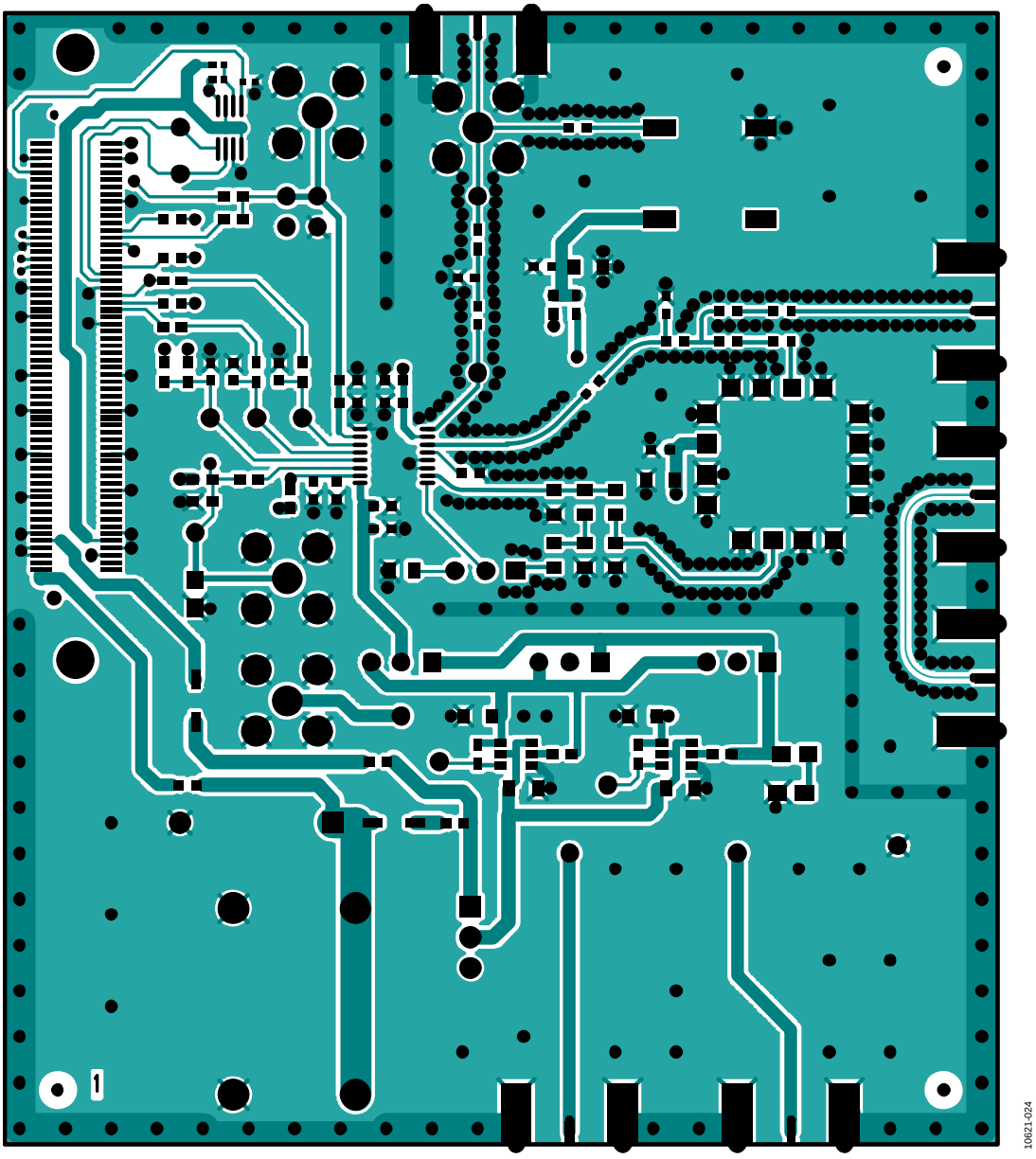

Figure 24. Layer 1 (Component Side)

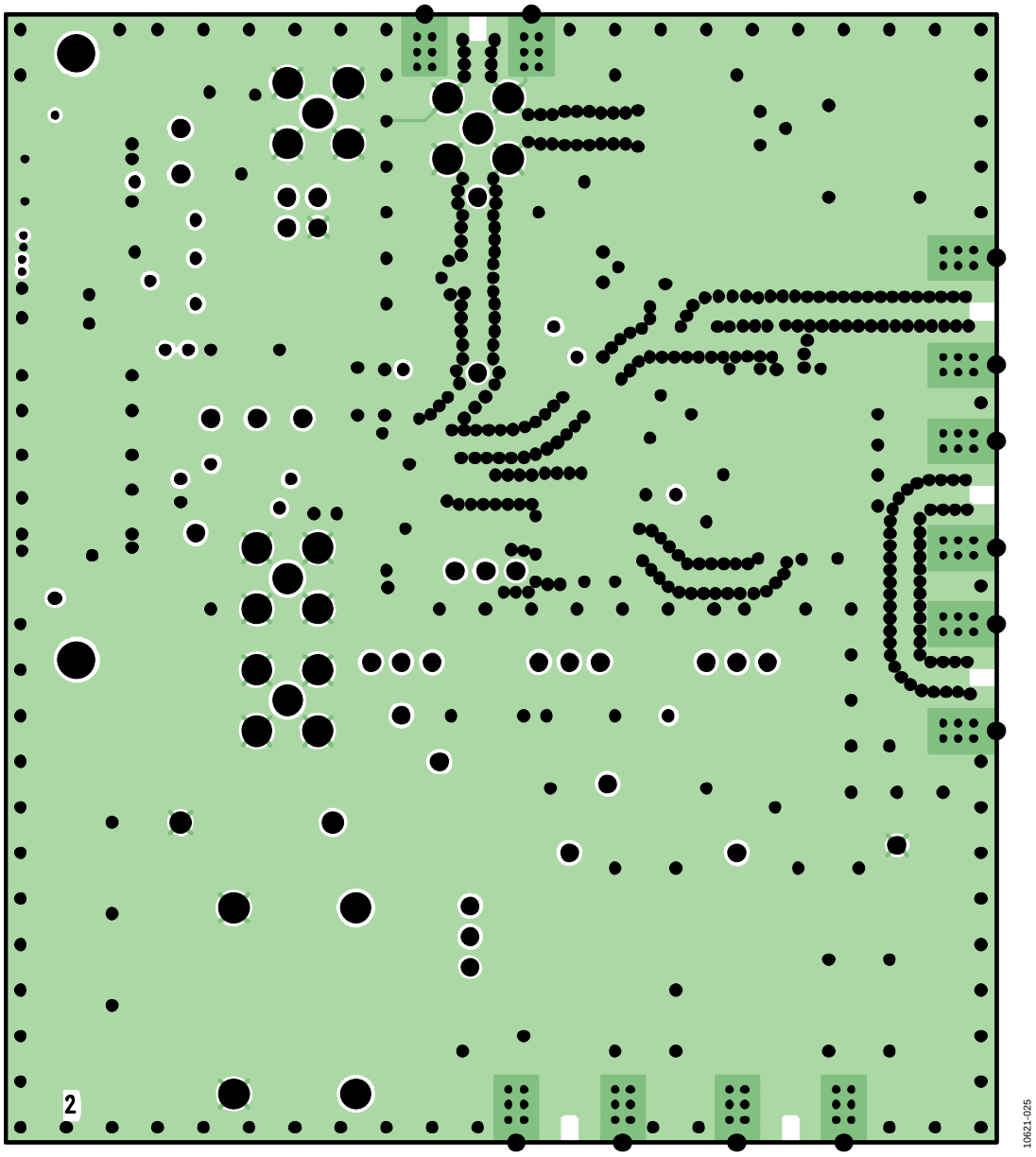

Figure 25. Layer 2 (Ground Plane)

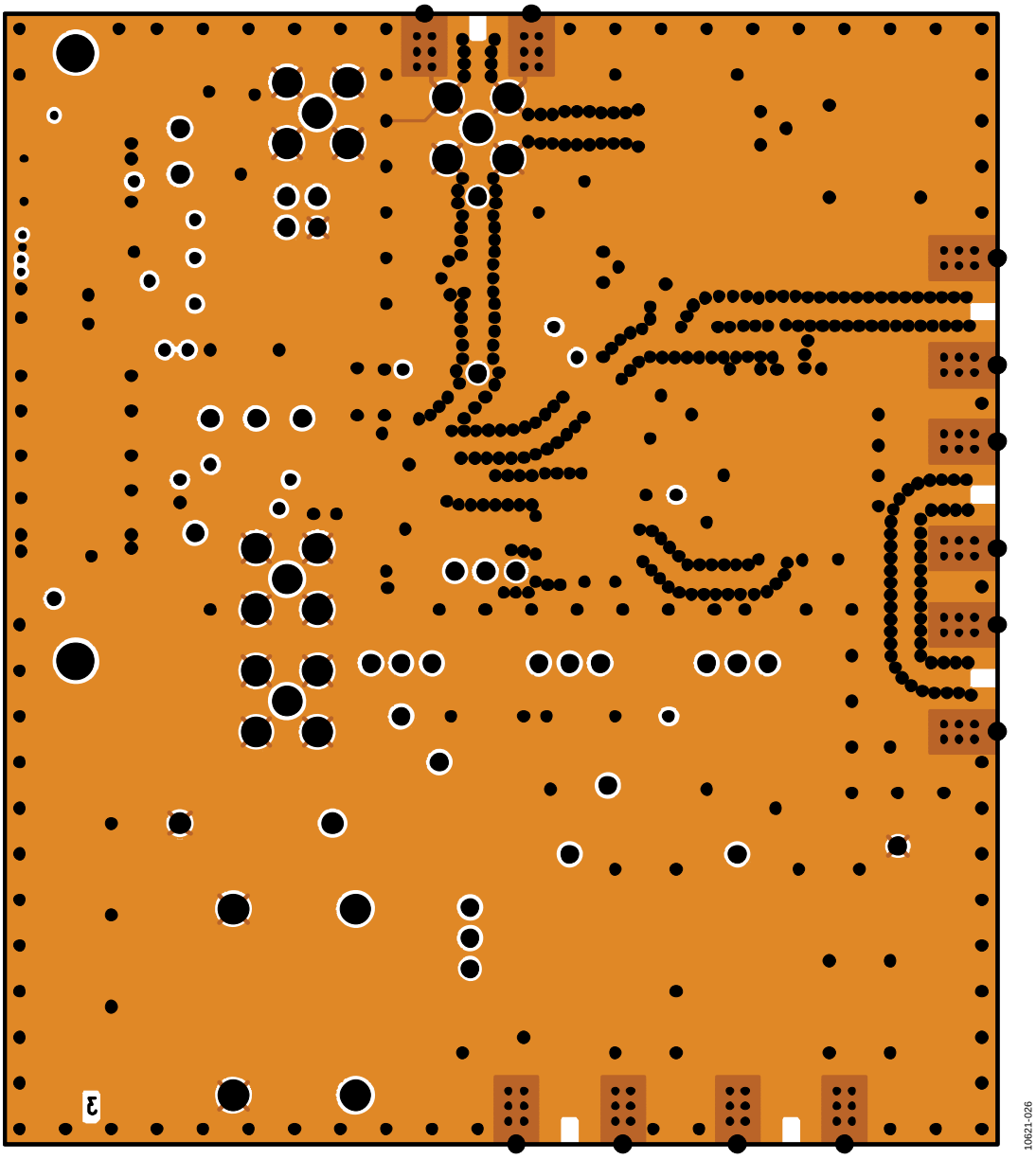

Figure 26. Layer 3 (Power Plane)

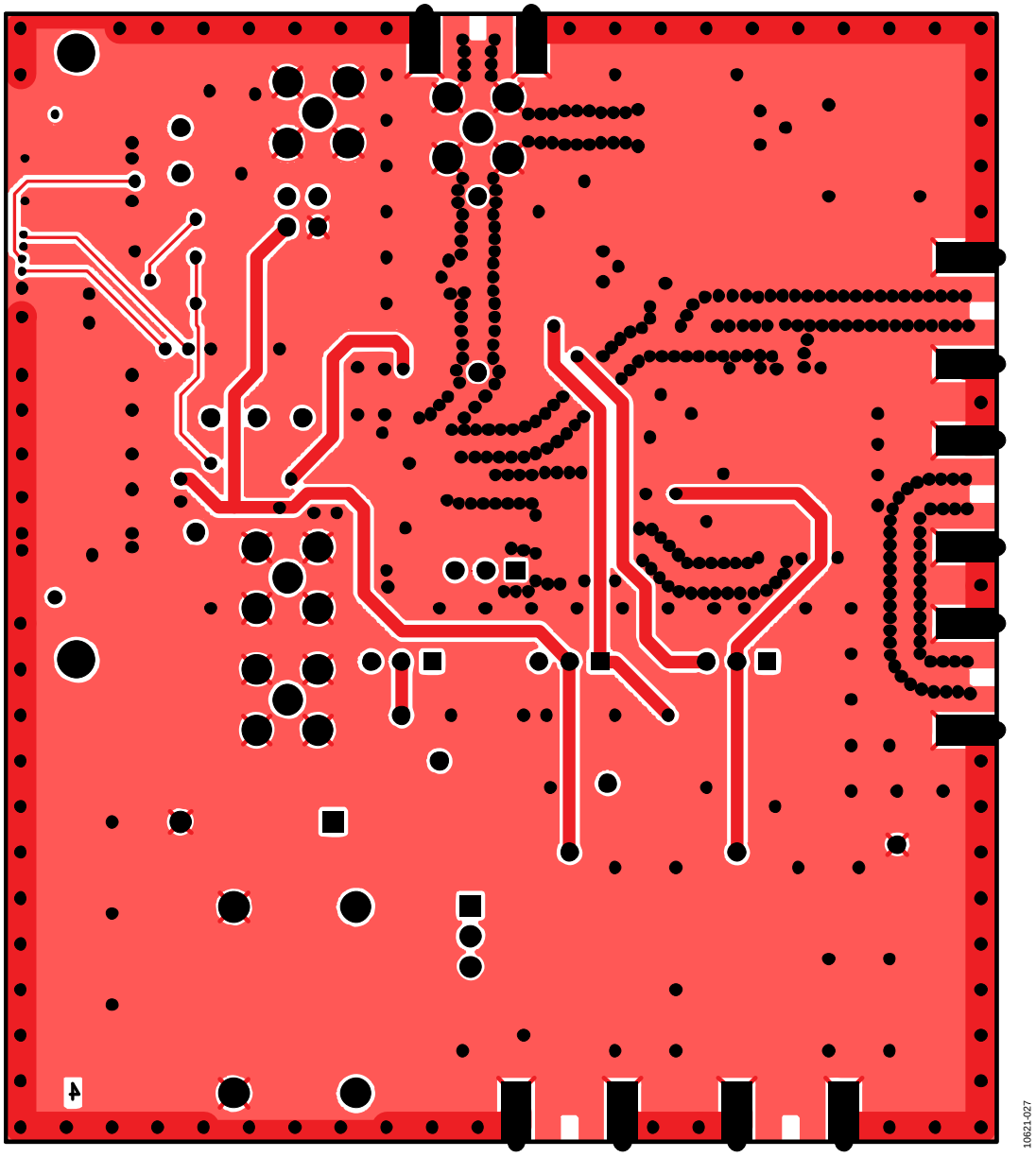

Figure 27. Layer 4 (Solder Side)

BILL OF MATERIALS

Table 2.

Reference Designator	Part Description	Manufacturer/Part No.
C1	Capacitor, 0805, 680 pF	PHYCOMP 2238 861 15681
C2	Capacitor, 0805, 10 nF	MURATA GRM2195C1H103JA01D
C3	Capacitor, 0805, 270 pF	PHYCOMP 2238 861 15271
C4, C6, C10	Capacitor, 0402, 0.1 µF, 16 V	AVX CM105X7R104K16AT
C5, C7, C9, C11, C13	Capacitor, 0603, 10 pF, 50 V, SMD	AVX 06035A100JAT2A
C8, C12	Capacitor, Case A, 22 µF, 6.3 V	AVX TAJA226K006R
C14, C15	Capacitor, 0603, 1 nF, 50 V	AVX 06035A102JAT2A
C16, C17, C18, C19	Capacitor, 0603, 100 pF, 50 V	AVX 06035A101JAT2A
C20, C23	Capacitor, Case A, 1 µF, 16 V	AVX TAJA105K016R
C21, C24	Capacitor, 0603, 10 nF, 50 V	AVX 06035C103JAT2A
C22, C25	Capacitor, Case A, 4.7 µF, 10 V	AVX TAJA475K010R
C26, C27	Capacitor, 0603, 10 nF, 50 V	Not inserted
D1	LED, green	OSRAM LGR971-Z
D2	Diode, DO41, 1 A, 50 V	Multicomp 1N4001
D3, D5	SD103C, 6.2 V	ON Semiconductor MBR0520LT1G
D4	LED, red	Avago HSMS-C170
J1	120-way connector, 0.6 mm pitch	Hirose FX8-120S-SV(21)
J2	Jack, SMA, SMA_EDGE	Johnson Components 142-0701-851
J3, J4, J10	JACK, SMA, receptacle straight PCB	Not inserted
J5, J6, J7, J8, J9	Jack, SMA, SMA_EDGE	Not inserted
J11	Jack, SMA, receptacle straight PCB	Pomona 72963
LK1, LK3, LK4, LK5	Jumper2\SIP3, 3-pin link	Harwin M20-9990345 and M7566-05
LK2	Jumper-2	Harwin M20-9990245 and M7566-05
GND	Black 4 mm banana socket	Deltron 571-0100-01
VSUPPLY	Red 4 mm banana socket	Deltron 571-0500-01
R1A	Resistor, 0805	User supplied
R1	Resistor, 0805, 2.4 kΩ	MULTICOMP MC 0.1W 0805 1% 2K4
R2	Resistor, 0805, 5.1 kΩ	MULTICOMP MC 0.1W 0805 1% 5K1
R3	Resistor, 0805, 5.1 kΩ, ±1%, 0.1 W	Multicomp MC 0.1 0805 1% 5K1
R4, R5, R6, R23, R29, R42	Resistor, 0603, 330 Ω	Multicomp MC 0.063W 0603 1% 330R
R7, R8, R9	Resistor, 0603, 18 Ω	Multicomp MC 0.063W 0603 1% 18R
R10	Resistor, 0603, 51 Ω	Multicomp MC 0.063W 0603 1% 51R
R11	Resistor, 0603 100 Ω	Multicomp MC 0.0625W 0402 1% 100R
R12, R13, R24, R25, R26	Resistor, 0603, 10 kΩ	Multicomp MC 0.063W 0603 1% 10K
R14, R16, R18, R28, R36	Resistor, 0603, 0 Ω	Multicomp MC 0.063W 0603 1% 0R
R15, R17, R22, R27, R32, R33, R37, R46	Resistor, 0603, 0 Ω	Not inserted
R19, R20	Resistor, 0603, 330 kΩ, ±1%, 0.063 W	Multicomp MC 0.063W 0603 1% 330K
R21	Resistor, 0603, 4.7 kΩ, ±1%, 0.063 W	Multicomp MC 0.063W 0603 1% 4K7
R30	Resistor, 0402	Not inserted
R31, R34	Resistor, RC31, 0402, 100 kΩ	YAGEO (Phycomp) RC0402JR-07100KL
S1	Switch, PCB, SPDT, 20 V	APEM TL36P0050
T1 to T14	Test point, PCB, red PK_100	Vero 20-313137
U1	ADF4157, 16-lead TSSOP	Analog Devices ADF4157BRUZ
U3	ADP3300, 5 V, 6-lead SOT-23	Analog Devices ADP3300ARTZ-5REEL7
U2	ADP3300, 3 V, 6-lead SOT-23	Analog Devices ADP3300ARTZ-3-RL7
U4	32k I^2C serial EEPROM, MSOP8	Microchip 24LC32A-I/MS
Y1	VCO V940ME03	Z-Communications V940ME03-LF
Y2	Low profile/temperature compensated crystal oscillator, OSC_TCXO, 10 W	Fox 801-BELF

RELATED LINKS

Resource	Description
ADF4157	Product Page: High Resolution 6 GHz Fractional-N Frequency Synthesizer
ADP3300	Product Page: High Accuracy anyCAP® 50 mA Low Dropout Linear Regulator
ADSP-BF527	Product Page: Low Power Blackfin Processor with Advanced Peripherals
SDP-S	Product Page: System Demonstration Platform-Serial (SDP-S)
SDP-B	Product Page: System Demonstration Platform-Blackfin (SDP-B)
UG-393	User Guide: Evaluation Board for the ADF4157 Fractional-N PLL Frequency Synthesizer
UG-291	User Guide: SDP-S Controller Board
UG-277	User Guide: SDP-B Controller Board

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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