Evaluation Board User Guide

EV-ADF4193SD1Z/EV-ADF4193SD2Z/EV-ADF4196SD1Z

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Evaluating the ADF4193 and ADF4196 Frequency Synthesizers for Phase-Locked Loops

FEATURES

- EV-ADF4193SD1Z board includes an ADF4193 synthesizer, loop filter, VCO, voltage regulators, and SDP interface
- EV-ADF4193SD2Z and EV-ADF4196SD1Z boards include an ADF4193 or ADF4196 synthesizer, voltage regulators, and SDP interface
- Accompanying software allows control of synthesizer functions from a PC (via an SDP interface)
- Externally powered by a 5 V to 9 V supply

EVALUATION KIT CONTENTS

- EV-ADF4193SD1Z, EV-ADF4193SD2Z, or EV-ADF4196SD1Z evaluation board
- CD with evaluation software

REQUIRED ADDITIONAL EQUIPMENT

- VCO (for EV-ADF4193SD2Z and EV-ADF4196SD1Z)
- Loop filter components (for EV-ADF4193SD2Z and EV-ADF4196SD1Z)
- Soldering equipment
- Spectrum analyzer
- Power supplies (9 V)
- Windows-based PC with USB port for evaluation software

REQUIRED DOCUMENTS

- ADF4193 data sheet
- ADF4196 data sheet
- EV-ADF4193SD1Z/EV-ADF4193SD2Z/EV-ADF4196SD1Z user guide

REQUIRED SOFTWARE

- Analog Devices ADF4193-6 evaluation software, Version 6.0.7 or higher (included on the CD in the evaluation board kit or available for download at www.analog.com)

GENERAL DESCRIPTION

The EV-ADF4193SD1Z/EV-ADF4193SD2Z/EV-ADF4196SD1Z evaluate the performance of the ADF4193 or ADF4196 frequency synthesizer for phase-locked loops (PLL). A photograph of the evaluation board is shown in Figure 1. The evaluation board includes the ADF4196 synthesizer, an SDP connector, SMA connectors, and power supply connectors. There are also footprints for loop filter components and a voltage controlled oscillator (VCO); if used, these components must be soldered to the board to complete the loop. The board connects to a PC via an SDP adapter board.

In addition, the evaluation kit contains Windows®-based software to allow easy programming of the synthesizer.

EVALUATION BOARD PHOTOGRAPH

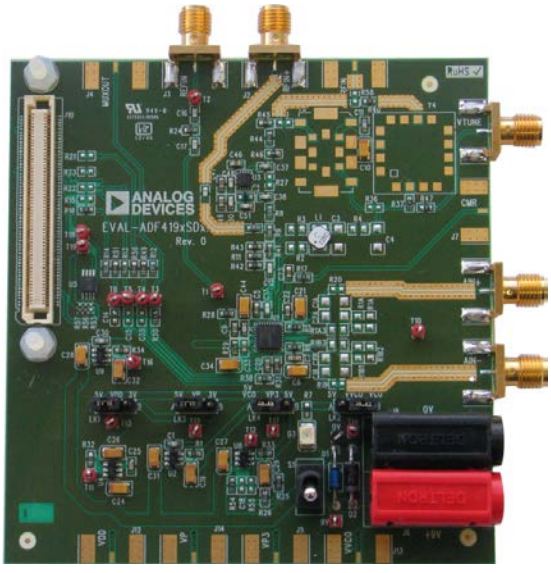

Figure 1. Photograph of the EV-ADF4196SD1Z

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT WARNING AND LEGAL TERMS AND CONDITIONS.

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REVISION HISTORY

3/13—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

EV-ADF4193SD1Z

The EV-ADF4193SD1Z board includes a VCO, loop filter components, power regulators, and an ADF4193 synthesizer.

To operate this board, it is necessary to

1. Supply a reference signal.
2. Power the board.
3. Program the board using the provided software.

EV-ADF4193SD2Z and EV-ADF4196SD1Z

The EV-ADF4193SD2Z and EV-ADF4196SD1Z boards include power regulators and an ADF4193 or ADF4196 synthesizer.

To operate these boards, it is necessary to

1. Solder the loop filter components to the board.
2. Connect/solder a VCO to the board.
3. Supply a reference signal.
4. Power the board.
5. Program the board using the provided software.

POWER SUPPLIES

The evaluation board is powered by a 5 V to 9 V power supply connected to the red and black banana connectors. Connect the red connector to a 5 V to 9 V power supply, and connect the black connector to ground.

VCO

The EV-ADF4193SD1Z/EV-ADF4193SD2Z/EV-ADF4196SD1Z can accept three industry-standard VCOs with different footprints. These VCOs are labeled Y4 and Y3 (Y3 can accept two different types of VCOs).

Table 1. VCOs[1]

VCO	R40	R37	R44	R37
Y4	0 Ω	0 Ω	DNI	DNI
Y3	DNI	DNI	0 Ω	0 Ω

[1] DNI = do not insert.

Alternatively, an external VCO can be connected at the VTUNE SMA, but you must ensure that R4 = R47 = 0 Ω. The output signal of the VCO should be fed back to the RFIN+ SMA.

LOOP FILTER

See the ADF4193-TN-001 technical note, *ADF4193 PLL Loop Filter Design Using ADISimPLL*, for guidance on designing a loop filter using ADIsimPLL.

OUTPUT SIGNALS

When an on-board VCO is used, the output signal is routed to J2. When an external VCO is used, connect the feedback signal to J2.

JUMPERS

Table 2 describes the various jumper options.

Table 2. Jumpers

Jumper	Supplies	Setting	Description
LK1	ADF4193/ADF4196 V_{DD} supply	5 V	From 5 V regulator, U8, ADP3331ARTZ-REEL7
		3 V	From 3 V regulator, U4, ADP3330ARTZ-3-RL7.
		None	Connect supply to T13.
LK2	VCO supply	5 V	From 5 V regulator, U8, ADP3331ARTZ-REEL7.
		VCO	From 5 V regulator, U2, ADP3330ARTZ-5-RL7.
		None	Connect supply to T14.
LK3	V_P supply	5 V	From 5 V regulator, U8, ADP3331ARTZ-REEL7.
		3 V	From 3 V regulator, U4, ADP3330ARTZ-3-RL7.
		None	Connect supply to T15.
LK4	V_{P3} supply	5 V	From 5 V regulator, U8, ADP3331ARTZ-REEL7.
		VCO	From 5 V regulator, U2, ADP3330ARTZ-5-RL7.
		None	Connect supply to T17.

EVALUATION SETUP

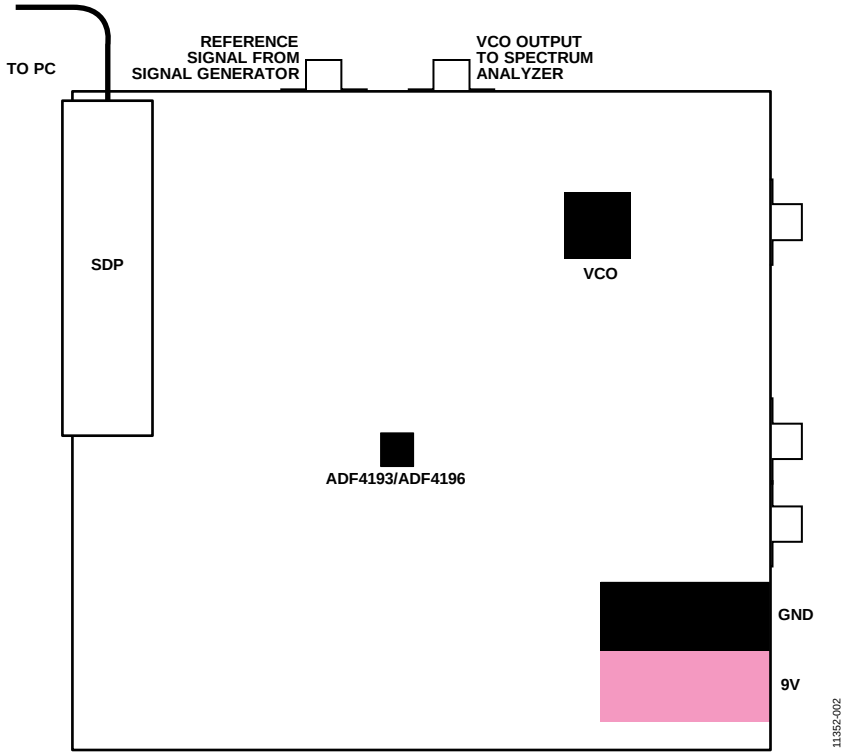

Figure 2. Evaluation Setup Block Diagram, Using On-Board VCO

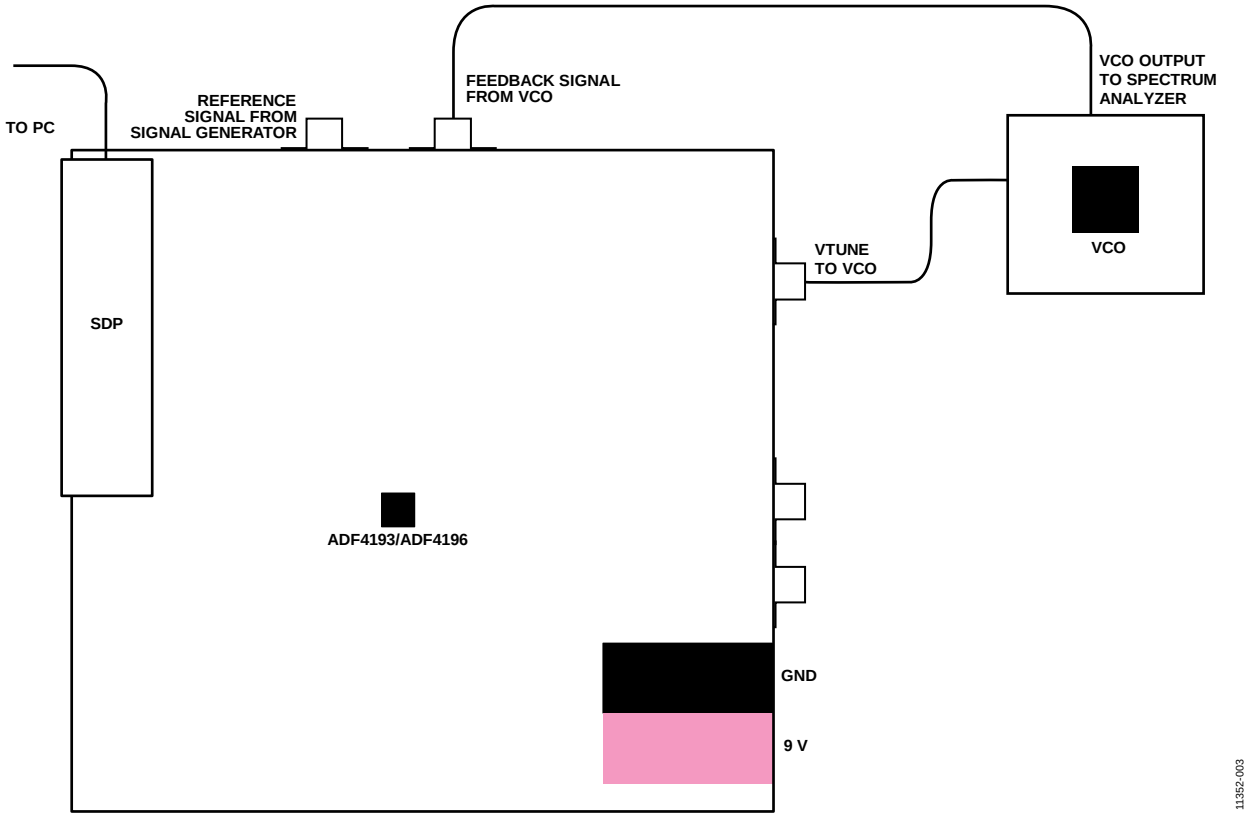

Figure 3. Evaluation Setup Block Diagram, Using External VCO

GETTING STARTED

INSTALLING THE SOFTWARE

For the software installation procedure, see UG-476, *PLL Software Installation Guide*. The control software for the EV-ADF4193SD1Z, EV-ADF4193SD2Z, and EV-ADF4196SD1Z is provided on the CD included in the evaluation board kit.

CONFIGURING AND SETTING UP THE BOARD

1. Set up the circuit as shown in Figure 2 or Figure 3.
2. Run the ADF4193-6 software.
3. Select **ADF4193** or **ADF4196** and **SDP board (black)**, and then click **Connect** (see Figure 4).
4. Click the **Main Controls** tab to view the main controls (see Figure 5). The default values are set to lock a VCO at 1880 MHz.
5. After initial power-up, the ADF4193 or ADF4196 must be initialized. To do this, click **Run Initialization Sequence**.
6. On the spectrum analyzer, confirm that the output signal is locked at 1880 MHz.

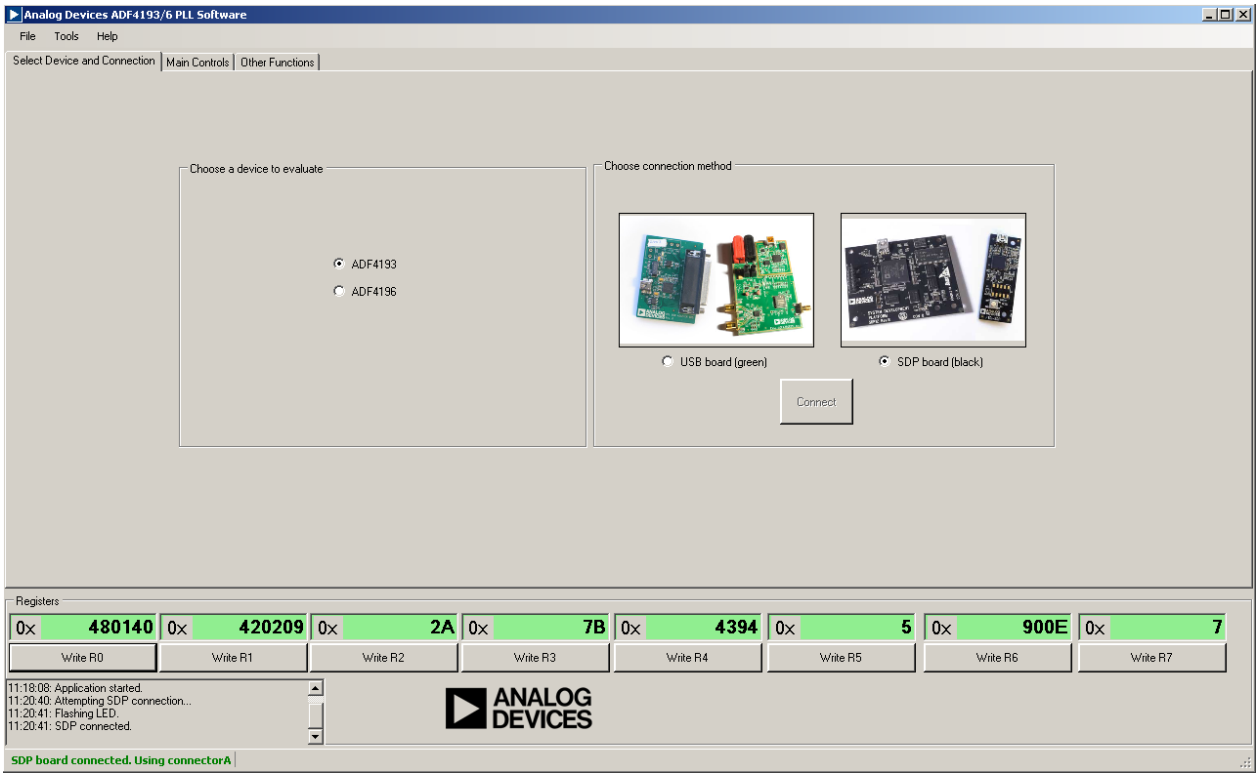

Figure 4. Software—Device Selection

USING THE SOFTWARE—MAIN CONTROLS

Use the **Main Controls** tab to select the RF and PLL settings. In the **RF Settings** area, set the **RF VCO Output Frequency** to the desired VCO output. Set the **Reference Frequency** to be the same as the applied reference signal. The PFD frequency is calculated from the reference frequency, the R-counter, the reference doubler, and the reference-divide-by-2. Ensure that the value in the **PFD Frequency** box matches the value specified in the loop filter design.

In the **PLL Settings** area, the **Muxout** drop-down box allows you to choose the signal that is connected to the output of the MUX_{OUT} pin.

In the **Registers** area near the bottom of the window, the values to be written to each register are displayed. If the background of a text box is green, the value displayed is different from the value actually on the device. Click **Write Rx** (where x = 0 to 7) to write the value displayed to the device.

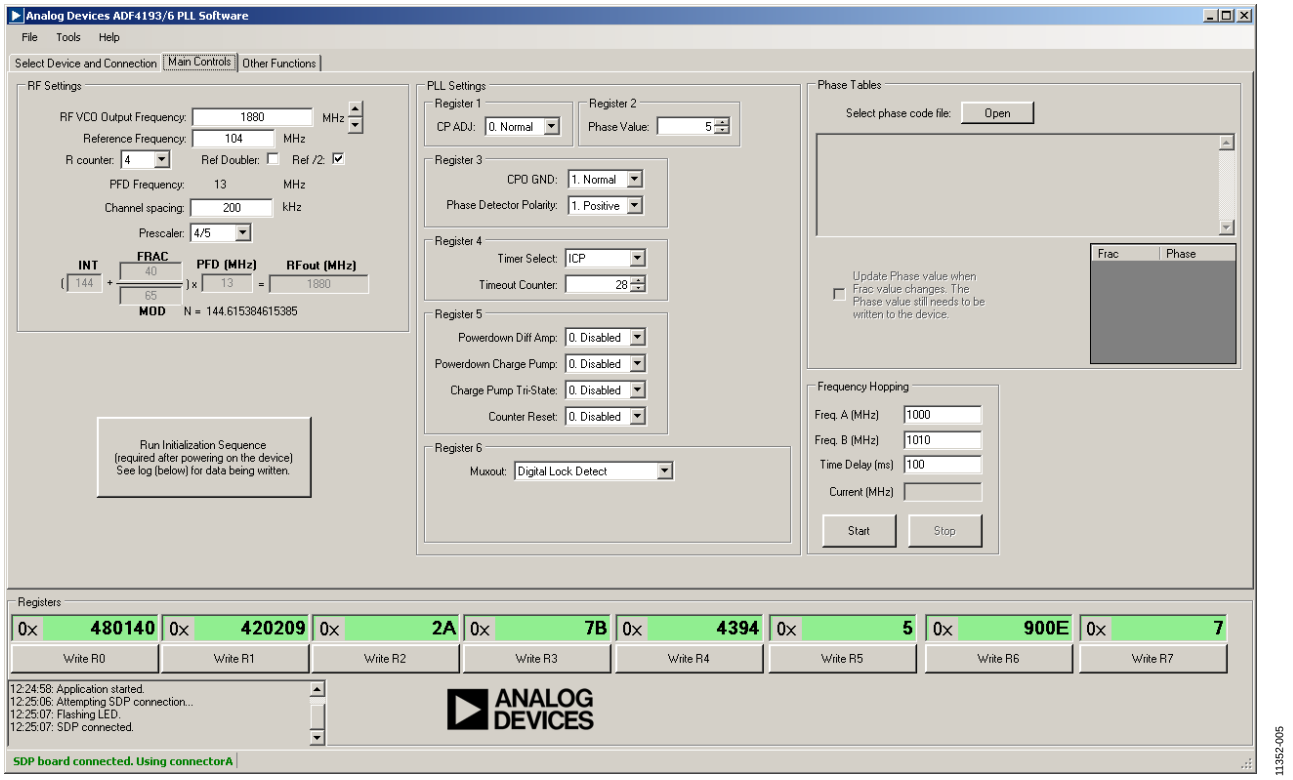

Figure 5. Software—Main Controls

USING THE SOFTWARE—PHASE TABLES

To achieve phase locking times of less than 20 µs, you must choose a value of phase corresponding to the value of FRAC for the ADF4193 or ADF4196

Use the **Phase Tables** area of the **Main Controls** tab to allow the software to automatically update to the optimum value of phase every time the value of FRAC changes.

After the software is installed, several phase code files are loaded into the **Phase Tables** directory within the installation directory. For example, the files described in Table 3 are loaded to **C:\Program Files\Analog Devices\ADF4193-6\Phase Tables**.

Table 3. Files Loaded into Phase Tables Directory for ADF4193-6

File Name	Description
gsm1800tx_phase_codes.txt	GSM 1800 Tx systems
gsm1800rx_phase_codes.txt	GSM 1800 Rx systems
gsm900tx_phase_codes.txt	GSM 900 Tx systems
gsm900rx_phase_codes.txt	GSM 900 Rx systems
26M_60K_phase_codes.txt	GSM 1800 Tx systems designed with a PFD frequency of 26 MHz

To use a phase code file, click **Open** in the **Phase Tables** area of the **Main Controls** tab, and then choose the required file. When the codes are loaded, select the **Update Phase value when Frac phase changes. The Phase value still needs to be written by the device** check box.

EVALUATION BOARD SCHEMATICS

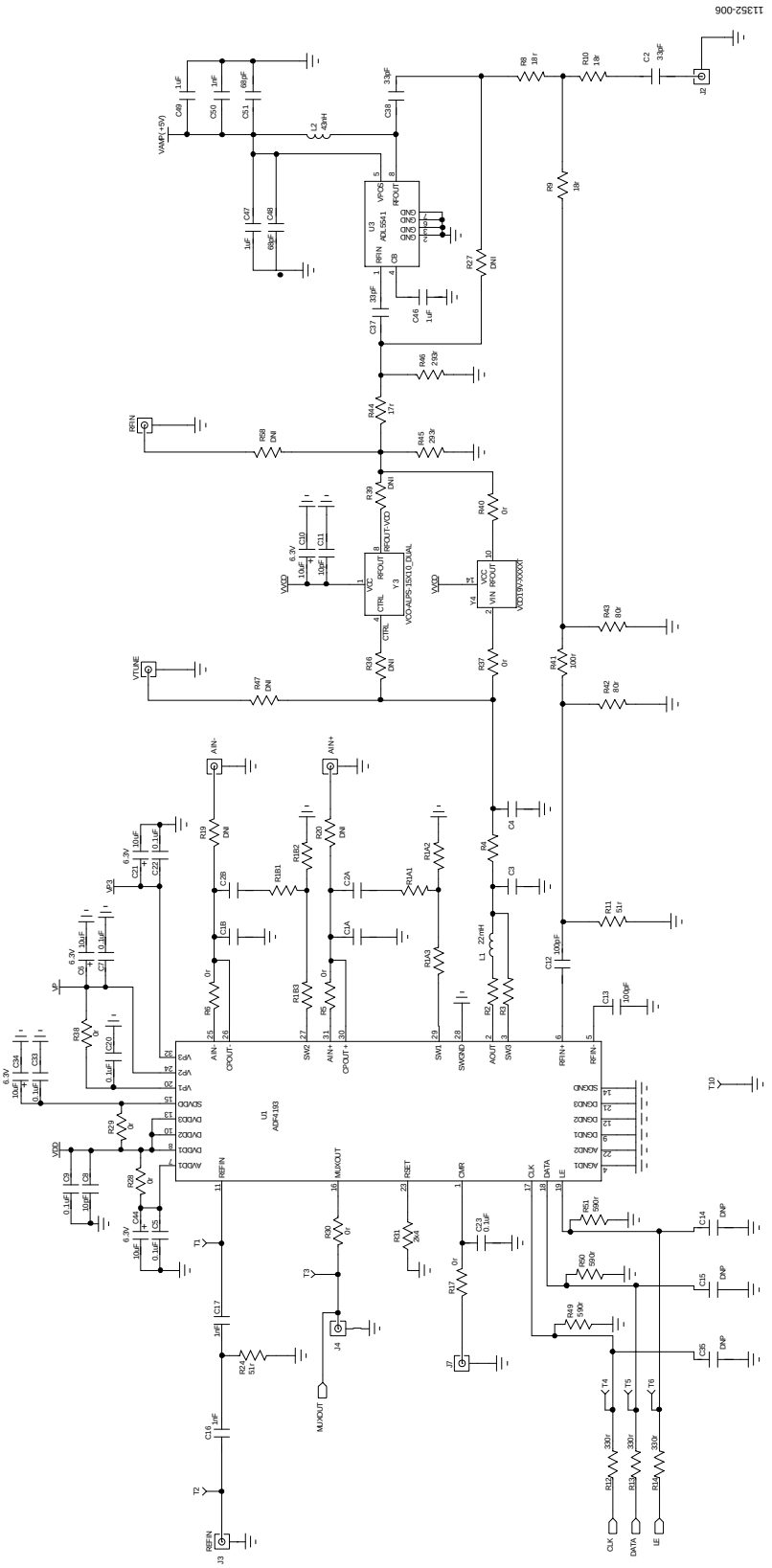

Figure 6. Evaluation Board Schematic (1 of 3)

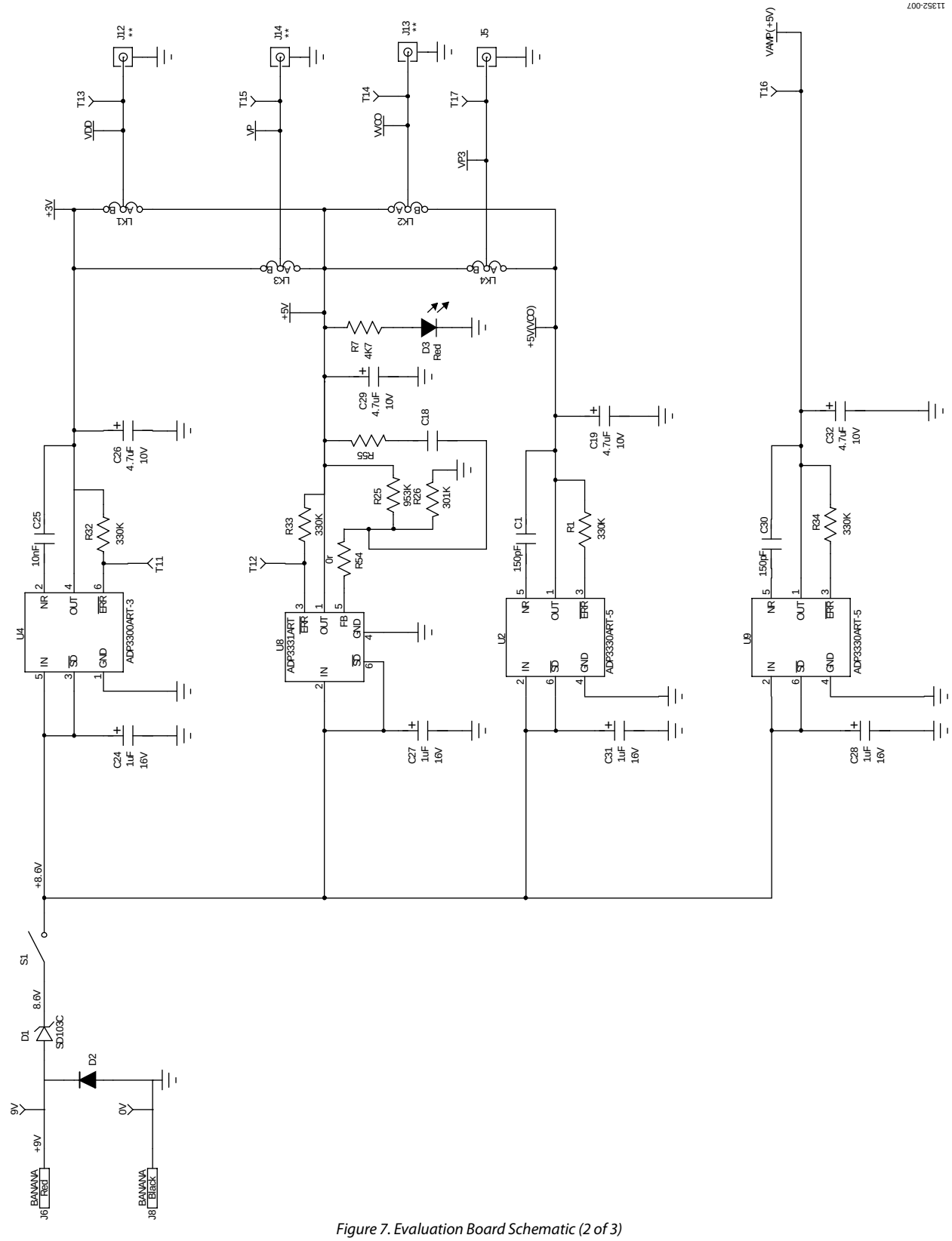

Figure 7. Evaluation Board Schematic (2 of 3)

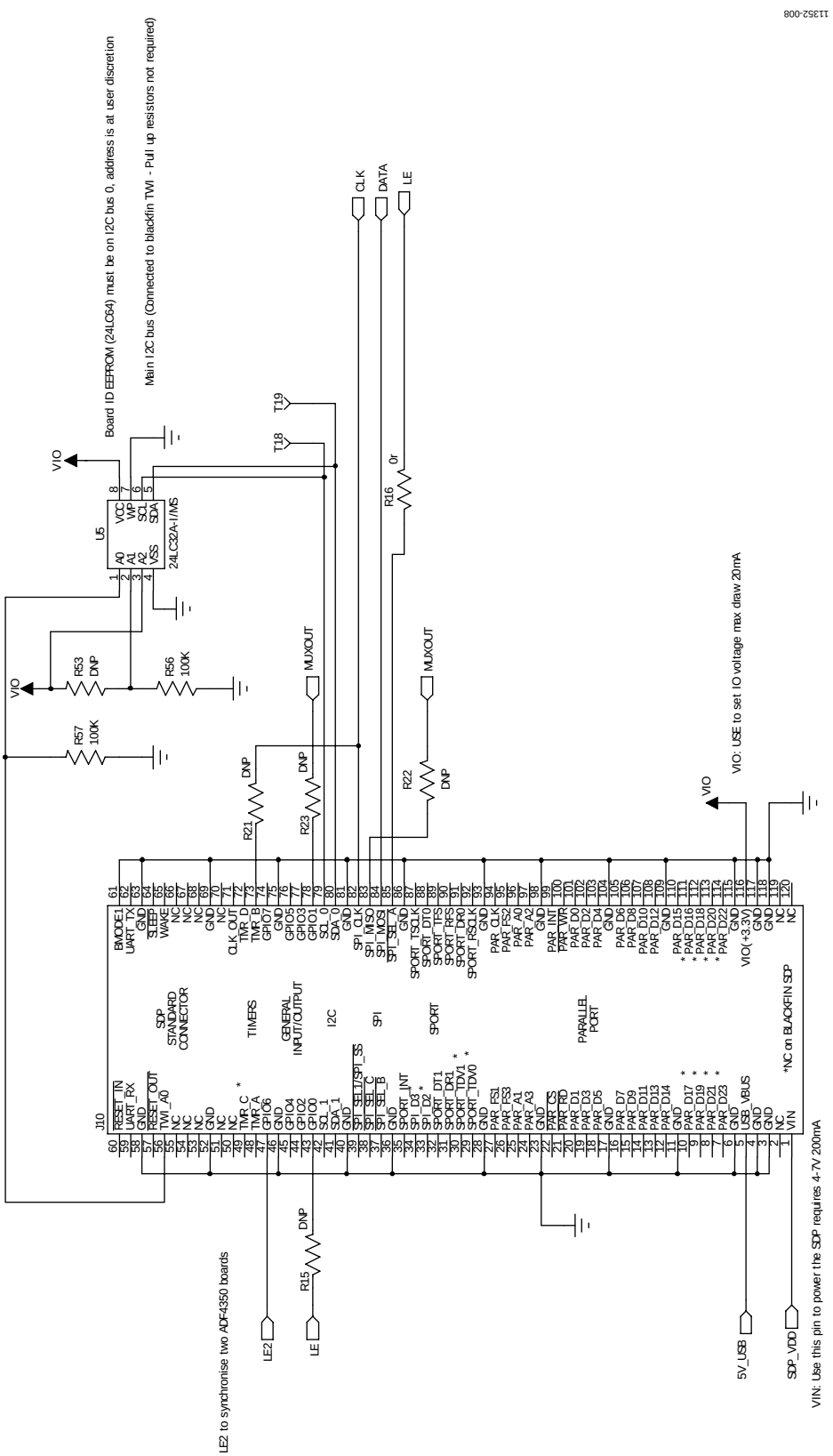

Figure 8. Evaluation Board Schematic (3 of 3)

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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