Microwave Wideband Synthesizer with Integrated VCO

Data Sheet

ADF4355-3

FEATURES

- RF output frequency range: 51.5625 MHz to 6600 MHz
- Fractional-N synthesizer and integer-N synthesizer
- High resolution 38-bit modulus
- Low phase noise, voltage controlled oscillator (VCO)
- Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
- All power supplies: 3.3 V
- Logic compatibility: 1.8 V
- Programmable dual modulus prescaler of 4/5 or 8/9
- Programmable output power level
- RF output mute function
- 3-wire serial interface
- Analog and digital lock detect

APPLICATIONS

- Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)
- Point to point/point to multipoint microwave links
- Satellites/VSATs
- Test equipment/instrumentation
- Clock generation

GENERAL DESCRIPTION

The ADF4355-3 allows the implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference frequency. A series of frequency dividers at the output provide operation from 51.5625 MHz to 6600 MHz.

The ADF4355-3 has an integrated VCO with a fundamental output frequency ranging from 3300 MHz to 6600 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allow the user to generate RF output frequencies as low as 51.5625 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin- and software-controllable.

Control of all on-chip registers is through a simple 3-wire interface. The ADF4355-3 operates with analog, digital, charge pump, and VCO power supplies ranging from 3.1515 V to 3.4485 V. The ADF4355-3 also contains hardware and software power-down modes.

FUNCTIONAL BLOCK DIAGRAM

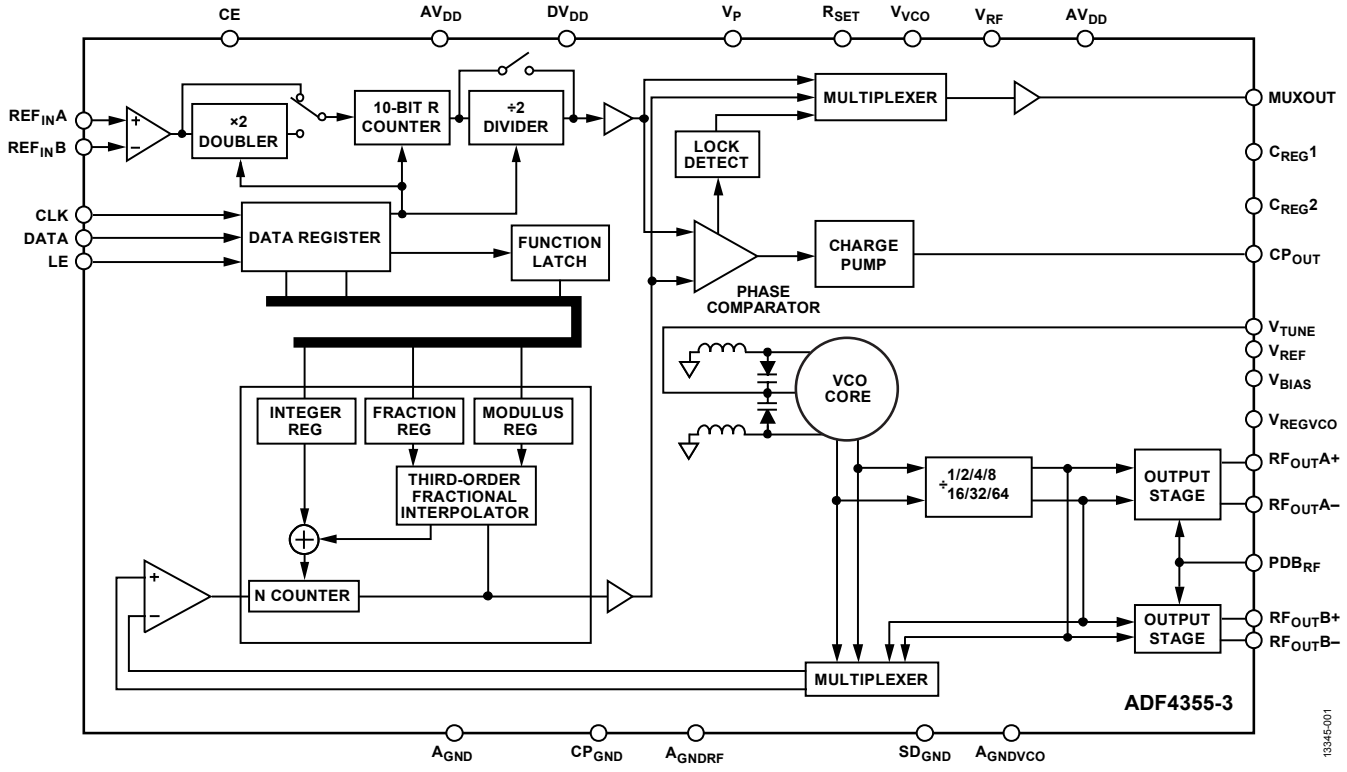

Figure 1.

Rev. B Document Feedback

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7/2015—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = V_{RF} = V_P = V_{VCO} = V_{REGVCO} = 3.3 V ± 4.5%, A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$REF_{IN}A/REF_{IN}B$ CHARACTERISTICS						
Input Frequency	REF_{IN}					For f < 10 MHz, ensure that the slew rate > 21 V/µs
Single-Ended Mode		10		250	MHz	
Differential Mode		10		600	MHz	
Doubler Enabled				100	MHz	Doubler is set in Register 4, Bit DB26
Input Sensitivity						
Single-Ended Mode		0.4		AV_{DD}	V p-p	$REF_{IN}A$ biased at $AV_{DD}/2$; ac coupling ensures $AV_{DD}/2$ bias
Differential Mode		0.4		1.8	V p-p	LVDS and LVPECL compatible, $REF_{IN}A/REF_{IN}B$ biased at 2.1 V; ac coupling ensures 2.1 V bias
Input Capacitance						
Single-Ended Mode			6.9		pF	
Differential Mode			1.4		pF	
Input Current				±60	µA	Single-ended reference programmed
				±250	µA	Differential reference programmed
Phase Detector Frequency				125	MHz	
CHARGE PUMP (CP)						
Charge Pump Current, Sink/Source	I_{CP}					R_{SET} = 5.1 kΩ
High			4.8		mA	
Low			0.3		mA	
R_{SET} Range			5.1		kΩ	Fixed
Current Matching			3		%	0.5 V ≤ V_{CP}[1] ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}[1]			3		%	0.5 V ≤ V_{CP}[1] ≤ V_P − 0.5 V
I_{CP} vs. Temperature			1.5		%	V_{CP}[1] = 2.5 V
LOGIC INPUTS						1.8 V and 3.3 V compatible
Input Voltage						
High	V_{INH}	1.5		DV_{DD}	V	
Low	V_{INL}			0.6	V	
Input Current	I_{INH}/I_{INL}			±1	µA	
Input Capacitance	C_{IN}		3.0		pF	
LOGIC OUTPUTS						
Output Voltage						
High	V_{OH}	DV_{DD} − 0.4			V	3.3 V output selected
		1.5	1.8		V	1.8 V output selected
Low	V_{OL}			0.4	V	I_{OL}[2] = 500 µA
Output High Current	I_{OH}			500	µA	
POWER SUPPLIES						
Analog Power	AV_{DD}	3.1515	3.3	3.4485	V	3.3 V ± 4.5%
Digital Power, RF Supply, Charge Pump, and VCO Supply Voltage	DV_{DD}, V_{RF}, V_P, V_{VCO}		AV_{DD}			Voltages must equal AV_{DD}
Charge Pump Supply Current	I_P		3.1	5	mA	
DI_{DD} + AI_{DD}[3]			66	75	mA	Supply current drawn by DV_{DD} plus supply current drawn by AV_{DD}
Output Dividers						See Table 6
VCO Supply Current	I_{VCO}		52	70	mA	
$RF_{OUT}A±/RF_{OUT}B±$ Supply Current	$I_{RF_{OUT}x±}$		13/19/25/31	20/27/34/41	mA	RF output stage is programmable; $RF_{OUT}B+/RF_{OUT}B–$ powered off
Low Power Sleep Mode			1500		µA	Hardware power-down
			1950		µA	Software power-down

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RF OUTPUT CHARACTERISTICS						
VCO Frequency Range		3300		6600	MHz	Fundamental VCO range
RF Output Frequency	f_{RF}	51.5625		6600	MHz	
VCO Sensitivity	K_V		63		MHz/V	
Frequency Pushing (Open-Loop)			22		MHz/V	
Frequency Pulling (Open-Loop)			0.54		MHz	Voltage standing wave ratio (VSWR) = 2:1
Harmonic Content						
Second			−27		dBc	Fundamental VCO output ($RF_{OUT}A+$)
			−22		dBc	Divided VCO output ($RF_{OUT}A+$)
Third			−20		dBc	Fundamental VCO output ($RF_{OUT}A+$)
			−12		dBc	Divided VCO output ($RF_{OUT}A+$)
RF Output Power[4]			8		dBm	$RF_{OUT}A+$ = 1 GHz. 7.5 nH inductor to V_{RF}
			3		dBm	$RF_{OUT}A+/RF_{OUT}A-$ = 4.4 GHz. 7.5 nH inductor to V_{RF}
RF Output Power Variation			±1		dB	$RF_{OUT}A+/RF_{OUT}A-$ = 4.4 GHz
Over Frequency			±3		dB	$RF_{OUT}A+/RF_{OUT}A-$ = 1 GHz to 4.4 GHz
Level of Signal with Output Disabled			−60		dBm	$RF_{OUT}A+/RF_{OUT}A-$ = 1 GHz, VCO = 4 GHz
			−30		dBm	$RF_{OUT}A+/RF_{OUT}A-$ = 4.4 GHz, VCO = 4.4 GHz
NOISE CHARACTERISTICS						
Fundamental VCO Phase Noise Performance						VCO noise in open-loop conditions
3.3 GHz Carrier			−113		dBc/Hz	100 kHz offset from 3.3 GHz carrier
			−133		dBc/Hz	800 kHz offset from 3.3 GHz carrier
			−135		dBc/Hz	1 MHz offset from 3.3 GHz carrier
			−153		dBc/Hz	10 MHz offset from 3.3 GHz carrier
5.0 GHz Carrier			−110		dBc/Hz	100 kHz offset from 5.0 GHz carrier
			−130		dBc/Hz	800 kHz offset from 5.0 GHz carrier
			−132		dBc/Hz	1 MHz offset from 5.0 GHz carrier
			−151		dBc/Hz	10 MHz offset from 5.0 GHz carrier
6.6 GHz Carrier			−107		dBc/Hz	100 kHz offset from 6.6 GHz carrier
			−127		dBc/Hz	800 kHz offset from 6.6 GHz carrier
			−129		dBc/Hz	1 MHz offset from 6.6 GHz carrier
			−148		dBc/Hz	10 MHz offset from 6.6 GHz carrier
Normalized In-Band Phase Noise Floor						
Fractional Channel[5]			−221		dBc/Hz	
Integer Channel[6]			−223		dBc/Hz	
Normalized 1/f Noise[7]	PN_{1_f}		−116		dBc/Hz	10 kHz offset, normalized to 1 GHz
Integrated RMS Jitter			200		fs	
Spurious Signals due to Phase Frequency Detector (PFD) Frequency			−85		dBc	

[1] V_{CP} is the voltage at the CP_{OUT} pin.
[2] I_{OL} is the output low current.
[3] T_A = 25°C; AV_{DD} = DV_{DD} = V_{RF} = V_{VCO} = V_P = 3.3 V; prescaler = 4/5; $f_{REF_{IN}}$ = 122.88 MHz; f_{PFD} = 61.44 MHz; and f_{RF} = 1650 MHz.
[4] RF output power using the EV-ADF4355-3SD1Z evaluation board measured into a spectrum analyzer, with board and cable losses de-embedded. Unused RF output pins are terminated in 50 Ω.
[5] Use this figure to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −221 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the fractional channel.
[6] Use this figure to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −223 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the integer channel.
[7] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by PN = P_{1_f} + 10log(10 kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL™ design tool.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = V_{RF} = V_P = V_{VCO} = 3.3 V ± 4.5%, A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Write Timing

Parameter	Limit	Unit	Description
f_{CLK}	50	MHz max	SPI CLK frequency
t_1	10	ns min	LE setup time
t_2	5	ns min	DATA to CLK setup time
t_3	5	ns min	DATA to CLK hold time
t_4	10	ns min	CLK high duration
t_5	10	ns min	CLK low duration
t_6	5	ns min	CLK to LE setup time
t_7	20 or (2/f_{PFD}), whichever is longer	ns min	LE pulse width

Write Timing Diagram

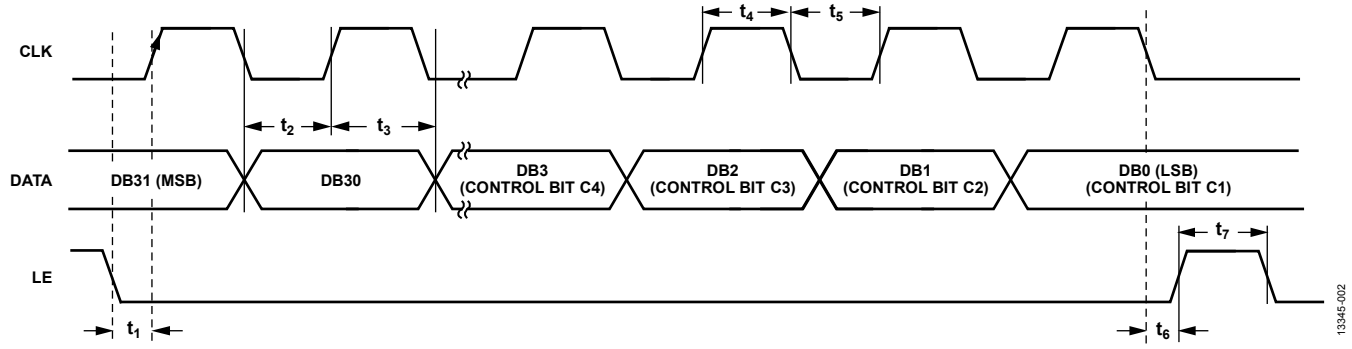

Figure 2. Write Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter[1]	Rating
V_{RF}, DV_{DD}, AV_{DD} to GND	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P, V_{VCO}, V_{REGVCO} to GND	−0.3 V to +3.6 V
CP_{OUT} to GND[1]	−0.3 V to V_P + 0.3 V
Digital Input/Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Analog Input/Output Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
$REF_{IN}A$, $REF_{IN}B$ to GND	−0.3 V to AV_{DD} + 0.3 V
$REF_{IN}A$ to $REF_{IN}B$	±2.1 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
θ_{JA}, Thermal Impedance Pad Soldered to GND	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Electrostatic Discharge (ESD)	
Charged Device Model	500 V
Human Body Model	2500 V

[1] GND = A_{GND} = SD_{GND} = A_{GNDRF} = A_{GNDVCO} = CP_{GND} = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The ADF4355-3 is a high performance RF integrated circuit with an ESD rating of 2500 V and is ESD sensitive. Take proper precautions for handling and assembly.

TRANSISTOR COUNT

The transistor count for the ADF4355-3 is 103,665 (CMOS) and 3214 (bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

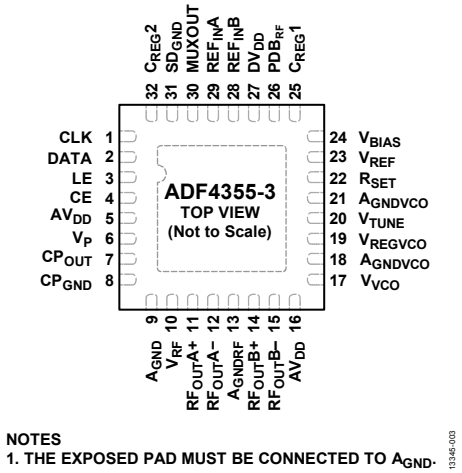

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
2	DATA	Serial Data Input. The serial data is loaded most significant bit (MSB) first with the four least significant bits (LSBs) as the control bits. This input is a high impedance CMOS input.
3	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the four LSBs.
4	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device, depending on the status of the power-down bits.
5, 16	AV_{DD}	Analog Power Supplies. These pins range from 3.1515 V to 3.4485 V. Connect decoupling capacitors to the analog ground plane as close to these pins as possible. AV_{DD} must have the same value as DV_{DD}.
6	V_P	Charge Pump Power Supply. V_P must have the same value as V_{VCO}. Connect decoupling capacitors to the ground plane as close to this pin as possible.
7	CP_{OUT}	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to V_{TUNE} to drive the internal VCO.
8	CP_{GND}	Charge Pump Ground. This output is the ground return pin for CP_{OUT}.
9	A_{GND}	Analog Ground. Ground return pin for AV_{DD}.
10	V_{RF}	Power Supply for the RF Output. Connect decoupling capacitors to the analog ground plane as close to this pin as possible. V_{RF} must have the same value as AV_{DD}. For optimum spurious performance, V_{RF} and DV_{DD} must originate from different regulators.
11	$RF_{OUT}A+$	VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
12	$RF_{OUT}A–$	Complementary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
13	A_{GNDRF}	RF Output Stage Ground. This pin is the ground return for the RF output stage.
14	$RF_{OUT}B+$	Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
15	$RF_{OUT}B–$	Complementary Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
17	V_{VCO}	Power Supply for the VCO. The voltage on this pin ranges from 3.1515 V to 3.4485 V. Connect decoupling capacitors to the analog ground plane as close to this pin as possible.
18, 21	A_{GNDVCO}	VCO Ground. This pin is the ground return path for the VCO.
19	V_{REGVCO}	VCO Compensation Node. Connect decoupling capacitors to the ground plane as close to this pin as possible. Connect this pin directly to V_{VCO}.
20	V_{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP_{OUT} output voltage. The capacitance at this pin (V_{TUNE} input capacitance) is 7 pF.

Pin No.	Mnemonic	Description
22	R_{SET}	Bias Current Resistor. Connecting a resistor between this pin and ground sets the charge pump output current.
23	V_{REF}	Internal Compensation Node. V_{REF} is dc biased at half of the tuning range. Connect decoupling capacitors to the ground plane as close to this pin as possible. The recommended capacitor values are 10 pF, 1 nF, and 4.7 µF.
24	V_{BIAS}	Reference Voltage. Connect decoupling capacitors to the ground plane as close to this pin as possible. The recommended capacitor values are 10 pF, 1 nF, and 1 µF.
25, 32	$C_{REG}1$, $C_{REG}2$	Outputs from the LDO Regulator. Pin 25 and Pin 32 are the supply voltages to the digital circuits, and have a nominal voltage of 1.8 V. Decoupling capacitors of 100 nF connected to A_{GND} are required for these pins.
26	PDB_{RF}	RF Power-Down. A logic low on this pin mutes the RF outputs. This mute function is also software-controllable.
27	DV_{DD}	Digital Power Supply. This pin must be at the same voltage as AV_{DD}. Place decoupling capacitors to the ground plane as close to this pin as possible. For optimum spurious performance, V_{RF} and DV_{DD} must originate from different regulators.
28	$REF_{IN}B$	Complementary Reference Input. If unused, ac-couple this pin to A_{GND}.
29	$REF_{IN}A$	Reference Input.
30	MUXOUT	Multiplexer Output. The multiplexer output allows the digital lock detect, the analog lock detect, scaled RF, or the scaled reference frequency to be externally accessible.
31	SD_{GND}	Digital Σ-Δ Modulator Ground. Pin 31 is the ground return path for the Σ-Δ modulator.
	EP	Exposed Pad. The exposed pad must be connected to A_{GND}.

TYPICAL PERFORMANCE CHARACTERISTICS

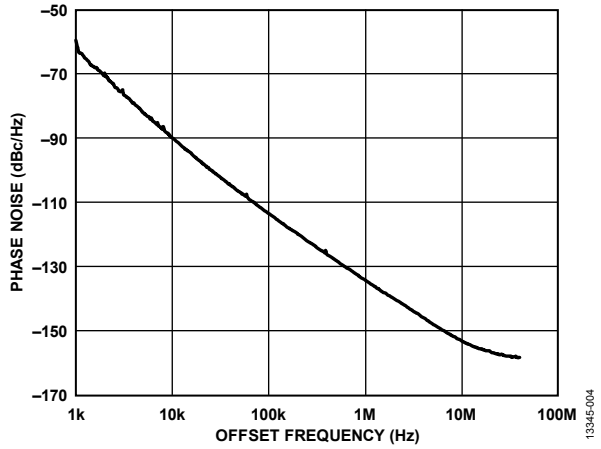

Figure 4. Open-Loop VCO Phase Noise, 3.3 GHz

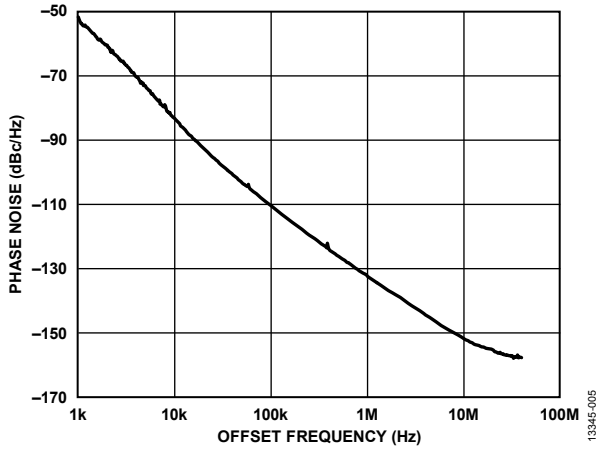

Figure 5. Open-Loop VCO Phase Noise, 5.0 GHz

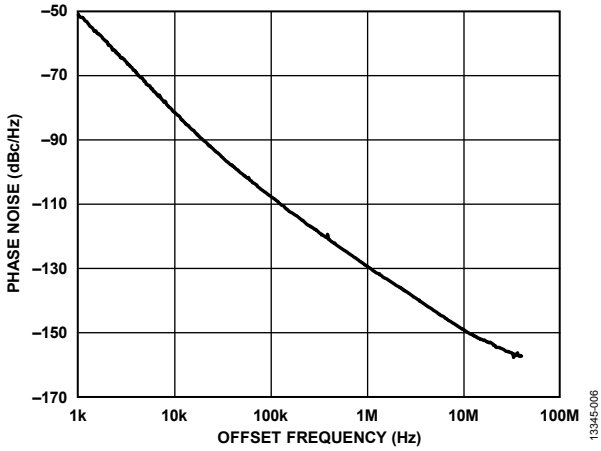

Figure 6. Open-Loop VCO Phase Noise, 6.6 GHz

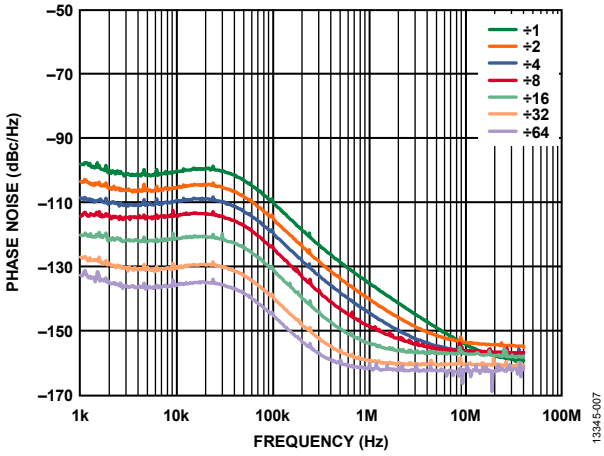

Figure 7. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Dividers, VCO = 3.3 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 35 kHz

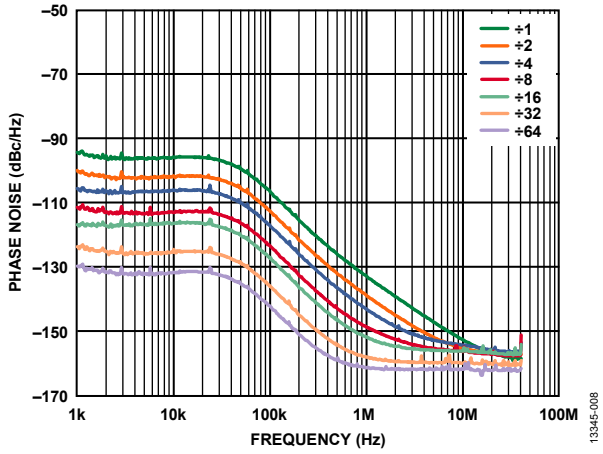

Figure 8. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Dividers, VCO = 5.0 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 35 kHz

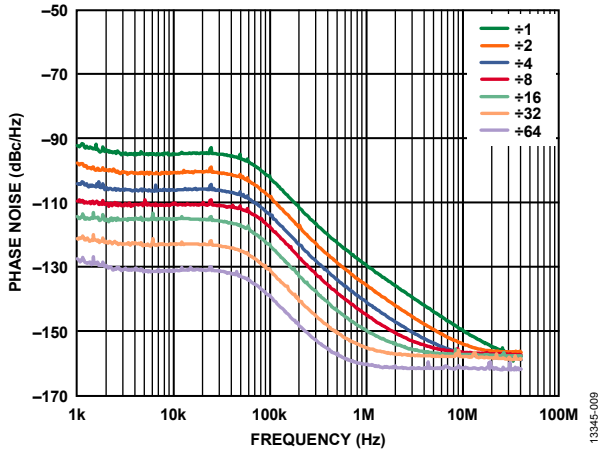

Figure 9. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Dividers, VCO = 6.6 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 35 kHz

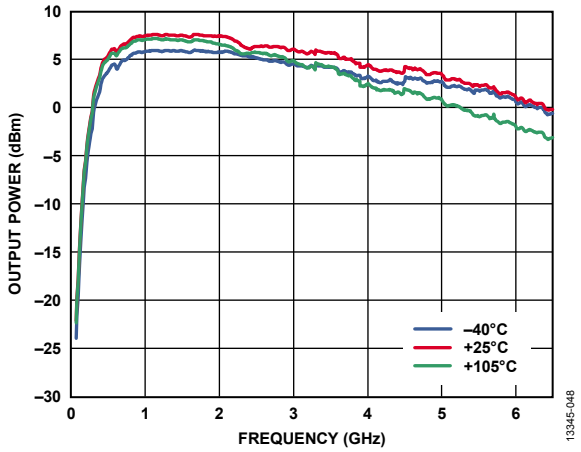

Figure 10. Output Power vs. Frequency, $RF_{OUT}A+/RF_{OUT}A-$ (7.5 nH Inductors, 10 pF Bypass Capacitors, Board Losses De-Embedded)

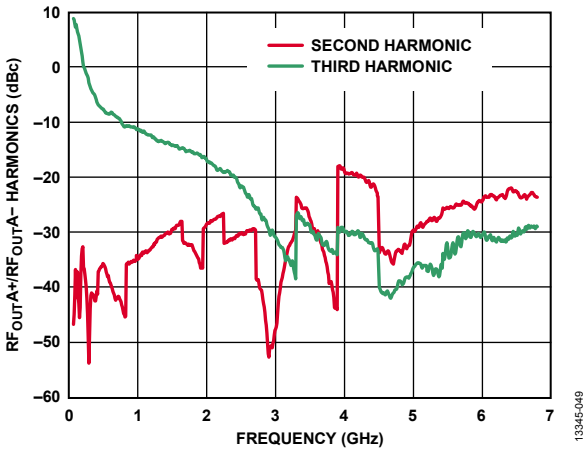

Figure 11. $RF_{OUT}A+/RF_{OUT}A-$ Harmonics vs. Frequency (7.5 nH Inductors, 10 pF Bypass Capacitors, Board Losses De-Embedded)

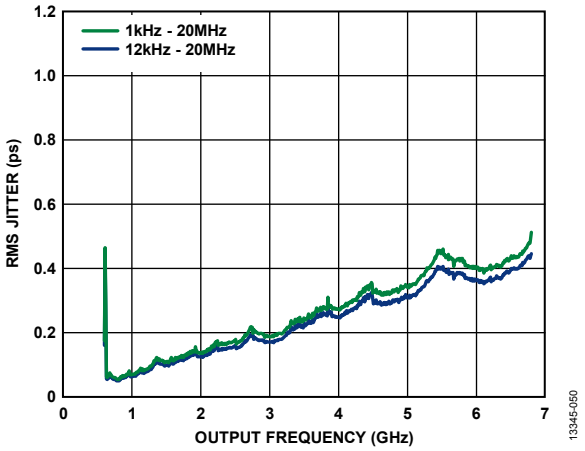

Figure 12. RMS Jitter vs. Output Frequency, f_{PFD} = 61.44 MHz, Loop Filter = 35 kHz

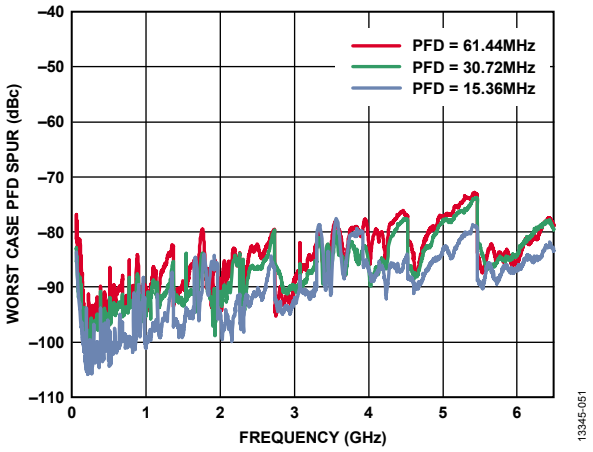

Figure 13. Worst Case PFD Spur vs. Frequency, f_{PFD} = 15.36 MHz, 30.72 MHz, and 61.44 MHz, Loop Filter = 35 kHz

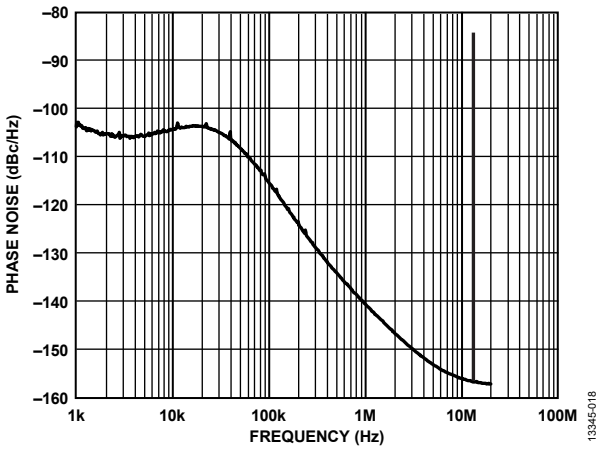

Figure 14. Spur Performance, GSM1800 Band, $RF_{OUT}A+$ = 1550.2 MHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide by 4 Selected, Loop Filter Bandwidth = 35 kHz, Channel Spacing = 20 kHz

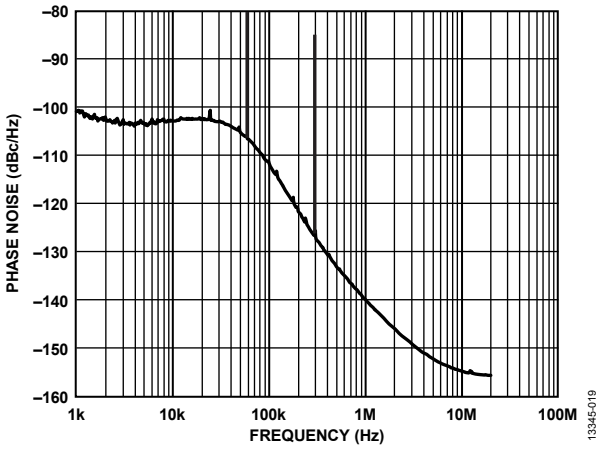

Figure 15. Spur Performance, W-CDMA Band, $RF_{OUT}A+$ = 2113.5 MHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 35 kHz, Channel Spacing = 20 kHz

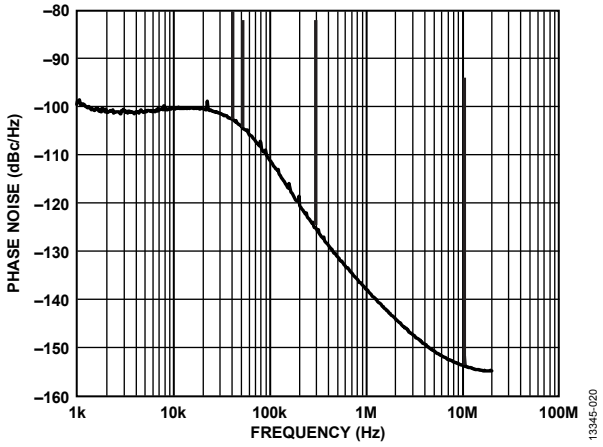

Figure 16. Spur Performance, $RF_{OUT}A+$ = 2.591 GHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide-by-2 Selected, Loop Filter Bandwidth = 35 kHz, Channel Spacing = 20 kHz

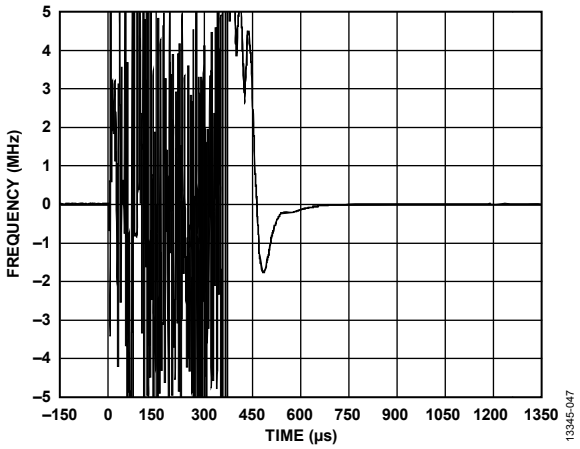

Figure 17. Lock Time for 100 MHz Jump from 3300 MHz to 6600 MHz, Loop Bandwidth = 3 kHz

THEORY OF OPERATION

REFERENCE INPUT SECTION

Figure 18 shows the reference input section of the ADF4355-3. The reference input can accept both single-ended and differential signals. Use the reference mode bit (Register 4, Bit DB9) to select the signal. To use a differential signal on the reference input, program this bit high. In this case, SW1 and SW2 are open, SW3 and SW4 are closed, and the current source that drives the differential pair of transistors switches on. The differential signal is buffered, and it is provided to an emitter coupled logic (ECL) to a CMOS converter. When a single-ended signal is the reference, connect the reference signal to $REF_{IN}A$ and program Bit DB9 in Register 4 to 0. In this case, SW1 and SW2 are closed, SW3 and SW4 are open, and the current source that drives the differential pair of transistors switches off. Single-ended mode results in lower integer boundary spurs.

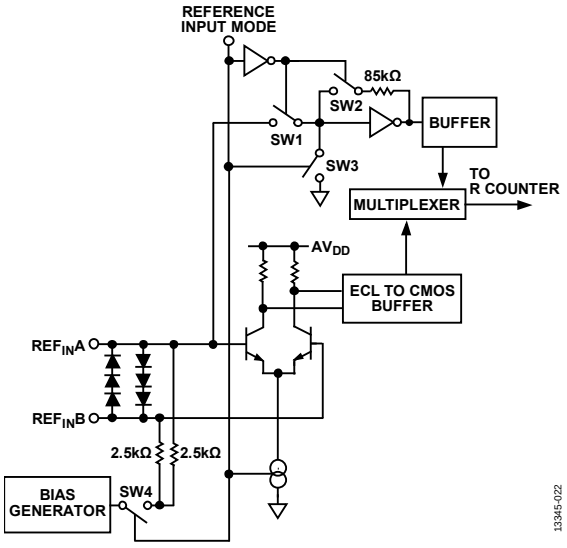

Figure 18. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. Determine the division ratio by the INT, FRAC1, FRAC2, and MOD2 values that this divider comprises.

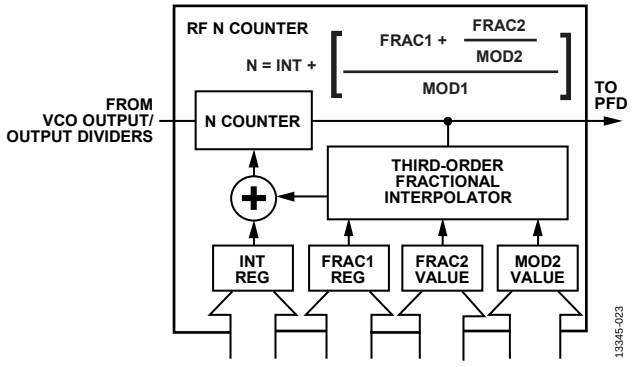

Figure 19. RF N Divider

INT, FRACx, MODx, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). For more information, see the RF Synthesizer—A Worked Example section.

Calculate the RF VCO frequency (VCO_{OUT}) by

$$VCO_{OUT} = f_{PFD} \times N \quad (1)$$

where:
VCO_{OUT} is the output frequency of the VCO (without using the output divider).
f_{PFD} is the frequency of the phase frequency detector.
N is the desired value of the feedback counter, N.

Calculate f_{PFD} by

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).
T is the REF_{IN} divide by 2 bit (0 or 1).

N comprises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \quad (3)$$

where:
INT is the 16-bit integer value (23 to 32,767 for the 4/5 prescaler, and 75 to 65,535 for the 8/9 prescaler).
FRAC1 is the numerator of the primary modulus (0 to 16,777,215).
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383).
MOD2 is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383).
MOD1 is a 24-bit primary modulus with a fixed value of 2^{24} = 16,777,216.

Equation 3 results in a very fine frequency resolution with no residual frequency error. Apply this formula using the following steps:

1. Calculate N by dividing VCO_{OUT}/f_{PFD}. The integer value of this number forms INT.
2. Subtract the INT value from the full N value.
3. Multiply the remainder by 2^{24}. The integer value of this number forms FRAC1.
4. Calculate the MOD2 based on the channel spacing (f_{CHSP}) by

$$MOD2 = f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) \quad (4)$$

where:
f_{CHSP} is the desired channel spacing.
$GCD(f_{PFD}, f_{CHSP})$ is the greatest common divider of the PFD frequency and the channel spacing frequency.

5. Calculate FRAC2 by the following equation:

$$FRAC2 = ((N - INT) \times 2^{24} - FRAC1)) \times MOD2 \quad (5)$$

The FRAC2 and MOD2 fraction results in outputs with zero frequency error for channel spacings when

$$f_{PFD}/GCD(f_{PFD}/f_{CHSP}) < 16{,}383 \quad (6)$$

where:
f_{PFD} is the frequency of the phase frequency detector.
GCD is a greatest common divider function.
f_{CHSP} is the desired channel spacing.

If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 38-bit resolution modulus.

INT N Mode

When FRAC1 and FRAC2 = 0, the synthesizer operates in integer-N mode.

R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 20 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO.

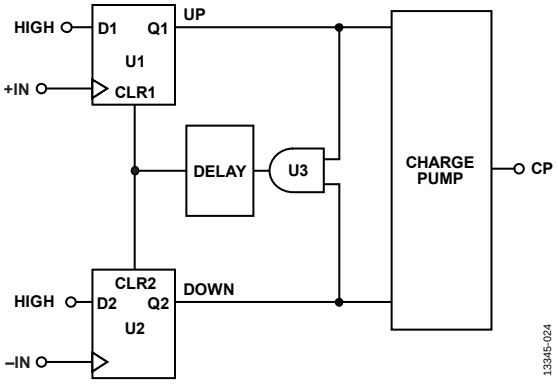

Figure 20. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4355-3 allows the user to access various internal points on the chip. The M3, M2, and M1 bits in Register 4 control the state of MUXOUT. Figure 21 shows the MUXOUT section in block diagram form.

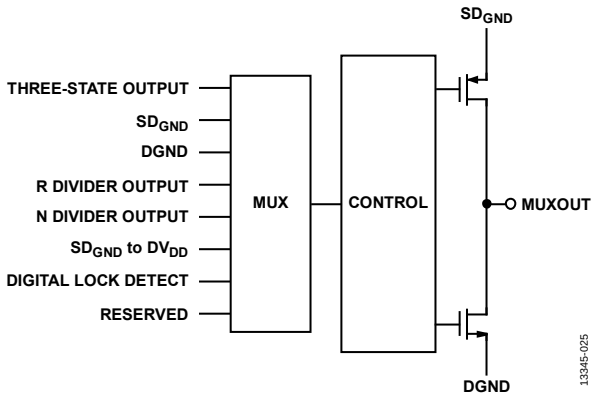

Figure 21. MUXOUT Block Diagram

If negative bleed is enabled, lock detect is not reliable for low PFD frequencies.

INPUT SHIFT REGISTERS

The ADF4355-3 digital section includes a 10-bit R counter, a 16-bit RF integer-N counter, a 24-bit FRAC1 counter, a 14-bit auxiliary fractional counter, and a 14-bit auxiliary modulus counter. Data clocks into the 32-bit shift register on each rising edge of CLK. The data clocks in MSB first. Data transfers from the shift register to one of 13 latches on the rising edge of LE. The state of the four control bits (C4, C3, C2, and C1) in the shift register determines the destination latch. As shown in Figure 2, the four least significant bits (LSBs) are DB3, DB2, DB1, and DB0. The truth table for these bits is shown in Table 5. Figure 24 and Figure 25 summarize the programing of the latches.

Table 5. Truth Table for the C4, C3, C2, and C1 Control Bits

Control Bits				
C4	C3	C2	C1	Register
0	0	0	0	Register 0
0	0	0	1	Register 1
0	0	1	0	Register 2
0	0	1	1	Register 3
0	1	0	0	Register 4
0	1	0	1	Register 5
0	1	1	0	Register 6
0	1	1	1	Register 7
1	0	0	0	Register 8
1	0	0	1	Register 9
1	0	1	0	Register 10
1	0	1	1	Register 11
1	1	0	0	Register 12

PROGRAM MODES

Table 5 and Figure 24 through Figure 38 show the program modes that must be set up in the ADF4355-3.

The following settings in the ADF4355-3 are double buffered: main fractional value (FRAC1), auxiliary modulus value (MOD2), auxiliary fractional value (FRAC2), reference doubler, reference divide by 2 (RDIV2), phase value, R counter value, and charge pump current setting. Two events must occur before the ADF4355-3 uses a new value for any of the double buffered settings. First, the new value must latch into the device by writing to the appropriate register, and second, a new write to Register 0 must be performed.

For example, to ensure that the modulus value loads correctly, every time the modulus value updates, Register 0 must be written to. The RF divider select in Register 6 is also double buffered, but only when DB14 of Register 4 is high.

VCO

The VCO core in the ADF4355-3 consists of four separate VCOs, each of which uses 256 overlapping bands, which allows covering a wide frequency range without a large VCO sensitivity (K_V) and without resulting poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic when Register 0 is updated and autocalibration is enabled. The VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage.

The R counter output is the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of K_V is 63 MHz/V when the N divider is driven from the VCO output, or the K_V value is divided by D. D is the output divider value if the N divider is driven from the RF output divider (chosen by programming Bits[D23:D21] in Register 6).

The VCO shows the variation of K_V as the tuning voltage, V_{TUNE}, varies within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 63 MHz/V provides the most accurate K_V, because this value is closest to the average value. Figure 22 shows how K_V varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer this figure when using narrow-band designs.

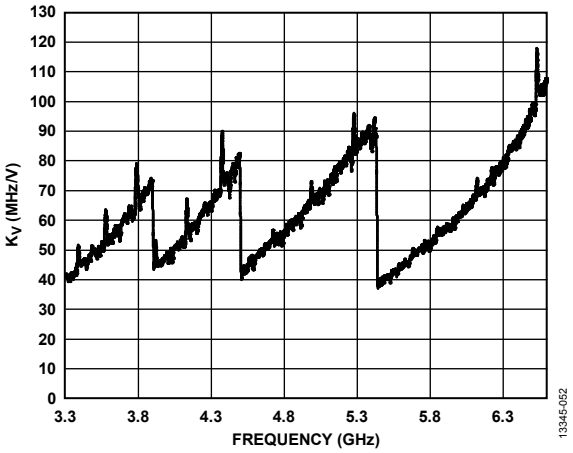

Figure 22. K_V vs. VCO Frequency

OUTPUT STAGE

The $RF_{OUT}A+$ and $RF_{OUT}A-$ pins of the ADF4355-3 connect to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 23. In this scheme, the ADF4355-3 contains internal 50 Ω resistors connected to the V_{RF} pin. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable using Bits[DB5:DB4] in Register 6. Four current levels can be set. These levels give the approximate output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively, using a 50 Ω resistor to V_{RF} and ac coupling into a 50 Ω load. For accurate power levels, see the Typical Performance Characteristics section. Add an external shunt inductor to provide higher power levels; however, this is less wideband than the internal bias only. Terminate the unused complementary output with a similar circuit to the used output.

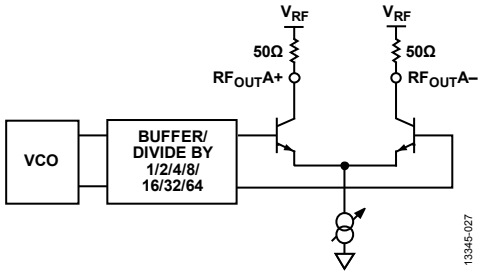

Figure 23. Output Stage

Another feature of the ADF4355-3 is that the supply current to the output stages can shut down until the ADF4355-3 achieves lock as measured by the digital lock detect circuitry. The mute until lock detect (MTLD) bit (Bit DB11) in Register 6 enables this function.

The $RF_{OUT}B+/RF_{OUT}B-$ pins are duplicate outputs that can be used independently or in addition to the $RF_{OUT}A+/RF_{OUT}A-$ pins.

LOOP FILTER

Use only passive loop filters. For information on designing a loop filter, use the ADIsimPLL design tool.

Table 6. Total I_{DD} ($RF_{OUT}A\pm$ Refers to $RF_{OUT}A+/RF_{OUT}A-$)

Divide By	$RF_{OUT}A\pm$ Off	$RF_{OUT}A\pm$ = −4 dBm	$RF_{OUT}A\pm$ = −1 dBm	$RF_{OUT}A\pm$ = +2 dBm	$RF_{OUT}A\pm$ = +5 dBm
I_{VCO} and I_P	49.4 mA	49.4 mA	49.4 mA	49.4 mA	49.4 mA
AI_{DD}, DI_{DD}, I_{RF}					
1	91.8 mA	103.3 mA	106.5 mA	111.7 mA	116.9 mA
2	100.9 mA	113.6 mA	117.0 mA	122.8 mA	128.4 mA
4	110.8 mA	123.9 mA	127.5 mA	133.6 mA	139.8 mA
8	118.9 mA	132.1 mA	135.6 mA	141.8 mA	148.0 mA
16	124.0 mA	137.3 mA	140.8 mA	147.0 mA	153.3 mA
32	128.0 mA	141.4 mA	144.9 mA	151.1 mA	157.5 mA
64	130.4 mA	144.0 mA	147.4 mA	153.6 mA	160.0 mA

REGISTER MAPS

REGISTER 0

RESERVED										AUTOCAL	PRESCALER	16-BIT INTEGER VALUE (INT)															CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	AC1	PR1	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				24-BIT MAIN FRACTIONAL VALUE (FRAC1) DBR[1]																							CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2

14-BIT AUXILIARY FRACTIONAL VALUE (FRAC2) DBR[1]														14-BIT AUXILIARY MODULUS VALUE (MOD2) DBR[1]													CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED	SD LOAD RESET	PHASE RESYNC	PHASE ADJUST	24-BIT PHASE VALUE (PHASE) DBR[1]																							CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SD1	PR1	PA1	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED	MUXOUT			REFERENCE DOUBLER DBR[1]	RDIV2 DBR[1]	10-BIT R COUNTER DBR[1]											DOUBLE BUFF	CURRENT SETTING DBR[1]				REF MODE	MUX LOGIC	PD POLARITY	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	U6	U5	U4	U3	U2	U1	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5

RESERVED																											CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6

RESERVED	GATED BLEED	NEGATIVE BLEED	RESERVED				FEEDBACK SELECT	RF DIVIDER SELECT[2]			CHARGE PUMP BLEED CURRENT								RESERVED	MTLD	RESERVED	AUX RF OUTPUT ENABLE	AUX RF OUTPUT POWER		RF OUTPUT ENABLE	RF OUTPUT POWER		CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BL10	BL9	1	0	1	0	D13	D12	D11	D10	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	0	D8	0	D6	D5	D4	D3	D2	D1	C4(0)	C3(1)	C2(1)	C1(0)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE BUFFERED BITS—BUFFERED BY A WRITE TO REGISTER 0 WHEN BIT DB14 OF REGISTER 4 IS HIGH.

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Figure 24. Register Summary (Register 0 to Register 6)

REGISTER 7

RESERVED						LE SYNC	RESERVED														LD CYCLE COUNT		LOL MODE	FRAC-N LD PRECISION		LDO MODE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	LE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD5	LD4	LOL	LD3	LD2	LD1	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	1	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9

VCO BAND DIVISION								TIMEOUT										RESERVED					SYNTHESIZER LOCK TIMEOUT					CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	1	1	1	1	1	SL5	SL4	SL3	SL2	SL1	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10

RESERVED																		ADC CLOCK DIVIDER								ADC CONVERSION	ADC ENABLE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AE2	AE1	C4(1)	C3(0)	C2(1)	C1(0)

REGISTER 11

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

REGISTER 12

RESYNC CLOCK																RESERVED												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	0	0	0	0	1	0	1	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

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Figure 25. Register Summary (Register 7 to Register 12)

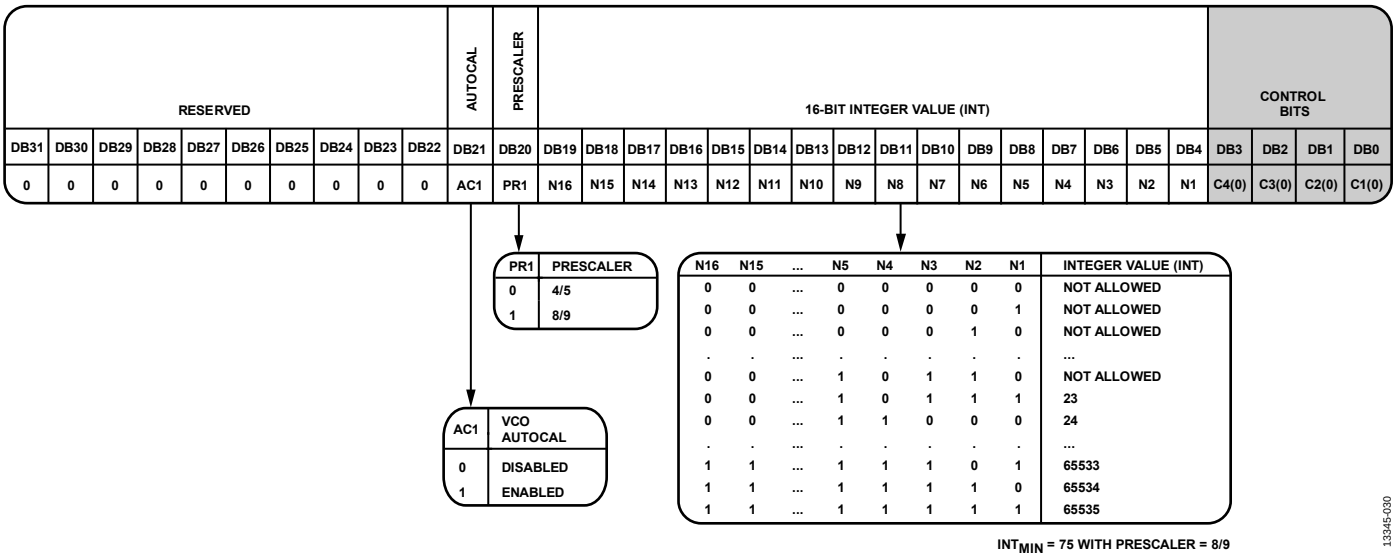


Figure 26. Register 0

REGISTER 0

Control Bits

With Bits[C4:C1] set to 0000, Register 0 is programmed. Figure 26 shows the input data format for programming this register.

Reserved

Bits[DB31:DB22] are reserved and must be set to 0.

Automatic Calibration (Autocal)

Write to Register 0 to enact (by default) the VCO automatic calibration, and to choose the appropriate VCO and VCO subband. Write 1 to the AC1 bit (Bit DB21) to enable the automatic calibration, which is the recommended mode of operation.

Set the AC1 bit to 0 to disable the automatic calibration, which leaves the ADF4355-3 in the same band it is already in when Register 0 is updated.

Disable the automatic calibration only for fixed frequency applications, phase adjust applications, or very small (<10 kHz) frequency jumps.

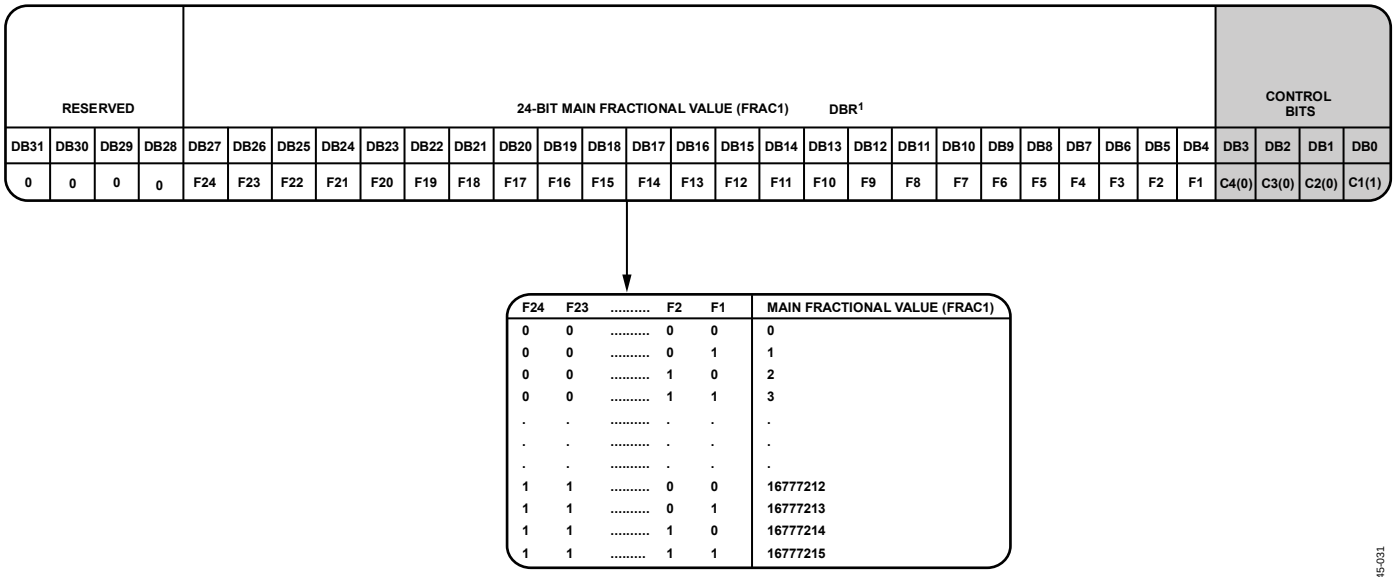
Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRACx, and MODx counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (Bit DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. The prescaler limits the INT value; therefore, if P is 4/5, INT_{MIN} is 23, and if P is 8/9, INT_{MIN} is 75.

16-Bit Integer Value

The 16 INT bits (Bits[DB19:DB4]) set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 3 (see the RF Synthesizer—A Worked Example section). All integer values from 23 to 32,767 are allowed for the 4/5 prescaler. For the 8/9 prescaler, the minimum integer value is 75, and the maximum value is 65,535.



1DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 27. Register 1

REGISTER 1

Control Bits

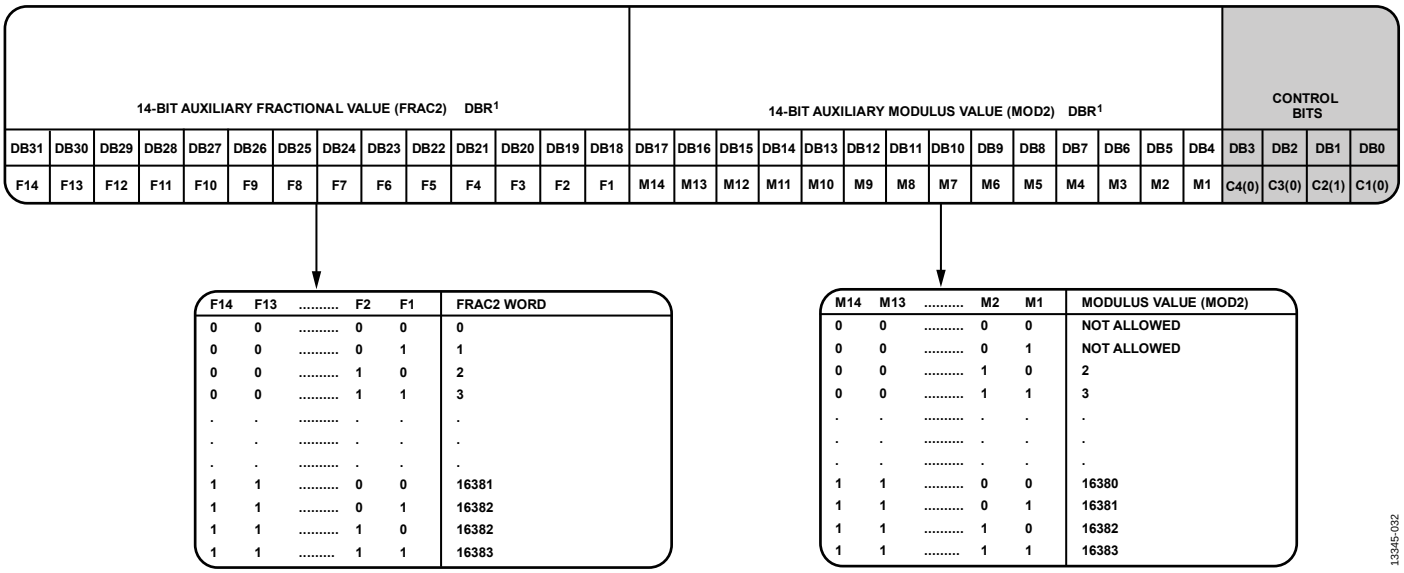
With Bits[C4:C1] set to 0001, Register 1 is programmed. Figure 27 shows the input data format for programming this register.

Reserved

Bits[DB31:DB28] are reserved and must be set to 0.

24-Bit Main Fractional Value

The 24 FRAC1 bits (Bits[DB27:DB4]) set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC1 values from 0 to (MOD1 − 1) cover channels over a frequency range equal to the PFD reference frequency.



1DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 28. Register 2

REGISTER 2

Control Bits

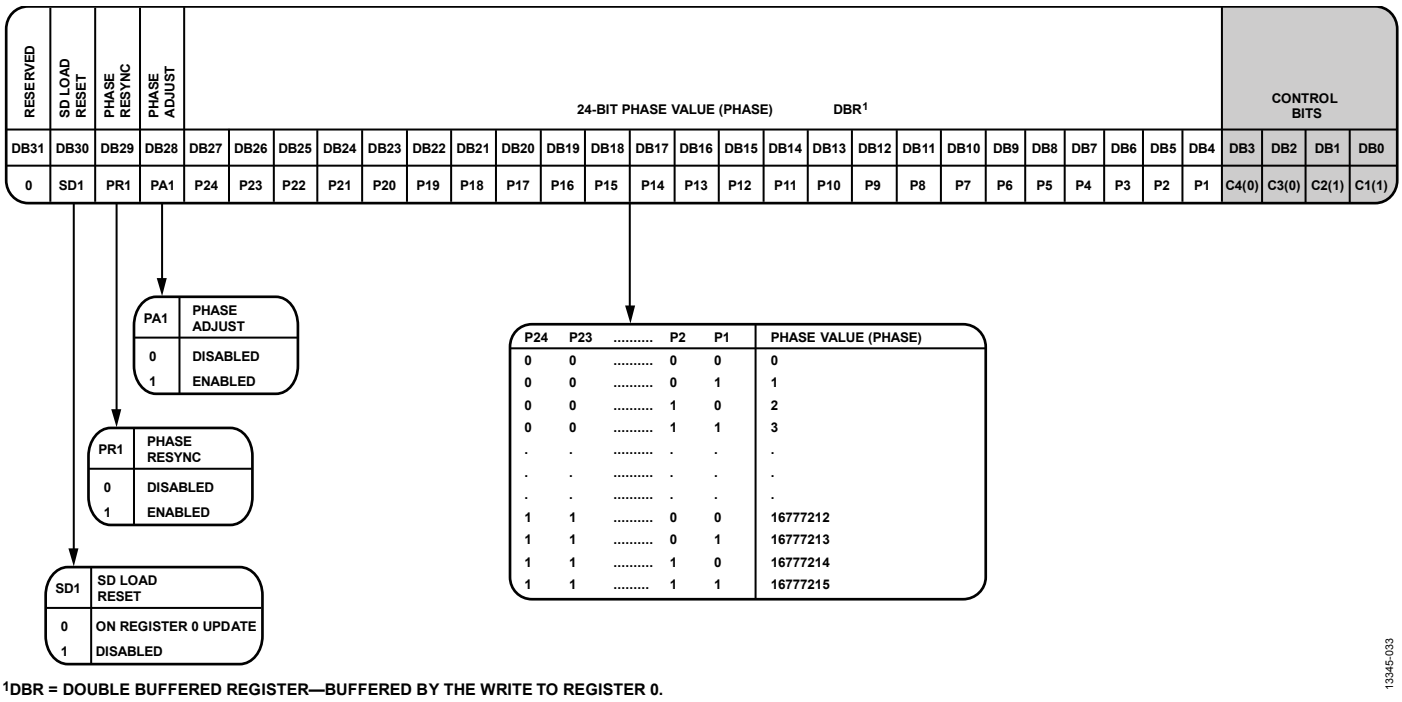
With Bits[C4:C1] set to 0010, Register 2 is programmed. Figure 28 shows the input data format for programming this register.

14-Bit Auxiliary Fractional Value (FRAC2)

The 14-bit auxiliary fractional value (Bits[DB31:DB18]) controls the auxiliary fractional word. FRAC2 must be less than the MOD2 value programmed in Register 2.

14-Bit Auxiliary Modulus Value (MOD2)

The 14-bit auxiliary modulus value (Bits[DB17:DB4]) sets the auxiliary fractional modulus. Use MOD2 to correct any residual error due to the main fractional modulus.



[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 29. Register 3

REGISTER 3

Control Bits

With Bits[C4:C1] set to 0011, Register 3 is programmed. Figure 29 shows the input data format for programming this register.

Reserved

Bit DB31 is reserved and must be set to 0.

SD Load Reset

When writing to Register 0, the Σ-Δ (SD) modulator resets. For applications in which the phase is continually adjusted, this reset may not be desirable; therefore, in these cases, the Σ-Δ reset can be disabled by writing a 1 to the SD1 bit (Bit DB30).

Phase Resync

To use the phase resynchronization feature, the PR1 bit (Bit DB29) must be set to 1. If unused, the bit can be programmed to 0. The phase resync timer must also be used in Register 12 to ensure that the resynchronization feature is applied after the PLL settles to the final frequency. If the PLL has not settled to the final frequency, phase resync may not function correctly. Resynchronization is useful in phased array and beam forming applications. It ensures repeatability of output phase when programming the same frequency. In phase critical applications that use frequencies requiring the output divider (<3300 MHz), it is necessary to feed the N divider with the divided VCO frequency as distinct from the fundamental VCO frequency, which is achieved by programming the D13 bit (Bit DB24) in Register 6 to 0, which ensures divided feedback to the N divider.

For resync applications, enable the Σ-Δ modulator load reset in Register 3 by setting DB30 to 0. Phase resync functions only when FRAC2 = 0.

Phase Adjustment

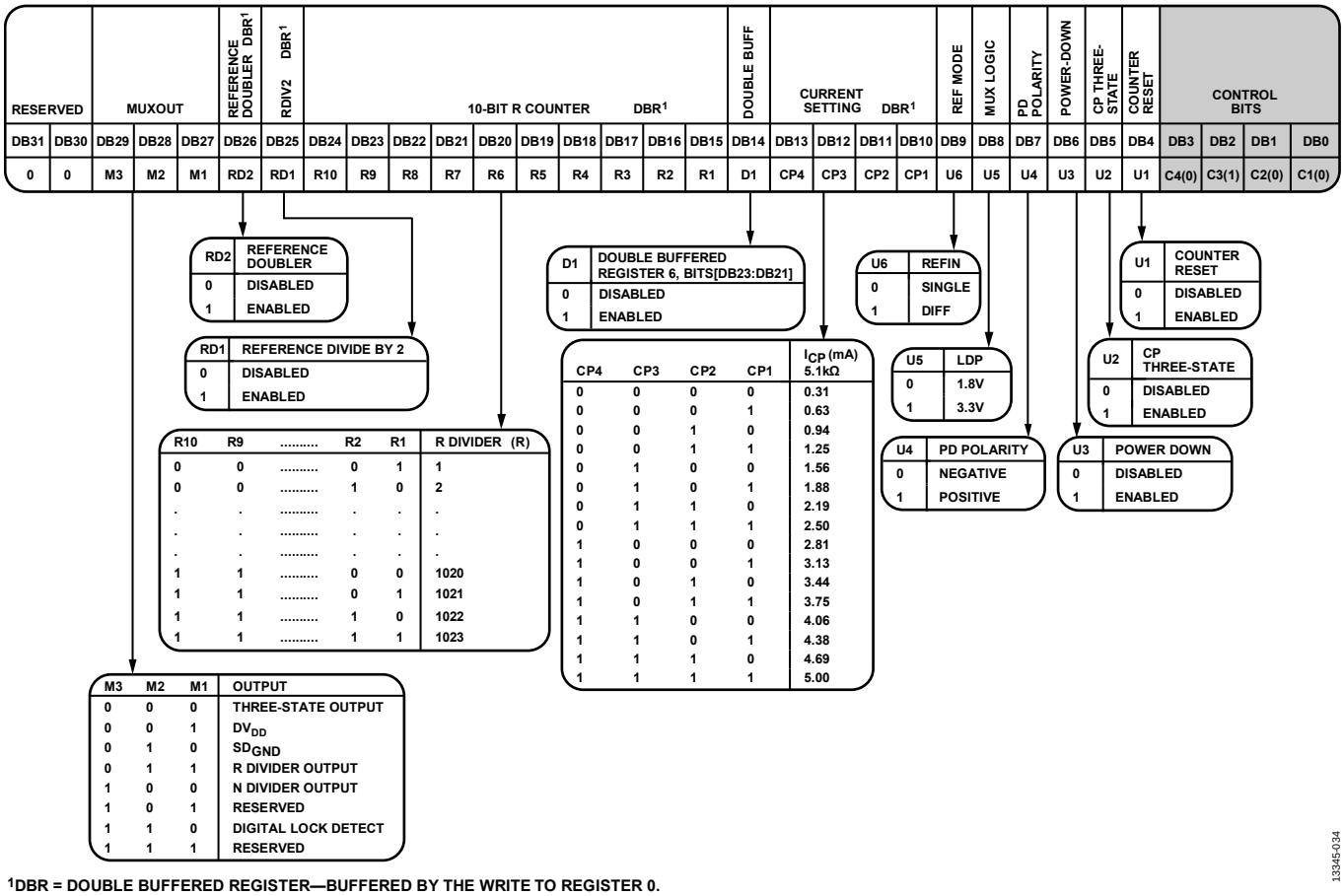
To adjust the relative output phase of the ADF4355-3 on each Register 0 update, set the PA1 bit (Bit DB28) to 1. This feature differs from the resynchronization feature in that it is useful when adjustments to phase are made continually in an application. For this function, disable the VCO automatic calibration by setting the AC1 bit (Bit DB21) in Register 0 to 1, and disable the SD load reset by setting the SD1 bit (Bit DB30) in Register 3 to 1. Note that phase resync and phase adjustment cannot be used simultaneously.

24-Bit Phase Value

The phase of the RF output frequency can be adjusted in 24-bit steps; from 0° (0) to 360° ($2^{24} - 1$). For phase adjustment applications, the phase is set by

$$(Phase\ Value/16{,}777{,}216) \times 360° \quad (7)$$

When the phase value is programmed to Register 3, each subsequent adjustment of Register 0 increments the phase by the value in this equation.



[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 30. Register 4

REGISTER 4

Control Bits

With Bits[C4:C1] set to 0100, Register 4 is programmed. Figure 30 shows the input data format for programming this register.

Reserved

Bits[DB31:DB30] are reserved and must be set to 0.

MUXOUT

The on-chip multiplexer (MUXOUT) is controlled by Bits[DB29:DB27]. For additional details, see Figure 30.

When changing frequency, that is, writing R0, MUXOUT must not be set to the N divider output or the R divider output. If needed, enable these functions after locking to the new frequency.

Reference Doubler

Setting the RD2 bit (Bit DB26) to 0 feeds the REF_{IN} signal directly to the 10-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the reference frequency by a factor of 2 before feeding it into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of the reference frequency become active edges at the PFD input.

The maximum allowable reference frequency when the doubler is enabled is 100 MHz.

RDIV2

Setting the RDIV2 bit (Bit DB25) to 1 inserts a divide by 2 toggle flip-flop between the R counter and PFD, which halves the reference frequency to the PFD. This function provides a 50% duty cycle signal at the PFD input.

10-Bit R Counter

The 10-bit R counter divides the input reference frequency (REF_{IN}) to produce the reference clock to the PFD. Division ratios range from 1 to 1023.

Double Buffer

The D1 bit (Bit DB14) enables or disables double buffering of the RF divider select bits (Bits[DB23:DB21]) in Register 6. The Program Modes section explains double buffering further.

Charge Pump Current Setting

The CP4 to CP1 bits (Bits[DB13:DB10]) set the charge pump current. Set this value to the charge pump current that the loop filter is designed with (see Figure 30). For the lowest spurs, the 0.9 mA setting is recommended.

Reference Mode

The ADF4355-3 permits the use of either differential or single-ended reference sources. For differential sources, set the reference mode bit (Bit DB9) to 1, and for single-ended sources, set it to 0. Single-ended mode results in lower integer boundary spurs. If only a differential signal is available, $REF_{IN}B$ can be left floating to get the integer boundary spur improvements (provided that the frequency and power meets the single-ended requirements shown in Table 1).

Level Select

To assist with logic compatibility, MUXOUT is programmable to two logic levels. Set the U5 bit (Bit DB8) to 0 to select 1.8 V logic, and set it to 1 to select 3.3 V logic.

Phase Detector Polarity

The U4 bit (Bit DB7) sets the phase detector polarity. Set DB7 to 1. Active filters are not supported.

Power-Down

The U3 bit (Bit DB6) sets the programmable power-down mode. Setting DB6 to 1 performs a power-down. Setting DB6 to 0 returns the synthesizer to normal operation. In software power-down mode, the ADF4355-3 retains all information in its registers. The register contents are lost only if the supply voltages are removed.

When power-down activates, the following events occur:

- The synthesizer counters are forced to their load state conditions.
- The VCO powers down.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry resets.
- The $RF_{OUT}A+/RF_{OUT}A-$ and $RF_{OUT}B+/RF_{OUT}B-$ output stages are disabled.
- The input registers remain active and capable of loading and latching data.

Charge Pump Three-State

Setting the U2 bit (Bit DB5) to 1 puts the charge pump into three-state mode. Set DB5 to 0 for normal operation.

Counter Reset

The U1 bit (Bit DB4) resets the R counter, N counter, and VCO band selection of the ADF4355-3. When DB4 is set to 1, the RF synthesizer N counter and R counter and the VCO band selection are reset. For normal operation, set DB4 to 0.

REGISTER 5

The bits in Register 5 are reserved and must be programmed as described in Figure 31, using a hexadecimal word of 0x00800005.

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	C4(0)	C3(1)	C2(0)	C1(1)

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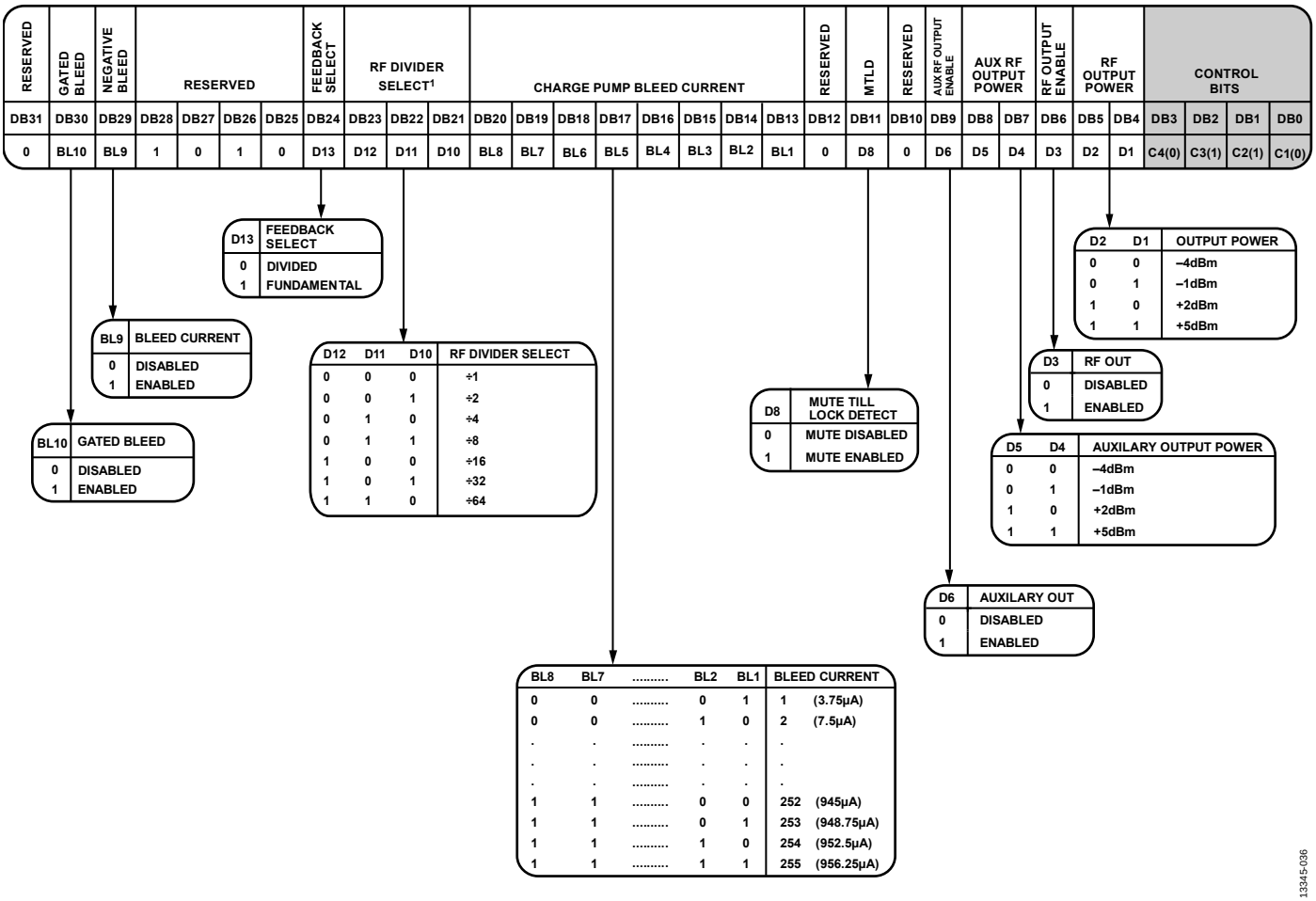
Figure 31. Register 5 (0x00800005)



[1]BITS[DB23:DB21] ARE BUFFERED BY A WRITE TO REGISTER 0 WHEN THE DOUBLE BUFFER BIT IS ENABLED, BIT DB14 OF REGISTER 4.

Figure 32. Register 6

REGISTER 6

Control Bits

With Bits[C4:C1] set to 0110, Register 6 is programmed. Figure 32 shows the input data format for programming this register.

Reserved

Bit DB31 is reserved and must be set to 0.

Gated Bleed

Bleed currents can improve phase noise and spurs. However, due to a potential impact on lock time, the gated bleed bit, BL10 (Bit DB30), if set to 1, ensures bleed currents are not switched on until the digital lock detect asserts logic high. Note that this function requires digital lock detection to be enabled.

Negative Bleed

Use of constant negative bleed is recommended for most applications because it improves the linearity of the charge pump, leading to lower noise and spurious performance than leaving constant negative bleed off. To enable negative bleed, write 1 to BL9 (Bit DB29), and to disable negative bleed, write 0 to BL9 (Bit DB29). Use negative bleed only when operating in fractional-N mode, that is, FRAC1 or FRAC2 not equal to 0.

Reserved

Bits[DB28:DB25] are reserved and must be set to 1010.

Feedback Select

D13 (Bit DB24) selects the feedback from the output of the VCO to the N counter. When D13 is set to 1, the signal is taken directly from the VCO. When this bit is set to 0, the signal is taken from the output of the output dividers. The dividers enable coverage of the wide frequency band (51.5625 MHz to 6.6 GHz). When the divider is enabled and the feedback signal is taken from the output, the RF output signals of two separately configured PLLs are in phase. Divided feedback is useful in some applications where the positive interference of signals is required to increase the power.

Divider Select

D12 to D10 (Bits[DB23:DB21]) select the value of the RF output divider (see Figure 32). These bits are buffered by a write to Register 0 when Bit DB14 of Register 4 is high.

Charge Pump Bleed Current

BL8 to BL1 (Bits[DB20:DB13]) control the level of the bleed current added to the charge pump output. This current optimizes the phase noise and spurious levels from the device.

Calculate the optimal bleed setting using Equation 8 and Equation 9.

If $f_{PFD} \leq 80$ MHz,

$$Bleed\ Value = Floor(39 \times (f_{PFD}/61.44\ MHz) \times (I_{CP}/0.9\ mA)) \quad (8)$$

If $f_{PFD} > 80$ MHz and ≤ 100 MHz,

$$Bleed\ Value = Floor(42 \times (I_{CP}/0.9\ mA)) \quad (9)$$

If $f_{PFD} > 100$ MHz, disable bleed current using DB29.

where:
Floor() is a function to round down to the nearest integer value.
Bleed Value is the value programmed to Bits[DB20:DB13].
f_{PFD} is the PFD frequency.
I_{CP} is the value of charge pump current setting, Bits[DB13:DB10] of Register 4.

Reserved

Bit DB12 is reserved and must be set to 0.

Mute Till Lock Detect

When D8 (Bit DB11) is set to 1, the supply current to the RF output stage is shut down until the device achieves lock, as determined by the digital lock detect circuitry.

Reserved

Bit DB10 is reserved and must be set to 0.

Auxiliary RF Output Enable

Bit DB9 enables or disables the auxiliary frequency RF output ($RF_{OUT}B+/RF_{OUT}B-$). When DB9 is set to 1, the auxiliary frequency RF output is enabled. When DB9 is set to 0, the auxiliary RF output is disabled.

Auxiliary RF Output Power

Bits[DB8:DB7] set the value of the auxiliary RF output power level.

RF Output Enable

Bit DB6 enables or disables the primary RF output ($RF_{OUT}A+/RF_{OUT}A-$). When DB6 is set to 0, the primary RF output is disabled; when DB6 is set to 1, the primary RF output is enabled.

Output Power

Bits[DB5:DB4] set the value of the primary RF output power level.

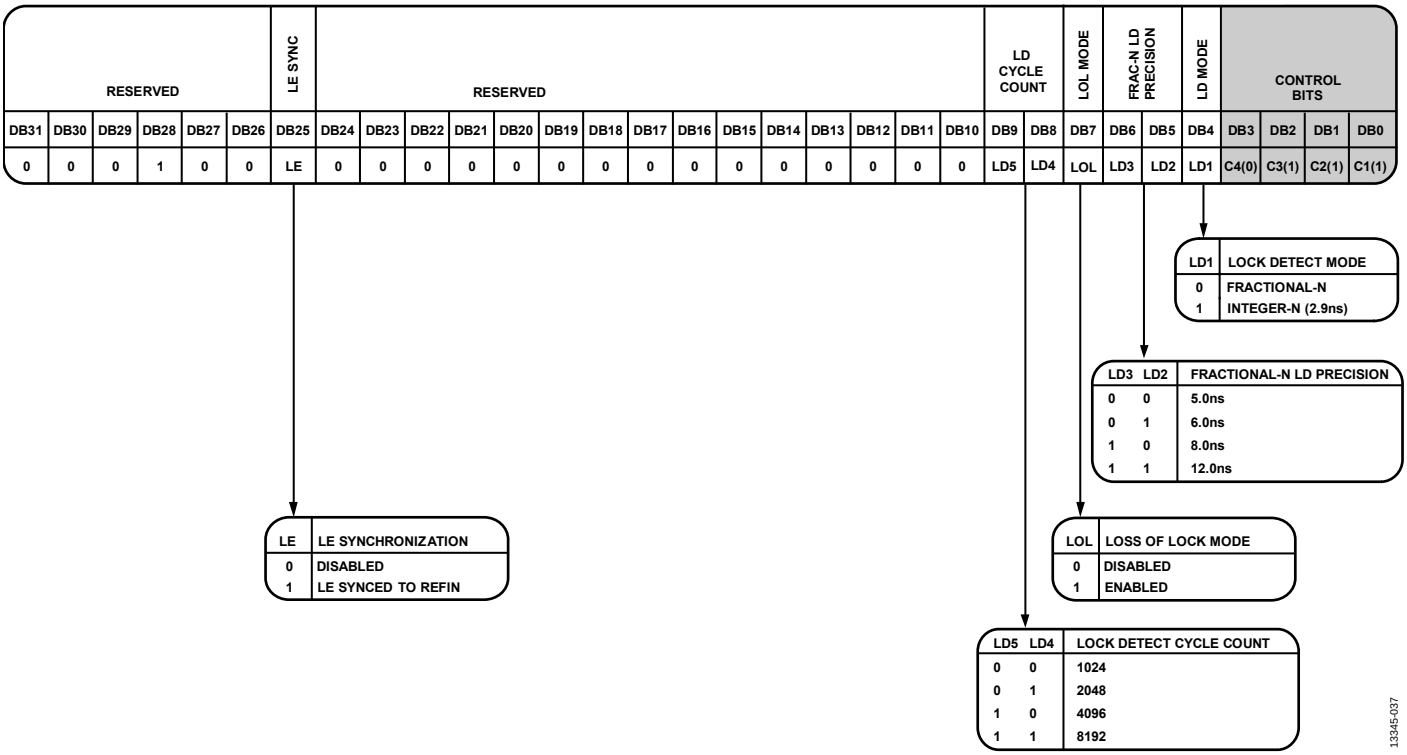


Figure 33. Register 7

REGISTER 7

Control Bits

With Bits[C4:C1] set to 0111, Register 7 is programmed. Figure 33 shows the input data format for programming this register.

Reserved

Bits[DB31:DB29] and Bits[DB27:DB26] are reserved and must be set to 0. Bit DB28 is reserved and must be set to 1.

LE Sync

When set to 1, Bit DB25 ensures that the load enable (LE) edge is synchronized internally with the rising edge of the reference input frequency. This synchronization prevents the rare event of reference and RF dividers loading at the same time as a falling edge of reference frequency, which can lead to longer lock times.

Reserved

Bits[DB24:DB10] are reserved and must be set to 0.

Fractional-N Lock Detect Count (LDC)

LD5 and LD4 (Bits[DB9:DB8]) set the number of consecutive cycles counted by the lock detect circuitry before asserting lock detect high. See Figure 33 for details.

Loss of Lock (LOL) Mode

Set LOL (Bit DB7) to 1 when the application is a fixed frequency application in which the reference (REF_{IN}) is likely to be removed, such as a clocking application. The standard lock detect circuit assumes that REF_{IN} is always present; however, this may not be the case with clocking applications. To enable this functionality, set Bit DB7 to 1. Loss of lock mode does not function reliably when using differential REF_{IN} mode.

Fractional-N Lock Detect Precision (LDP)

LD3 and LD2 (Bits[DB6:DB5]) set the precision of the lock detect circuitry in fractional-N mode. LDP is available at 5.0 ns, 6.0 ns, 8.0 ns, or 12.0 ns. If bleed currents are used, use 12.0 ns.

Lock Detect Mode (LDM)

If LD1 (Bit DB4) is set to 0, each reference cycle is set by the fractional-N lock detect precision as described in the Fractional-N Lock Detect Count (LDC) section. If DB4 is set to 1, each reference cycle is 2.9 ns long, which is more appropriate for integer-N applications.

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	1	C4(1)	C3(0)	C2(0)	C1(0)

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Figure 34. Register 8 (0x1A69A6B8)

VCO BAND DIVISION								TIMEOUT										RESERVED					SYNTHESIZER LOCK TIMEOUT					CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	1	1	1	1	1	SL5	SL4	SL3	SL2	SL1	C4(1)	C3(0)	C2(0)	C1(1)

TL10	TL9	.....	TL2	TL1	TIMEOUT
0	0	.....	0	1	1
0	0	.....	1	0	2
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	1020
1	1	.....	0	1	1021
1	1	.....	1	0	1022
1	1	.....	1	1	1023

SL5	SL4	.....	SL2	SL1	SLC WAIT
0	0	.....	0	1	1
0	0	.....	1	0	2
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	28
1	1	.....	0	1	29
1	1	.....	1	0	30
1	1	.....	1	1	31

VC8	VC7	.....	VC2	VC1	VCO BAND DIV
0	0	.....	0	1	1
0	0	.....	1	0	2
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	252
1	1	.....	0	1	253
1	1	.....	1	0	254
1	1	.....	1	1	255

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Figure 35. Register 9

REGISTER 8

The bits in this register are reserved and must be programmed as shown in Figure 34, using a hexadecimal word of 0x1A69A6B8.

REGISTER 9

For a worked example and more information, see the Lock Time section.

Control Bits

With Bits[C4:C1] set to 1001, Register 9 is programmed. Figure 35 shows the input data format for programming this register.

Reserved Bits

Bits[DB13:DB9]) are reserved and must be set to 0b11111.

VCO Band Division

VC8 to VC1 (Bits[DB31:DB24]) set the value of the VCO band division clock. Determine the value of this clock by

$$VCO\ Band\ Div = \text{ceiling}(f_{PFD}/2{,}400{,}000)$$

Timeout

TL10 to TL1 (Bits[DB23:DB14]) set the timeout value for the VCO band selection.

Synthesizer Lock Timeout

SL5 to SL1 (Bits[DB8:DB4]) set the synthesizer lock timeout value. This value allows the V_{TUNE} force to settle on the V_{TUNE} pin. The value must be 20 µs. Calculate the value using Equation 10:

$$Synthesizer\ Lock\ Timeout > (20\ \mu s \times f_{PFD})/Timeout \quad (10)$$

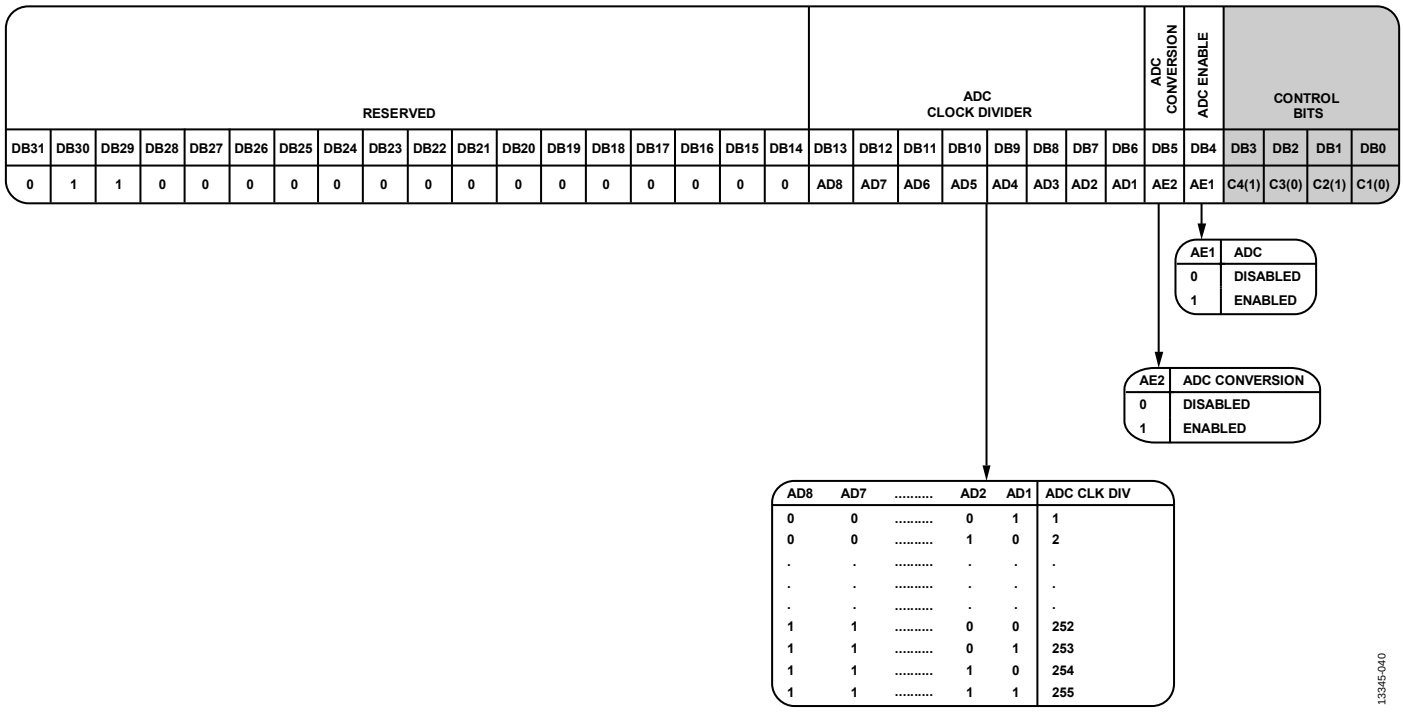

Figure 36. Register 10

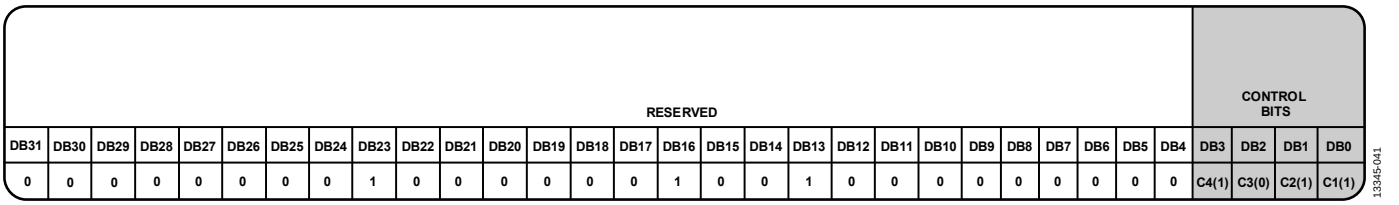

Figure 37. Register 11 (0x0081200B)

REGISTER 10

Control Bits

With Bits[C4:C1] set to 1010, Register 10 is programmed. Figure 36 shows the input data format for programming this register.

Reserved

Bits[DB31:DB14] are reserved. Bits[DB23:DB22] must be set to 11, and all other bits in this range must be set to 0.

ADC Conversion Clock (ADC_CLK_DIV)

An on-board analog-to-digital converter (ADC) is connected to a temperature sensor. It determines the V_{TUNE} setpoint relative to the ambient temperature of the ADF4355-3 environment. The ADC ensures that the initial tuning voltage in any application is chosen correctly to avoid any temperature drift issues.

The ADC uses a clock that is equal to the output of the R counter (or the PFD frequency) divided by ADC_CLK_DIV.

AD8 to AD1 (Bits[DB13:DB6]) set the value of this divider. On power-up, the R counter is not programmed; however, in these power-up cases, it defaults to R = 1.

Choose the ADC_CLK_DIV value such that

$$ADC\_CLK\_DIV = \text{ceiling}(((f_{PFD}/100{,}000) - 2)/4) \quad (11)$$

where ceiling() is a function to round up to the nearest integer.

For example, for f_{PFD} = 61.44 MHz, set ADC_CLK_DIV = 154 so that the ADC clock frequency is 99.417 kHz. If ADC_CLK_DIV is greater than 255, set it to 255.

ADC Conversion Enable

AE2 (Bit DB5) ensures that the ADC performs a conversion when a write to Register 10 is performed. It is recommended to enable this mode.

ADC Enable

AE1 (Bit DB4), when set to 1, powers up the ADC for the temperature dependent V_{TUNE} calibration. It is recommended to always use this function.

REGISTER 11

The bits in this register are reserved and must be programmed as described in Figure 37, using a hexadecimal word of 0x0081200B.

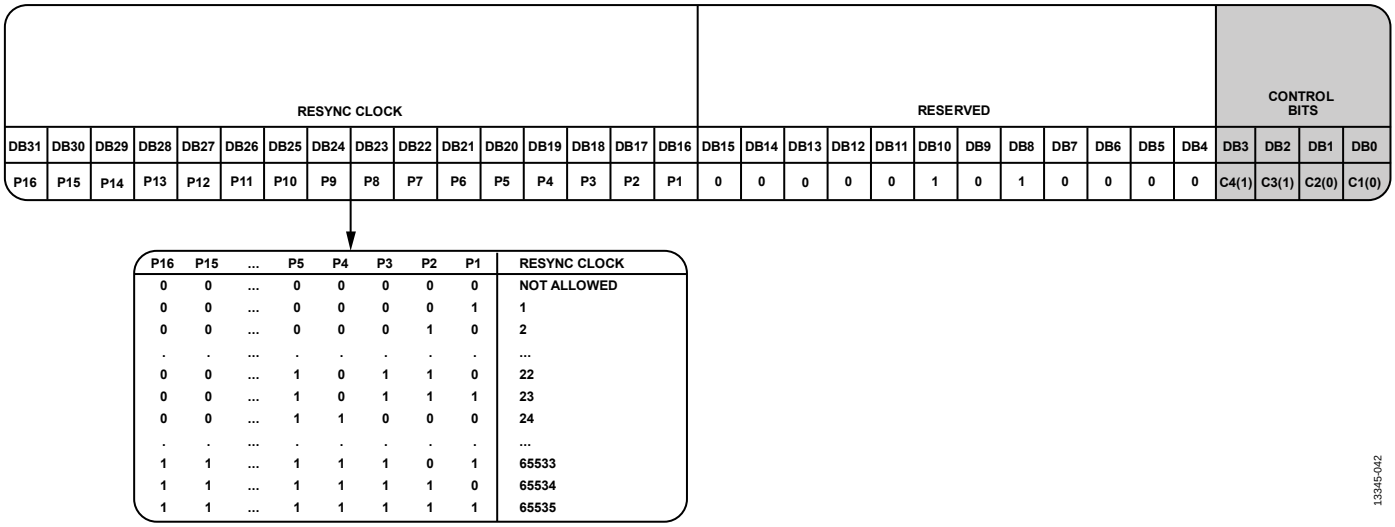

Figure 38. Register 12

REGISTER 12

Control Bits

With Bits[C4:C1] set to 1100, Register 12 is programmed. Figure 38 shows the input data format for programming this register.

Phase Resync Clock Divider Value

P16 to P1 (Bits[DB31:DB16]) set the timeout counter for activation of phase resync. This value must be set such that a the resync happens immediately after (and not before) the PLL achieves lock after reprogramming.

Calculate the timeout value using the following equation:

$$Timeout\ Value = Phase\ Resync\ Clock/f_{PFD} \quad (12)$$

Reserved

Bits[DB15:DB4] are reserved. Bit DB10 and Bit DB8 must be set to 1, but all other bits in this range must be set to 0.

REGISTER INITIALIZATION SEQUENCE

At initial power-up, after the correct application of voltages to the supply pins, the ADF4355-3 registers must be programmed in sequence. For f ≤ 75 MHz, use the following sequence:

1. Register 12.
2. Register 11.
3. Register 10.
4. Register 9.
5. Register 8.
6. Register 7.
7. Register 6.
8. Register 5.
9. Register 4.
10. Register 3.
11. Register 2.
12. Register 1.
13. Wait >16 ADC_CLK cycles. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 µs. See the Register 10 section for more information.
14. Register 0.

For f_{PFD} > 75 MHz (initially lock with halved f_{PFD}), use the following sequence:

1. Register 12.
2. Register 11.
3. Register 10.
4. Register 4 (with the R divider doubled to halve f_{PFD}).
5. Register 9.
6. Register 8.
7. Register 7.
8. Register 6.
9. Register 5.
10. Register 4 (with the R divider doubled to halve f_{PFD}).
11. Register 3.
12. Register 2 (for halved f_{PFD}).
13. Register 1 (for halved f_{PFD}).
14. Wait >16 ADC_CLK cycles. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 µs. See the Register 10 section for more information.
15. Register 0 (for halved f_{PFD}; autocalibration enabled).
16. Register 4 (with the R divider set for desired f_{PFD}).
17. Register 2 (for desired f_{PFD}).
18. Register 1 (for desired f_{PFD}).
19. Register 0 (for desired f_{PFD}; autocalibration disabled).

FREQUENCY UPDATE SEQUENCE

Frequency updates require updating the auxiliary modulator (MOD2) in Register 2, the fractional value (FRAC1) in Register 1, and the integer value (INT) in Register 0. It is recommended to perform a temperature dependent V_{TUNE} calibration by updating Register 10 first. Therefore, for $f_{PFD} \leq 75$ MHz, the sequence must be as follows:

1. Register 10.
2. Register 2.
3. Register 1.
4. Wait >16 ADC_CLK cycles. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 µs. See the Register 10 section for more information.
5. Register 0.

For $f_{PFD} > 75$ MHz (initially lock with halved f_{PFD}), the sequence must be as follows:

1. Register 10.
2. Register 4 (RDivider doubled for halved f_{PFD}).
3. Register 2 (for halved f_{PFD}).
4. Register 1 (for halved f_{PFD}).
5. Wait >16 ADC_CLK cycles. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 µs. See the Register 10 section for more information.
6. Register 0 (for halved f_{PFD}; autocalibration enabled).
7. Register 4 (RDivider set for desired f_{PFD}).
8. Register 2 (for desired f_{PFD}).
9. Register 1 (for desired f_{PFD}).
10. Register 0 (for desired f_{PFD}; autocalibration disabled).

The frequency change occurs only when writing to Register 0.

RF SYNTHESIZER—A WORKED EXAMPLE

Use the following equations to program the ADF4355-3 synthesizer:

$$RF_{OUT} = \left(INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1}\right) \times (f_{PFD})/RF\ Divider \quad (13)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC1 is the fractionality.
FRAC2 is the auxiliary fractionality.
MOD2 is the auxiliary modulus.
MOD1 is the fixed 24-bit modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (14)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.
T is the reference divide by 2 bit (0 or 1).

For example, in a universal mobile telecommunication system (UMTS) where 2112.8 MHz RF frequency output (RF_{OUT}) is required, a 122.88 MHz reference frequency input (REF_{IN}) is available. Note that the ADF4355-3 VCO operates in the frequency range of 3.3 GHz to 6.6 GHz. Therefore, RF divider of 2 must be used (VCO frequency = 4225.6 MHz, RF_{OUT} = VCO frequency/RF divider = 4225.6 MHz/2 = 2112.8 MHz).

The feedback path is also important. In this example, the VCO output is fed back before the output divider (see Figure 39).

In this example, the 122.88 MHz reference signal is divided by 2 to generate an f_{PFD} value of 61.44 MHz. The desired channel spacing is 200 kHz.

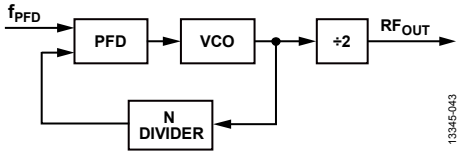

Figure 39. Loop Closed Before Output Divider

The worked example is as follows:

- $N = VCO_{OUT}/f_{PFD}$ = 4225.6 MHz/61.44 MHz = 68.7760416666666667
- INT = int(VCO frequency/f_{PFD}) = 68
- FRAC = 0.7760416666666667
- MOD1 = 16,777,216
- FRAC1 = int(MOD1 × FRAC) = 13,019,817
- Remainder = 0.6666666667 or 2/3
- MOD2 = $f_{PFD}/GCD(f_{PFD}/f_{CHSP})$ = 61.44 MHz/GCD(61.44 MHz/200 kHz) = 1536
- FRAC2 = remainder × 1536 = 1024

From Equation 14,

$$f_{PFD} = (122.88\ MHz \times (1 + 0)/2) = 61.44\ MHz \quad (15)$$

$$2112.8\ MHz = 61.44\ MHz \times ((INT + (FRAC1 + FRAC2/MOD2)/2^{24}))/2 \quad (16)$$

where:
INT = 68
FRAC1 = 13,019,817
FRAC2 = 1024
MOD2 = 1536

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. The doubler is useful for increasing the PFD comparison frequency. To improve the noise performance of the system, increase the PFD frequency. Doubling the PFD frequency typically improves noise performance by 3 dB.

The reference divide by 2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

SPURIOUS OPTIMIZATION AND FAST LOCK

Narrow loop bandwidths can filter unwanted spurious signals, but these bandwidths usually have a long lock time. A wider loop bandwidth achieves faster lock times but may lead to increased spurious signals inside the loop bandwidth.

OPTIMIZING JITTER

For lowest jitter applications, use the highest possible PFD frequency to minimize the contribution of in-band noise from the PLL. Set the PLL filter bandwidth such that the in-band noise of the PLL intersects with the open-loop noise of the VCO, minimizing the contribution of both to the overall noise.

Use the ADIsimPLL design tool for this task.

SPUR MECHANISMS

This section describes the two different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4355-3.

Integer Boundary Spurs

One mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or the difference in frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth (thus the name, integer boundary spurs).

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop may cause a problem. Feedthrough of low levels of on-chip reference switching noise, through the prescaler back to the VCO, can result in reference spur levels as high as −80 dBc.

LOCK TIME

The PLL lock time divides into a number of settings. All of these settings are modeled in the ADIsimPLL design tool.

Much faster lock times than those detailed in this data sheet are possible; contact Analog Devices, Inc., for more information.

Synthesizer Lock Timeout

The synthesizer lock timeout ensures that the VCO calibration DAC, which forces V_{TUNE}, settles to a steady value for the band select circuitry.

The timeout and synthesizer lock timeout variables programmed in Register 9 select the length of time the DAC is allowed to settle to the final voltage before the VCO calibration process continues to the next phase, which is VCO band selection. The PFD frequency is used as the clock for this logic, and the duration is set by

$$(Timeout \times Synthesizer\ Lock\ Timeout)/f_{PFD} \quad (17)$$

The calculated time must be greater than or equal to 20 µs.

VCO Band Selection

Use the PFD frequency again as the clock for the band selection process. Calculate this value by

$$f_{PFD}/(VCO\ Band\ Selection \times 16) < 150\ \text{kHz} \quad (18)$$

The band selection takes 11 cycles of the previously calculated value. Calculate the duration by

$$11 \times (VCO\ Band\ Selection \times 16)/f_{PFD} \quad (19)$$

PLL Low-Pass Filter Settling Time

The time taken for the loop to settle is inversely proportional to the low-pass filter bandwidth. The settling time is also modeled in the ADIsimPLL design tool.

The total lock time for changing frequencies is the sum of the three separate times (synthesizer lock, VCO band selection, and PLL settling time), all of which are modeled in the ADIsimPLL design tool.

APPLICATIONS INFORMATION

DIRECT CONVERSION MODULATOR

Direct conversion architectures are used to implement base station transmitters. Figure 40 shows how to use Analog Devices devices to implement such a system.

The circuit block diagram shows the AD9761 TxDAC® being used with the ADL5375. The use of a dual integrated DAC, such as the AD9761, ensures minimum error contribution (over temperature) from this portion of the signal chain.

The local oscillator (LO) is implemented using the ADF4355-3. The low-pass filter was designed using the ADIsimPLL design tool for a PFD of 61.44 MHz and a closed-loop bandwidth of 20 kHz.

The LO ports of the ADL5375 can be driven differentially from the complementary $RF_{OUT}A+/RF_{OUT}A-$ outputs of the ADF4355-3. A differential drive gives better second-order distortion performance than a single-ended LO driver and eliminates the use of a balun to convert from a single-ended LO input to the more desirable differential LO input for the ADL5375.

The ADL5375 accepts LO drive levels from −6 dBm to +6 dBm. The optimum LO power can be software programmed on the ADF4355-3, which allows levels from −4 dBm to +5 dBm from each output.

The RF output is designed to drive a 50 Ω load; however, it must be ac-coupled, as shown in Figure 40. If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power from the ADL5375 modulator is approximately 2 dBm.

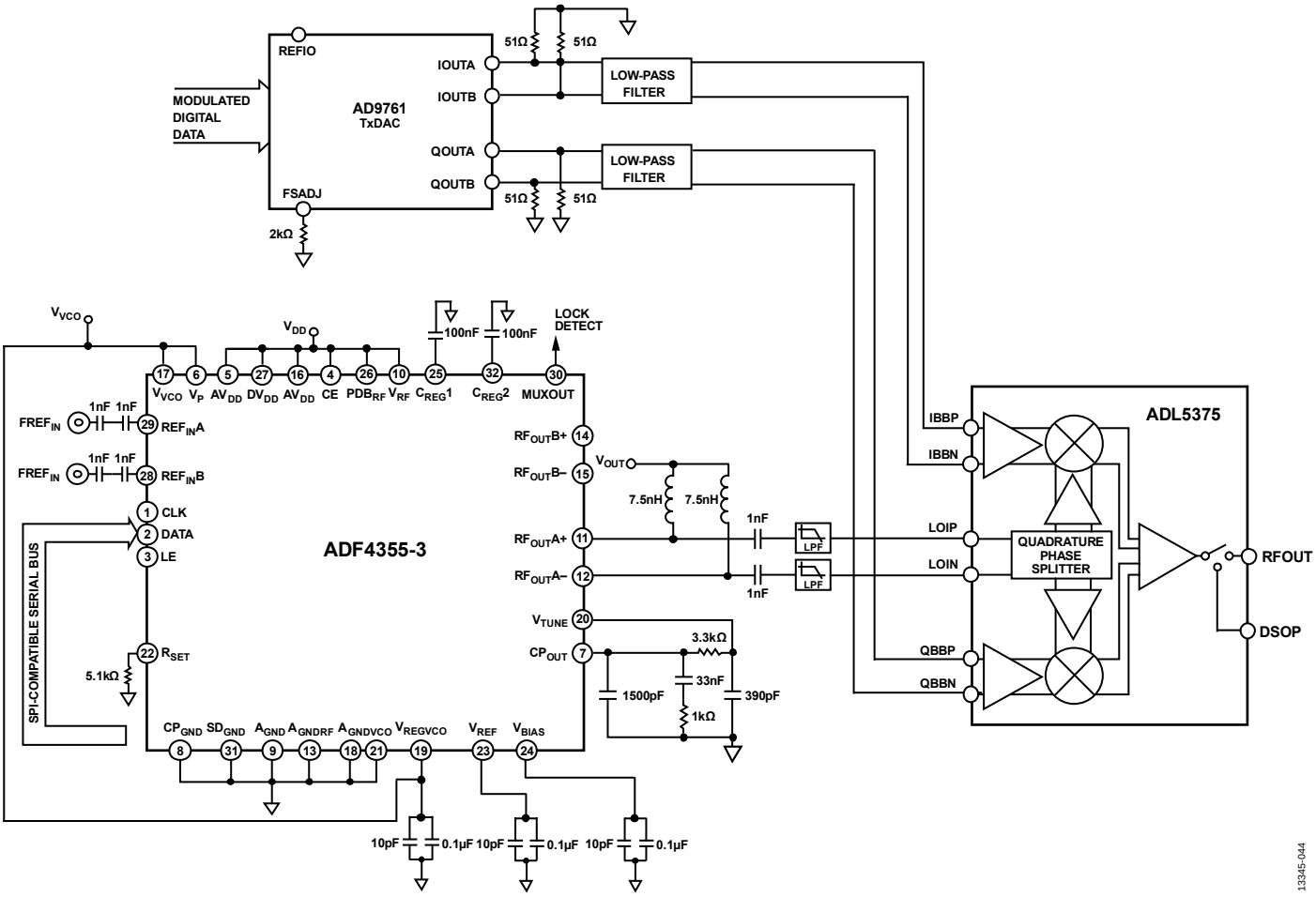

Figure 40. Direct Conversion Modulator

POWER SUPPLIES

The ADF4355-3 contains four multiband VCOs that together cover an octave range of frequencies. To ensure best performance, it is vital to connect a low noise regulator, such as the ADM7150, to the V_{VCO} pin. Connect the same regulator to V_{VCO}, V_{REGVCO}, V_{RF}, and V_P.

For the 3.3 V supply pins, use one or two ADM7150 regulators. Figure 42 shows the recommended connections.

PRINTED CIRCUIT BOARD (PCB) DESIGN GUIDELINES FOR A CHIP-SCALE PACKAGE

The lands on the 32-lead lead frame chip-scale package are rectangular. The PCB pad for these lands must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center each land on the pad to maximize the solder joint size.

The bottom of the chip-scale package has a central exposed thermal pad. The thermal pad on the PCB must be at least as large as the exposed pad. On the PCB, there must be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern. This clearance ensures the avoidance of shorting.

To improve the thermal performance of the package, use thermal vias on the PCB thermal pad. If vias are used, incorporate them into the thermal pad at the 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. of copper to plug the via.

For a microwave PLL and VCO synthesizer, such as the ADF4355-3, take care with the board stack-up and layout. Do not use FR4 material because it is too lossy above 3 GHz. Instead, Rogers 4350, Rogers 4003, or Rogers 3003 dielectric material is suitable.

Take care with the RF output traces to minimize discontinuities and ensure the best signal integrity. Via placement and grounding are critical.

OUTPUT MATCHING

The low frequency output can simply be ac-coupled to the next circuit, if desired; however, if higher output power is required, use a pull-up inductor to increase the output power level.

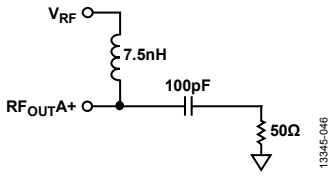

Figure 41. Optimum Output Stage

When differential outputs are not needed, terminate the unused output or combine it with both outputs using a balun.

For lower frequencies below 2 GHz, it is recommended to use a 100 nH inductor on the $RF_{OUT}A+/RF_{OUT}A-$ pins.

The $RF_{OUT}A+/RF_{OUT}A-$ pins are a differential circuit. Provide each output with the same (or similar) components where possible, such as the same shunt inductor value, bypass capacitor, and termination.

The auxiliary frequency output, $RF_{OUT}B+/RF_{OUT}B-$, can be treated the same as the $RF_{OUT}A+/RF_{OUT}A-$ output. If unused, leave both $RF_{OUT}B+/RF_{OUT}B-$ pins open.

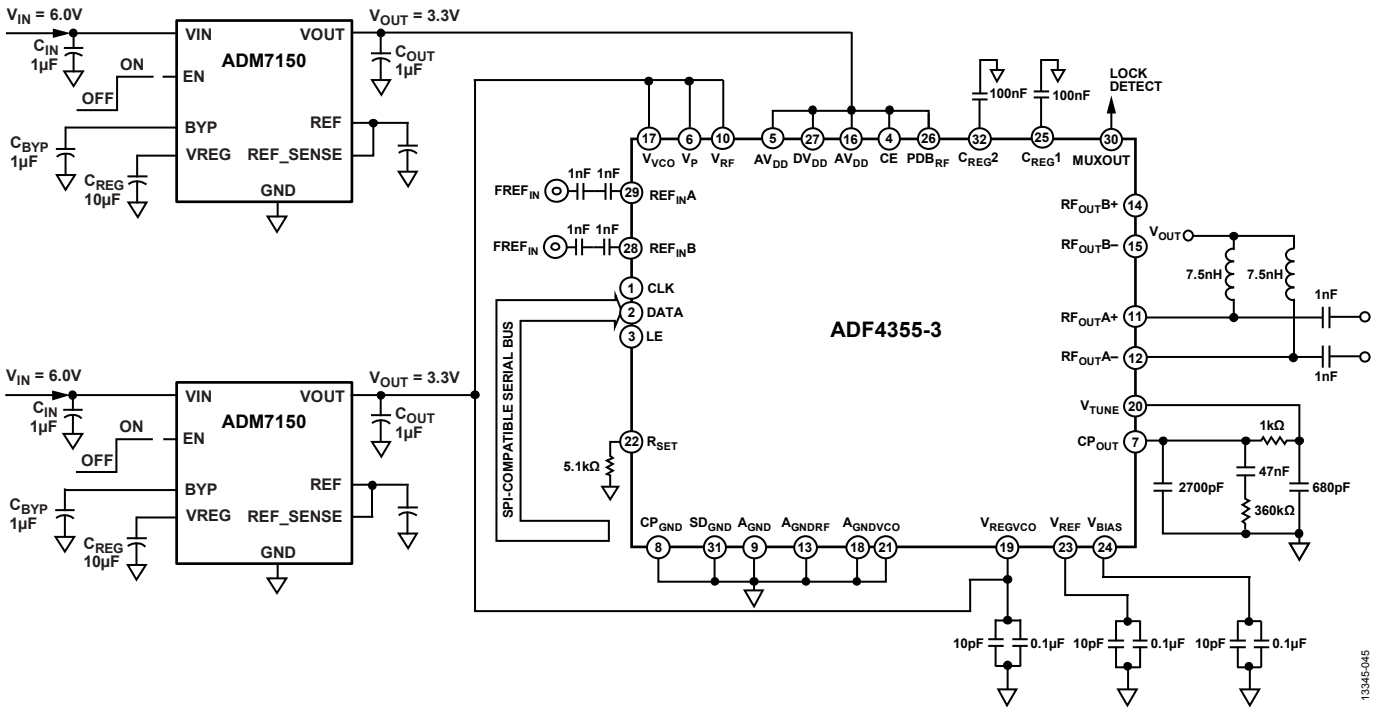

Figure 42. Power Supplies

OUTLINE DIMENSIONS

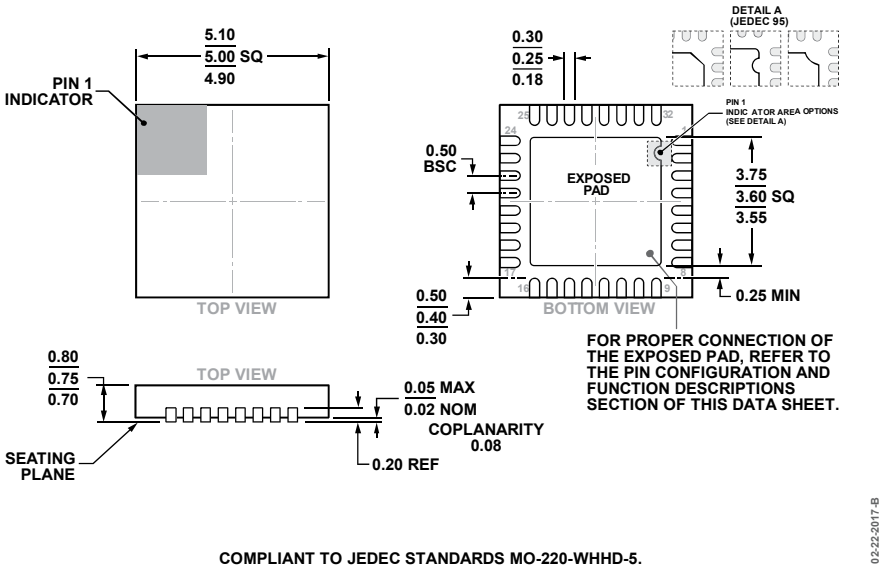

Figure 43. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4355-3BCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADF4355-3BCPZ-RL7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EV-ADF4355-3SD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

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D13345-0-8/17(B)