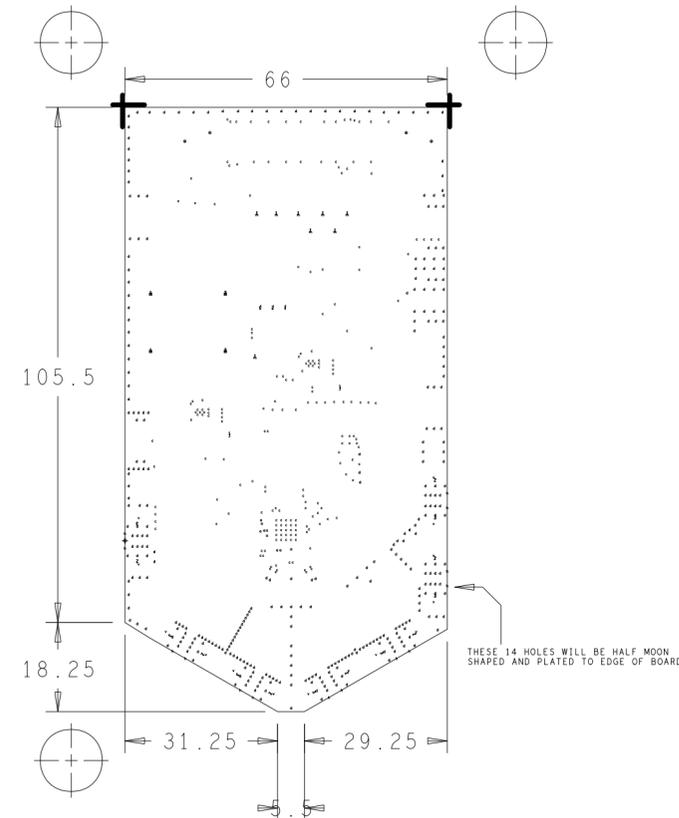


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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	04SEP17	S.BROOKES

PLATED: +/- 0.07mm  
 HOLE TOLERANCE  
 UNLESS SPECIFIED  
 NON PLATED: +/- 0.05mm



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	FINISHED_SIZE	PLATED	QTY
.	0.2032	PLATED	9 MAX TOL
.	0.254	PLATED	199 MAX TOL
.	0.4064	PLATED	345 MAX TOL
.	0.9906	PLATED	14 MAX TOL
.	1.016	PLATED	5
.	1.6002	PLATED	8
.	1.905	PLATED	4
.	2.1082	PLATED	14
.	0.7112	NON-PLATED	1
.	1.0922	NON-PLATED	1
.	3.175	NON-PLATED	2

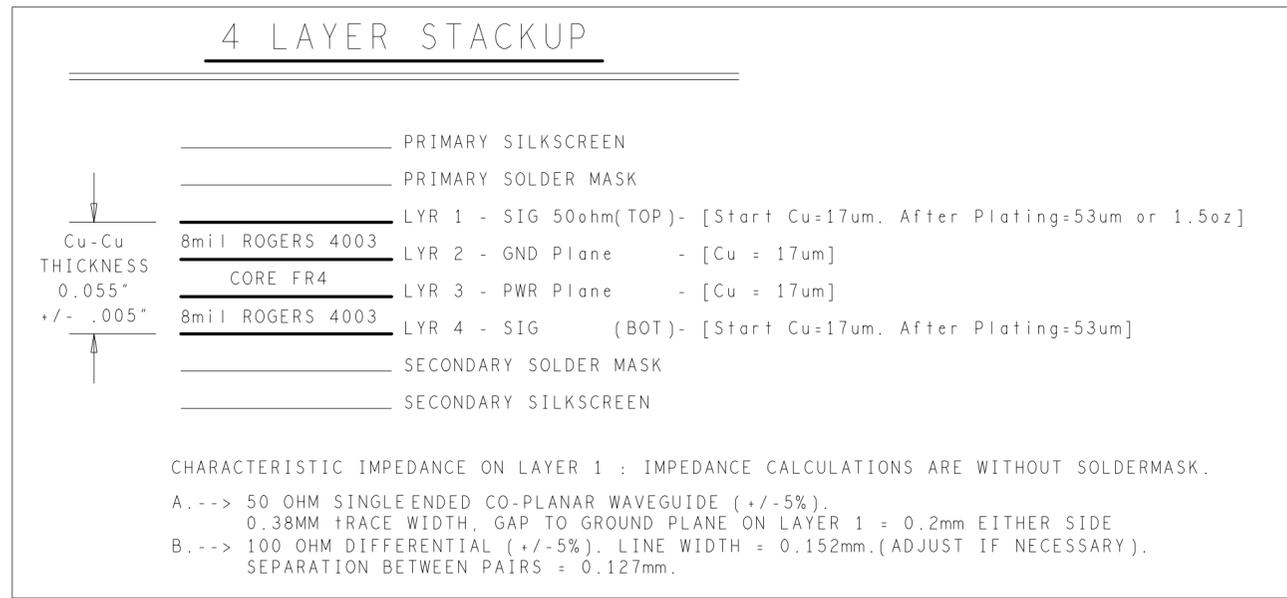
- NOTES:
- ACCEPTABILITY; PER ANALOG DEVICES, INC. SPECIFICATION TST00115 LATEST REVISION.
  - MATERIALS; ROGERS 4003(8 MILS) AND RF4 COMPOSITE FOR RF BUILD. SEE LAYER STACK-UP FOR MORE DETAIL.ESISTANT.
  - BONDING AGENT; PREIMPREGNATED B STAGE EPOXY GLASS CLOTH IN ACCORDANCE WITH IPC-L-109 (LATEST REV.).
  - CLADDING; EXTERNAL LAYERS 1/2 OZ. AFTER PLATING 53UM TOTAL. INTERNAL SIGNAL LAYERS 1 OZ COPPER. INTERNAL PLANE LAYERS 1 OZ COPPER.
  - SOLDER MASK; SHALL BE LIQUID PHOTOIMAGABLE (LPI) APPLIED ON BOTH SIDES OVER BARE COPPER AND SHALL MEET IPC-SM-840 (LATEST REV.) CLASS 3.
  - SILK SCREEN; SHALL BE PERMANENT NON-CONDUCTIVE EPOXY INK, COLOR WHITE.
  - U.L. RATING; 94VO MINIMUM. WAIVED FOR ROGERS MATERIAL.

- FABRICATION:
- REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
  - UNDIMENSIONED HOLES TO BE LOCATED WITHIN +/- .005 OF THEIR TRUE POSITION WITH RESPECT TO ARTWORK.
  - PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN .001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
  - HOLE DIAMETERS APPLY AFTER PLATING.
  - FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL, INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
  - MINIMUM DESIGN LINE WIDTH IS .008 INCH.
  - MINIMUM DESIGN SPACING IS .008 INCH.
  - BOARD/PANEL MUST MEET IPC-A-600 (LATEST REV.) CLASS 2 FOR FLATNESS.
  - MFGR. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED; A. U.L. CODE(N/A) D. MFGR. LOGO - DESIGNATED AREA, B. DATE CODE (STAMP) E. SUCCESSFUL ELECTRICAL BOARD TEST, C. FLAMMABILITY RATING F. LOT NUMBER - DESIGNATED AREA.
  - NON-FUNCTIONAL PADS MAY BE REMOVED FROM INNER SIGNAL LAYERS AT MFGR. DISCRETION.
  - IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFGR. MAY TEAR DROP PADS TO MAINTAIN ANNULAR RING AT PAD TO CIRCUIT INTERFACE ONLY AND MUST INSURE ELECTRICAL INTEGRITY. REPAIRS PER IPC-R-700 ARE ALLOWED.
  - MODIFICATIONS TO THE ARTWORK, OTHER THAN THOSE DESCRIBED ON THE FABRICATION DRAWING, ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
  - SURFACE FINISH TOP AND BOTTOM IS ENIG.
  - FINISHED BOARD MUST BE ROHS COMPLIANT.
  - NOTE THE 16 HOLES AT THE EDGE OF THE BOARD THAT WILL BE A HALF MOON AND PLATED.
  - NOTE THE TOLERANCE ON THE THICKNESS IS CRITICAL BECAUSE OF THE SIDE LAUNCH SMA'S. THE BOARD MUST NOT BE ABOVE 0.061" THICK.

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4 LAYER STACKUP



PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 -- 2 .XXX -.005 .XXXX -.0050	APPROVAL EVAL ENGINEER IAN COLLINS	DATE 28MAY18	ANALOG DEVICES WWM DIVISION RAHEEN INDUSTRIAL PARK LIMERICK IRELAND
	HARDWARE SERVICES PAT SHEAHAN	28MAY18	
MATERIAL	CHECKED IAN COLLINS	28MAY18	TITLE FABRICATION EV-ADF4371SD1Z
	APPROVED IAN COLLINS	28MAY18	
FINISH	PCB DESIGN ENGINEER PAT SHEAHAN	28MAY18	SIZE 24355
DO NOT SCALE DWG	SCALE 1/1	DRAWING NUMBER 09-049338	REV A
		SHEET 1 OF 2	

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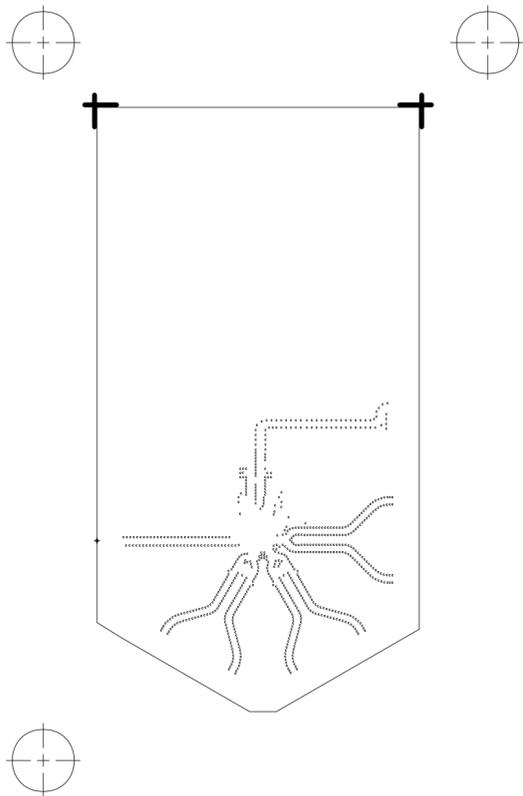
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	04SEP17	S. BROOKES



DRILL CHART: TOP to GROUND			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	FINISHED_SIZE	PLATED	QTY
.	0.254	PLATED	696

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PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX - .010 -- 1/32 -- 2 .XXX - .005 .XXXX - .0050	APPROVAL EVAL ENGINEER IAN COLLINS	DATE 28MAY18	 WWM DIVISION RAHEEN INDUSTRIAL PARK LIMERICK IRELAND
	CHECKED IAN COLLINS	28MAY18	
MATERIAL	APPROVED IAN COLLINS	28MAY18	TITLE FABRICATION EV-ADF4371SD1Z
	PCB DESIGN ENGINEER PAT SHEAHAN	28MAY18	
FINISH			SIZE FSCM NO DRAWING NUMBER REV 24355 09-049338 A
DO NOT SCALE DWG		SCALE 1/1	SHEET OF 2

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