Using an External VCO with the ADF7010
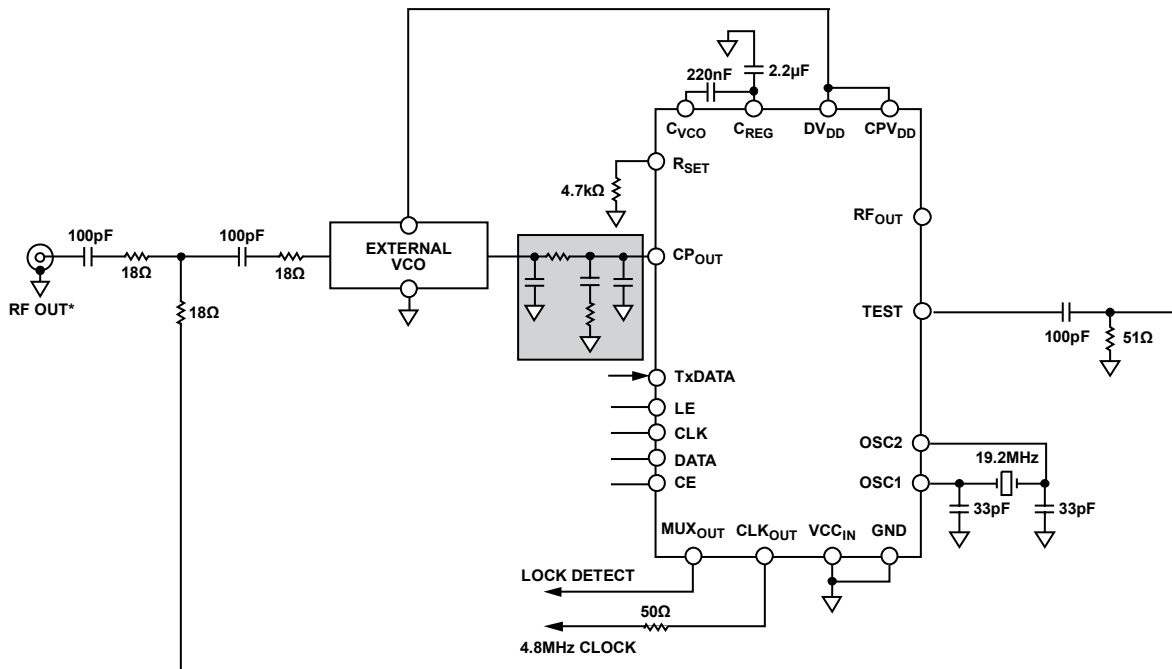
by Austin Harney

INTRODUCTION

An external VCO can easily be used in conjunction with the ADF7010 transmitter. This allows operation up to 1.4 GHz with superior phase noise and spurious performance. The test pin on the functional schematic is connected via a MUX to the input of the prescaler. The external VCO can be connected between the loop filter and the test pin.

REASONS FOR USING AN EXTERNAL VCO

1. Frequency of Operation:
    The internal VCO on the ADF7010 is limited to 902 MHz to 928 MHz operation over temperature. Using an external VCO allows the user select any frequency up to 1.4 GHz with a VCO output signal of > −5 dBm.

2. Phase Noise Performance:
    A standalone VCO has significantly better phase noise than an integrated one. The internal spiral inductors on the ADF7010 have a much lower Q than an external discrete inductor.

Phase noise at 1 MHz offset from 900 MHz carrier:
    ADF7010: −112.5 dBc/Hz
    Sirenza VCO190-902T: −155 dBc/Hz

Additional phase noise performance allows for very narrow channel operation while meeting the edge band signal level requirements. Good phase noise performance out-of-band allows better selectivity in a receiver, where the ADF7010 was used for LO generation.

3. Spurious Performance:
    The proximity of PLL blocks to each other internally on a fully integrated transmitter solution causes undesired coupling of unwanted components onto the output spectrum. These spurious components can make it difficult to meet regulatory standards at high power. An external VCO provides significant isolation between the PLL dividers and the VCO output, resulting in significantly cleaner output spectrums.

*THIS MIGHT BE CONNECTED TO A PA STAGE OR DIRECTLY TO AN ANTENNA.

NOTES
1. ASSUMING THE PA IS NOT BEING USED IT SHOULD BE DISABLED IN SOFTWARE.

Figure 1. Application Schematic

APPLICATION INFORMATION

The external VCO is connected following the loop filter and before the test pin. ADIsimPLL™ is an invaluable tool in the design and simulation of these loop filters.

The 18 Ω/100 pF combination is designed to split the VCO output RF power equally between the system output and the test pin. By altering the resistor/capacitor combination more or less power can be fed back to the N-divider. Feeding extra power back to the test pin can allow the PLL to lock to higher frequencies, and give greater margin in terms of the minimum input signal. Care should be taken so as not to feed >5 dBm output power into the test pin, as this reduces the effective range of the N-dividers.

In software, the external VCO mode is enabled by simply powering down the internal VCO.

The internal PA can be used with an external VCO; however, it does cause significantly higher spurious. A cheap external discrete PA stage is more effective at amplifying the VCO output power.

DESIGNING LOOP FILTERS TO USE WITH AN EXTERNAL VCO

ADIsimPLL can be downloaded for free from the ADI PLL Web page. To design and simulate a loop filter for the ADF7010 with external VCO, you should follow the following procedure.

1. <screen 1> Select the option "PLL should produce a range of output frequencies."

2. "Specify the PFD frequency" option should be checked.

3. <screen2> Input the frequencies required and the PFD you wish to use. The maximum PFD frequency is the crystal frequency, and results in the best phase noise. Spurious components are a few dB higher for a higher PFD.

4. <screen 3> Select the ADF4153 as the PLL to use. The ADF7011 is not available yet in this mode.

5. <screen5> Enter required VCO parameters, based on VCO module parameters.

6. <screen7> Hit the next button and select the loop filter as shown in applications diagram. (3-pole integrator).

7. Once the <finish> button has been pressed, under CHIP > PFD, change the R_{SET} resistor to 2.5 kΩ and select a charge pump current of 2.02 mA. Note that the level of phase noise is 8 dB worse on the ADF7010/ADF7011 compared to the ADF4153. All other measurements including lock time, and loop filter BW are accurate.
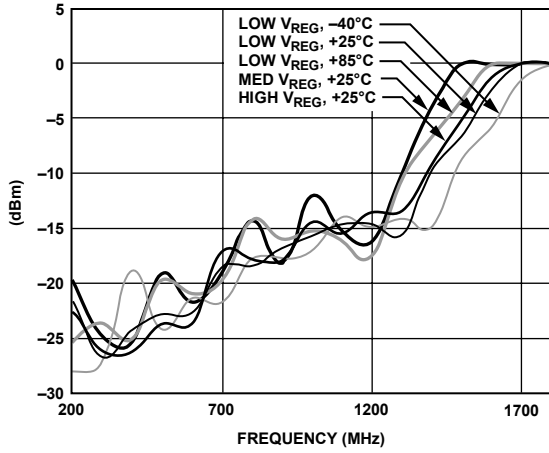
PERFORMANCE PLOTS

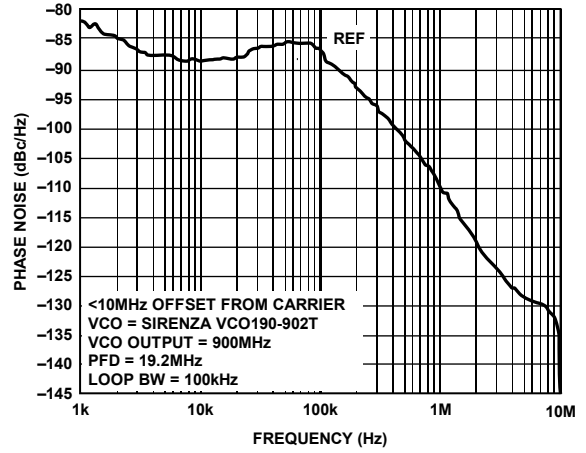*Figure 2. N-Divider (Input Sensitivity)*
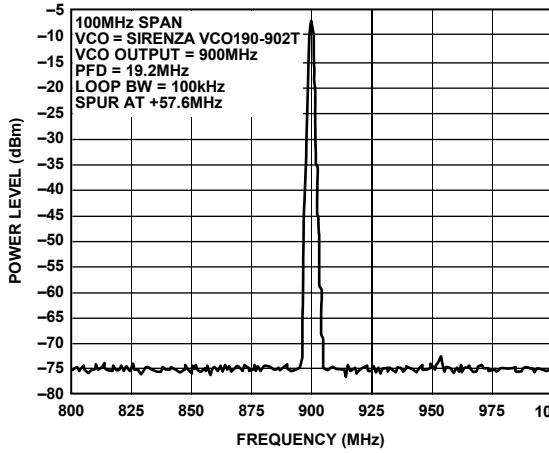

Figure 4. Phase Noise Performance

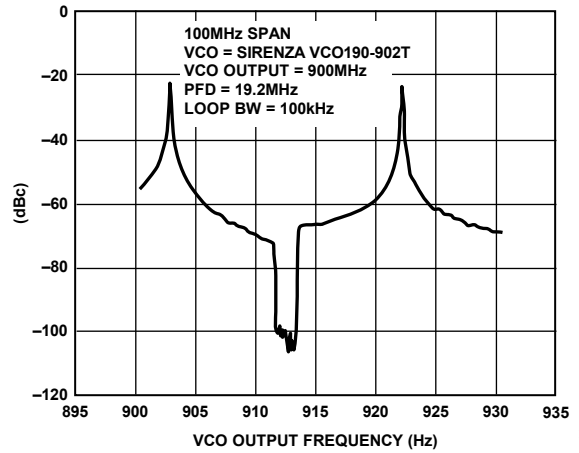*Figure 3. Output Spectrum*

Figure 5. Spurious Response

APPLICATION GUIDELINES

LAYOUT TIPS WHEN USING AN EXTERNAL VCO

- Ensure that tracks from charge pump to VCO input are kept short. The tracks from the VCO output to the test pin should be kept as short as possible.

- A 22 µF capacitor and a 10 pF capacitor should be used to decouple the supplies of the VCO. These capacitors should be kept as close as possible to the VCO.

- All supplies of the ADF7010 should be decoupled with 100 nF and 10 pF capacitors. These capacitors should be as close to the supply pins as possible.

ADDITIONAL GUIDELINES

- The mode to enable the external VCO is selected by disabling the internal VCO. The PA should also be turned off in software.

- Examine the sensitivity plot in Figure 2. The minimum input power as per the plot should have at least 3 dB of margin, to ensure reliable N-divider performance over all supplies and temperatures.

- Beatnote spurious are elements of the nearest integer channel coupling onto the RF output. This is an integral part of any fractional-N design. The spurious levels are attenuated by the loop filter, so having a low filter BW reduces these. Avoid operating on an integer channel. Careful crystal selection reduces the levels to the point where it is swamped by the modulation.

- Beatnote spurious level can be traded off against phase noise using the fastlock mode in the software. This activates a bleed current, which linearizes the charge pump.

- There will be a spur at VCO/2. This is a prescaler spur and is typically <−70 dBc.

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