AN-1182
APPLICATION NOTE

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Understanding and Optimizing the AFC Loop on the ADF7021 for Minimum Preamble

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ACRONYMS AND ABBREVIATIONS

The following acronyms and abbreviations are used in this application note:

AFC—Automatic Frequency Control

CDR—Clock and Data Recovery

DPL—Data Packet Length

LO—Local Oscillator

MI—Modulation Index

PER—Packet Error Rate

PI—Proportional Integral

RLL—Run Length Limit

Rx—Receive

SWD—Synch Word

Tx—Transmit

INTRODUCTION

Remote transceivers, within radio communication networks, use their own independent clock sources. They are, thus, susceptible to frequency errors. When a transmitter initiates a communication link, the associated receiver needs to correct these errors during the preamble phase of the data packet to ensure correct demodulation. An effective design block that performs this correction is an automatic frequency control (AFC) loop. This application note provides information on how AFC is implemented and optimized on the ADF7021, ADF7021-N, and ADF7021-V.

Because latency and battery life are critical for remote applications, designers are motivated to reduce the settling time required to correct a frequency error. The ADF7021 series radios typically require up to 15 bytes of preamble to correct a frequency error. There are methods to reduce this number to 4 to 6 bytes.

This application note outlines the various parameters that affect the response of the AFC loop and presents the recommended settings that enable fast settling time for specific use cases while detailing the trade-offs in performance that are incurred.

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REVISION HISTORY

3/13—Revision 0: Initial Version

QUICK SETTINGS

Modulation Index (MI), which provides a metric relating frequency deviation to data rate, is a key factor for optimizing settling time.

$$MI = \frac{2 \times Frequency\ Deviation\ (Hz)}{Data\ Rate\ (bps)}$$

Table 1 contains the settings for the recommended default setup. The default settings on the ADF7021 ensure the best possible receiver sensitivity with AFC enabled for all modulation indexes (MI). Table 2 contains the settings for optimum settling time. Note that preamble lengths as low as 4 bytes are possible with these settings. Table 2 settings are only recommended for systems with MI ≥ 1.

The trade-off for enabling faster AFC loop settling is a degradation in receiver sensitivity. There will be a 1dB to 2 dB degradation in receiver sensitivity performance with the settings in Table 2 compared to the default settings in Table 1. To achieve fast settling with MI < 1, follow the steps outlined in Figure 7 while accounting for other factors and their effects, which are explained in detail in this application note.

Table 1. Default Settings, Optimum Receiver Sensitivity

KI	11
KP	4
Peak	default
Leak	default
Required Preamble	8 to 14 bytes

Table 2. Optimized Settings, Fast Settling Time (MI ≥ 1)

KI	8
KP	2
Peak	0
Leak	0
Required Preamble	4 to 6 bytes

CLOCK AND DATA RECOVERY (CDR)

An understanding of the CDR algorithm is beneficial when considering the response of the AFC loop. The ADF7021 radio modems implement the CDR algorithm by oversampling the data output from the data Slicer (see Figure 1) at 32× the transmitted data rate. When bit transitions on the data are detected, the CDR algorithm is updated and the Rx clock is adjusted +1/32, 0 or −1/32 of a bit time. Note that 16-bit transitions on the data are required for the CDR algorithm to achieve lock. Application Note AN-915, describes this in more detail.

To achieve fast CDR lock, a 1010… preamble sequence is preferable. For best PER performance the mark space ratio of the 1010… sequence at the Slicer output should be as close as possible to 50:50 during CDR acquisition. When a frequency error is present, the mark space ratio will not be 50:50. Therefore, AFC must be carried out before CDR acquisition can occur.

Figure 1 shows the average response of the local oscillator (LO) to a 1010… preamble sequence with the optimized settings in Table 1 and the default settings in Table 2. At time t = 0 there is a 5 kHz frequency error. With the optimized settings implemented, at t = 16, the frequency error has been minimized and the CDR acquisition begins.

Note there is an error about zero on the LO between t = 16 and t = 32. The error present is referred to as the LO steady state error. The magnitude of this error increases as the AFC loop response speed is increased. This is highlighted by the difference in steady state error between the optimized and default settings in Figure 1. The degree of error that is tolerated by the CDR algorithm will vary with MI. For example, systems with a MI ≥ 1 can tolerate the steady state error on the red trace. Systems with MI < 1 require a slower AFC response, ensuring a lower steady state error.

In Figure 1, at t = 32, CDR acquisition is complete. At this time, the Rx clock is synchronized with the Tx data rate and the center of the Rx eye is sampled. Only after the CDR algorithm achieves lock, can a certain amount of LO drift, due to consecutive 1s or 0s on the synch word (SWD), be tolerated. This application note provides more detail on this topic later.

The trade-off between the rise time and the steady state frequency error of the LO during preamble is a primary consideration when selecting AFC settings.

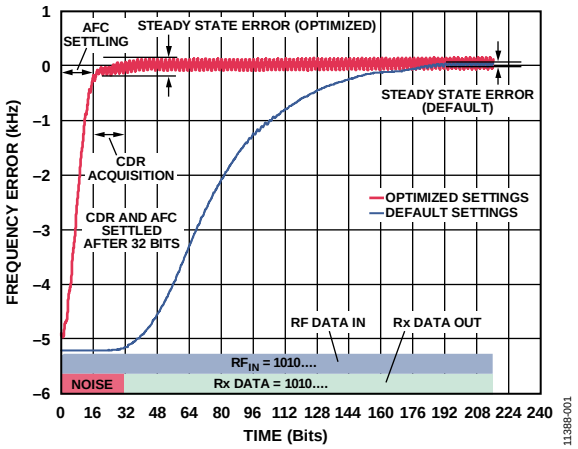

Figure 1. LO Steady State Error

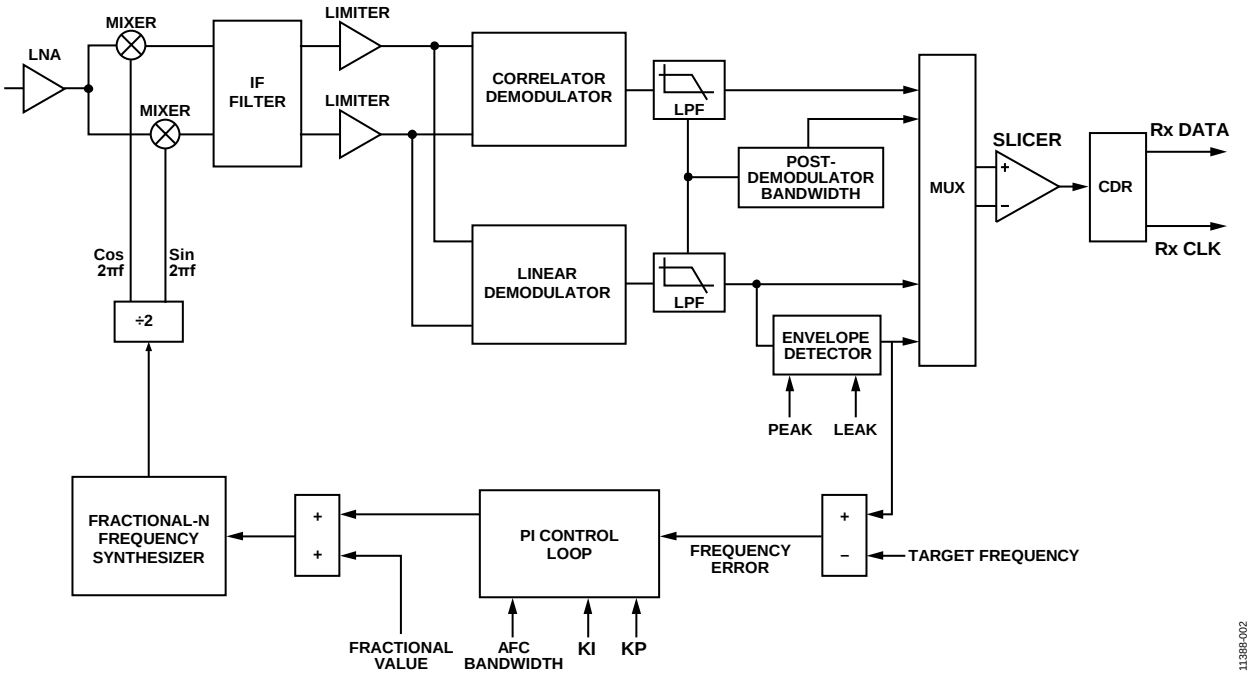

Figure 2. Functional Block Diagram

AFC LOOP OVERVIEW

Figure 2 shows a block diagram of the AFC loop.

When AFC is enabled, the envelope detector is used to estimate the center frequency of the received signal. Ideally, this is performed on a consecutive 1010... preamble sequence. This estimation of the received signal is then compared to the target frequency and an error signal is generated.

The error signal is passed through a proportional-integral (PI) control loop and the output adjusts the Fractional-N Frequency synthesizer. The overall AFC loop response is dominated by a combination of the envelope detector and PI control loop. Their effect is discussed in more detail in the following section.

ENVELOPE DETECTOR

The function of the envelope detector is to track the center frequency (the carrier) of the received signal in the presence of noise while tolerating received data of variable run length limit (RLL). The time response of the envelope detector is determined by ED_PEAK_RESPONSE and ED_LEAK_FACTOR.

Figure 3 shows the average response of the LO to a 1010… preamble sequence with the default peak/leak settings and with the parameters set to zero. Initially the LO is biased to an offset of −5 kHz.

Note the initial response (between t = 0 and t = 32) is considerably faster with peak and leak settings set to zero, but the slopes of the traces are similar, since this is dominated by the PI control loop. The trade-off is an increase in LO steady state error.

The ED_PEAK_RESPONSE and ED_LEAK_FACTOR is set to zero by setting Register14_DB[27:31] = 0 and setting Register15_DB[4:7] = 9.

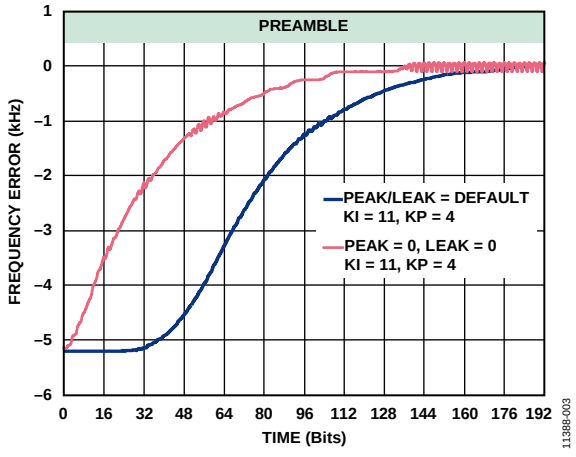

Figure 3. Effect of Peak and Leak Settings

PI CONTROLLER

The proportional and integral gain of the AFC loop is controlled in Register10_DB[17:23]. The response is dominated by the integrated gain component KI. Figure 4 and Figure 5 show the effect of KI and KP on the response of the LO to a 1010… preamble signal. As KI is reduced, the rise time is reduced but some overshoot begins to occur.

It is clear from Figure 5 that the effect of the proportional gain component, KP, is minimal compared to KI. However, reducing to a value of KP = 2 reduces the overshoot caused by decreasing KI. Although it is a marginal improvement, this is found to improve the PER when a short preamble length is used.

To ensure the stability of the AFC loop, it is recommended to set KI ≥ 8 and KP ≥ 2.

The red trace in Figure 5 shows the fully optimized response of the LO. These are the same settings as used in Table 2. With these settings, a steady state is achieved after approximately 2 bytes of preamble. The CDR loop requires 16 bit transitions to consistently synchronize with the received signal requiring an additional 2 bytes of preamble.

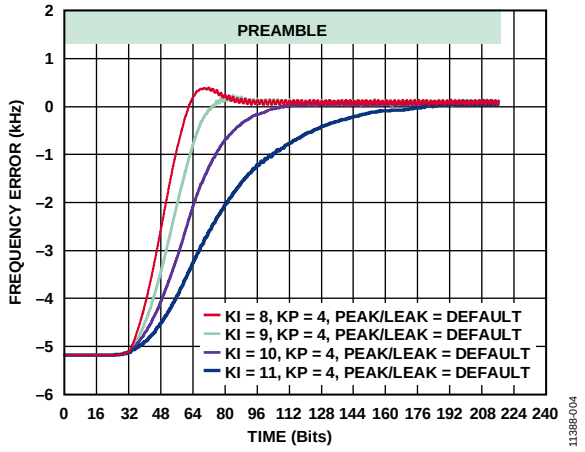

Figure 4. Effect of KI

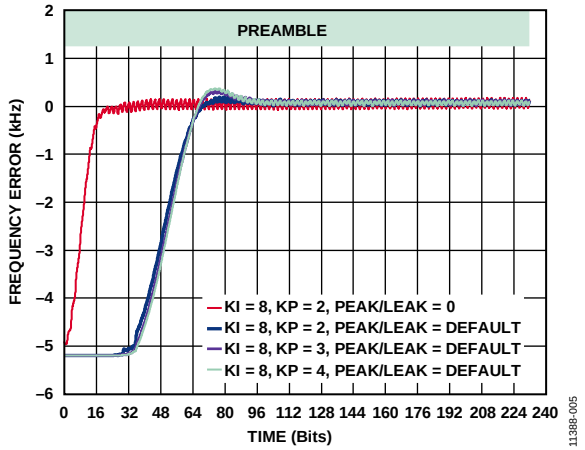

Figure 5. Effect of KP

EFFECT OF SWD SELECTION

As the response of the AFC loop is increased, LO drift on the SWD can be significant. Figure 6 shows the response of the LO to a typical SWD. The AFC loop is locked on successful reception of the SWD. LO drift is observed at Bit 160 when the SWD is received. When RLL = 5 and the loop is optimized for fast response, the drift can be as large as ±1 kHz. As the CDR is sampling the center of the bit, some LO drift on the SWD portion of the packet can be tolerated at high Rx power. However, depending on the magnitude of the LO drift, receiver sensitivity may be degraded. For this reason, it is recommended to minimize the RLL of the SWD. The locking position of the AFC loop in Figure 6 highlights the need for a dc-balanced final 4 bits of the SWD.

It is recommended to lock the AFC loop on successful reception of a SWD. This ensures that a long RLL can be tolerated in the payload portion of the packet. This is carried out on-chip by setting Register12_DB[4:5] = 2 and keeping the AFC loop locked for a specified time data packet length (DPL) from the end of the SWD. DPL is configured in Register12_DB[8:15].

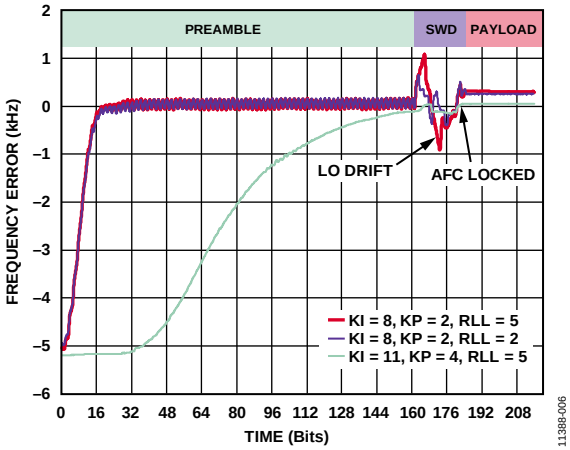

Figure 6. Effect of SWD RLL

OTHER CONSIDERATIONS

As the occupied bandwidth of the received signal approaches the bandwidth of the receiver IF filter, the sensitivity of the AFC loop can be degraded. In this case, a longer preamble may be required to recover the signal.

There is a data rate tolerance requirement on the ADF7021. The actual transmitted data rate must be within ±2 % of the desired receiver data rate. This is described in more detail in the Application Note AN-915.

Reference oscillator tolerance is important when considering the AFC loop. An error on the crystal results in an error on the operating RF frequency. This error increases proportionally with operating frequency. For example, a 5 ppm error on a 10 MHz crystal generates a 50 Hz error at the fundamental crystal frequency. At 868 MHz, this error is multiplied to 4.34 kHz. Compare this to 433 MHz where the RF error is 2.165 kHz.

The AFC readback function cannot be used with AFC on.

Receiver sensitivity may be improved by using a shorter SWD or setting match error tolerance > 0. This is set in Register 11_DB[6:7]. There is a trade off with false SWD detects to find an optimum setup. Note that false SWD detects lock the AFC loop for a programmable duration DPL when the lock threshold after next SWD setting is enabled. ADIsimSRD Design Studio provides a calculator to determine the probability of false SWD detects. This is available for download from the ADF7021 product page.

Bypassing the on-chip CDR could yield further improve-ments in terms of receiver sensitivity and CDR settling time. This is achieved by taking the slicer output to the host microprocessor and implementing a custom CDR algorithm. The slicer data can be output on the TxRxData pin by setting Register15_DB[4:7]. With on-chip CDR bypassed, the AFC loop response speed can be increased further by increasing the speed of the CDR clock.

EXAMPLE CONFIGURATIONS

Table 3 shows the measured Rx sensitivity performance when using the settings in Table 4. The receiver sensitivity quoted is the worst case across the range of frequency errors tested. The measurements in Table 1 were taken with RLL = 2 on the SWD. This is not a limitation and longer run lengths may be used, if required.

Table 3. Example Performance

Data Rate (kbps)	Fdev (kHz)	Sensitivity 1% PER (dBm)	Preamble (Bytes)
1.2	1.2	−116	4
2.4	2.4	−115	4
2.4	1.2	−114.5	4
4.8	4.8	−114	4
4.8	2.4	−113.5	4
9.6	4.8	−112	5

Table 4. Configuration to Achieve Performance in Table 3

XTAL (MHz)	19.68
AFC BW (kHz)	± 4.5
Freq Error (kHz)	± 4
IFBW (kHz)	18.5
Demodulator	Correlator
Modulation	GFSK (0.5)
Lock Thresholds on SWD	Yes
SWD	D4C95A
Match Error Tolerance	0
KI	8
KP	2
Peak	0
Leak	0

STEPS TO OPTIMIZE THE AFC LOOP FOR MINIMUM PREAMBLE

The configurations suggested in this application note may not be suitable for certain systems, including those where MI < 1. Figure 7 contains a suggested flowchart for optimizing the loop for minimum preamble for such systems. When undertaking this approach, it is assumed that the user has a measurement setup capable of performing a PER test.

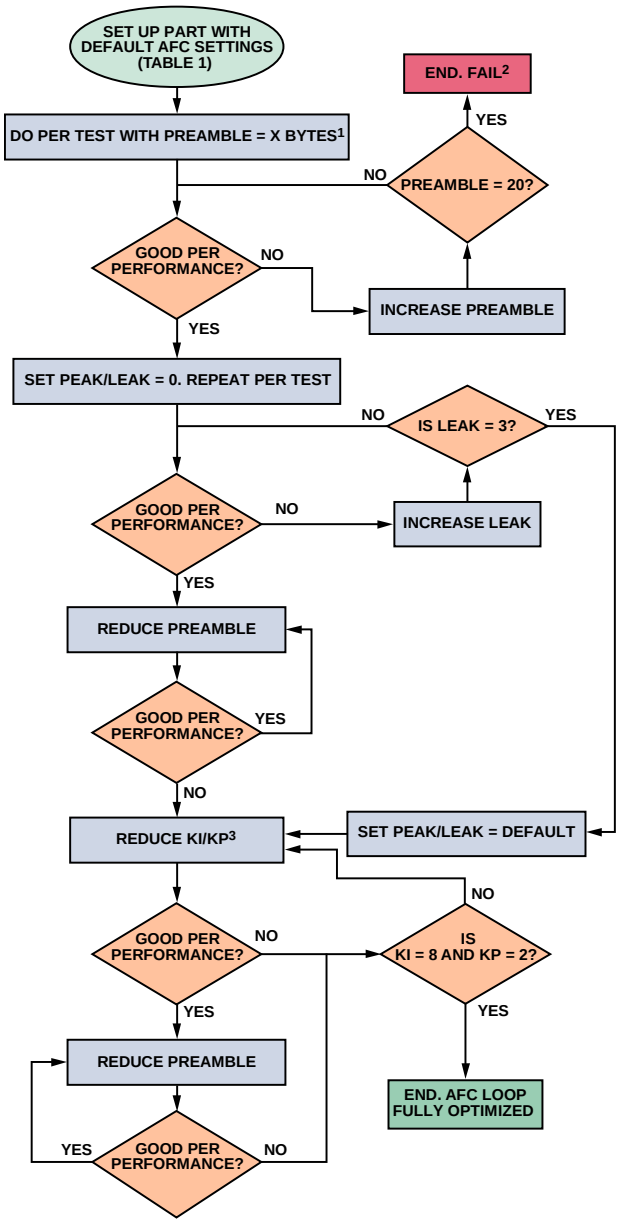

Figure 7. Recommended Steps to Find Optimum AFC Settings

Figure 7 includes three numbered labels (1, 2, and 3). For label 1, note that for setups where AFC optimization is the goal, set X to the current value of the preamble being used in the system and follow the steps. Where AFC is being switched on, X = 12 bytes is a recommended starting point. In both instances, the preamble may need to be initially increased before eventually optimizing.

Label 2 indicates that some other component of the system is causing incompatibility with AFC. This cannot be overcome by changes to the AFC loop or by increasing preamble.

For Label 3, it is recommended to reduce KI first since its effect on the settling speed is more substantial than KP. See the PI Controller section for more details

NOTES

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