

Evaluating the ADG1519 3.8 Ω On-Resistance, SPDT Switch

FEATURES

- ▶ Asymmetrical supply voltages
 - ▶ VDD = +5 V
 - ▶ VSS = -8 V
- ▶ Parallel interface compatible with 3 V logic

EVALUATION KIT CONTENTS

- ▶ EVAL-ADG1519EBZ evaluation board

DOCUMENTS NEEDED

- ▶ [ADG1519](#) data sheet
- ▶ EVAL-ADG1519EBZ user guide

EQUIPMENT NEEDED

- ▶ DC voltage source
 - ▶ 5 V positive power supply
 - ▶ -5 V to -8 V negative supply
- ▶ Optional digital voltage source: 5 V
- ▶ Analog signal source
- ▶ Method to measure voltage, such as a digital multimeter (DMM)

TYPICAL EVALUATION BOARD SETUP

GENERAL DESCRIPTION

The EVAL-ADG1519EBZ is the evaluation board for the ADG1519, which features a single channel, single-pole, double through (SPDT) switch. The ADG1519 is fully specified for asymmetrical voltage supplies of $V_{DD} = +5 \text{ V} \pm 10\%$ and $V_{SS} = -4.5 \text{ V to } -8.8 \text{ V}$.

Figure 1 shows the EVAL-ADG1519EBZ in a typical evaluation setup. The ADG1519 is soldered to the center of the evaluation board, and two wire screw terminals are provided to connect to each of the source pins and the drain pin. Three screw terminals are used to power the device, with a fourth terminal used to provide an optional logic voltage for the digital control of the ADG1519.

Full specifications on the ADG1519 are available in the product data sheet, which should be consulted in conjunction with this user guide when using the EVAL-ADG1519EBZ.

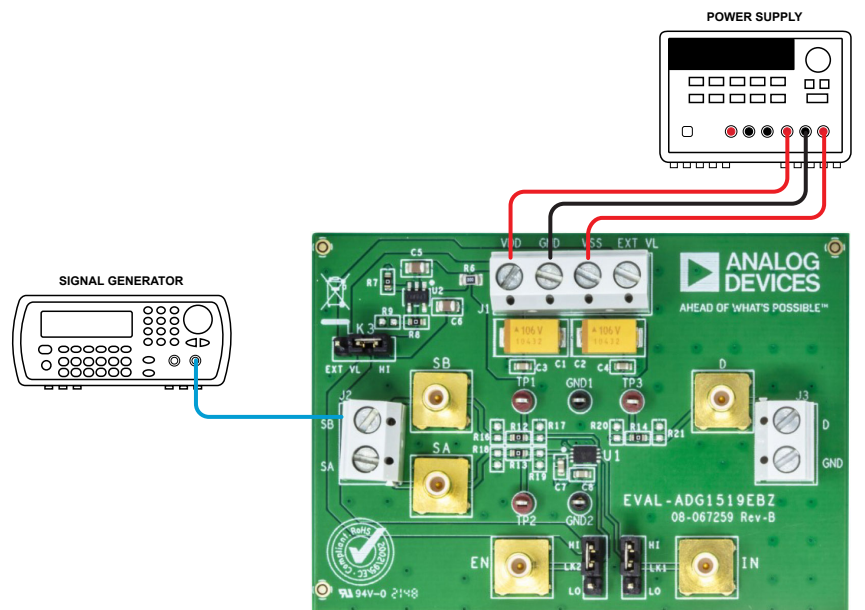


Figure 1. EVAL-ADG1519EBZ (on Right), Power Supply, and Signal Generator

TABLE OF CONTENTS

Features.....	1	Power Supply.....	4
Evaluation Kit Contents.....	1	Input Signals.....	4
Documents Needed.....	1	Jumper Settings.....	5
Equipment Needed.....	1	Link Headers and 0 Ω Resistor.....	5
General Description.....	1	SMB Connectors.....	5
Typical Evaluation Board Setup.....	1	Evaluation Board Schematics and Artwork.....	6
Getting Started.....	3	Ordering Information.....	8
Evaluation Board Setup Procedure.....	3	Bill of Materials.....	8
Evaluation Board Hardware.....	4		

REVISION HISTORY**1/2022—Revision 0: Initial Version**

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG1519EBZ operates independently and does not require any additional evaluation boards or software to operate. An on-board [ADP7142](#) LDO regulator is provided as the digital power supply to manually control the [ADG1519](#).

The J1 connector is used to supply the EVAL-ADG1519EBZ with a dual power supply of +5 V for VDD and -8 V for VSS. If the [ADP7142](#) LDO regulator is not required, remove the R6 resistor and use LK3 to select the EXT_VL input on J1 to supply an alternative digital voltage supply.

To set up the EVAL-ADG1519EBZ to perform a functionality test, connect a power supply to the J1 connector.

LK1 and LK2 controls the digital signals for the switch channel enable and channel select on the ADG1519.

- ▶ With LK2 In Position LO, the switch channels are open and present as an open circuit.
- ▶ With LK2 In Position HI, the switch is enabled and LK1 is used to select between SA and SB. The selected channel presents with a resistance of approximately 3.8 Ω.

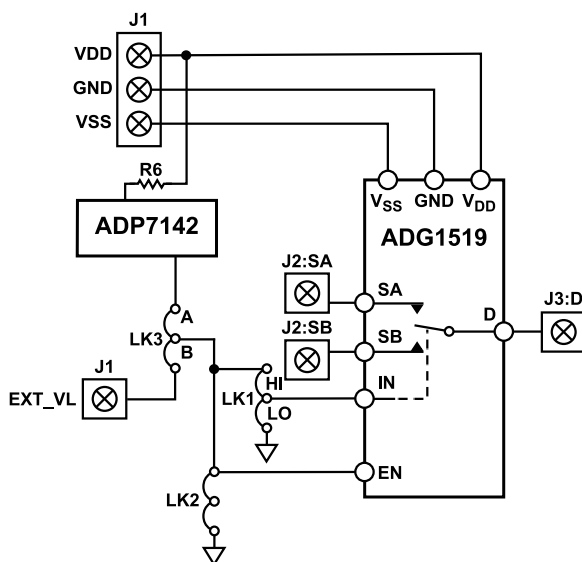


Figure 2. EVAL-ADG1519EBZ Block Diagram

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EVALUATION BOARD HARDWARE

The operation of the [ADG1519](#) is evaluated using the EVAL-ADG1519EBZ. [Figure 1](#) shows a typical evaluation setup where only a power supply and signal generator are required.

[Figure 2](#) shows the block diagram of the main components of the EVAL-ADG1519EBZ.

Using the EVAL-ADG1519EBZ, the ADG1519 is used to pass signals from either the source or drain connectors. See the ADG1519 data sheet for more details.

POWER SUPPLY

Connector J1 provides access to the supply pins of the ADG1519. VDD, GND, and VSS link to the appropriate pins on the ADG1519. For dual-supply voltages, the EVAL-ADG1519EBZ can be powered with +5 V for VDD and –8 V for VSS.

The on-board [ADP7142](#) LDO regulator is provided for the digital control voltage. A secondary voltage source can be connected to the EXT_VL terminal of the EVAL-ADG1519EBZ and be used as the digital control voltage. To use the EXT_VL terminal of the EVAL-ADG1519EBZ, move the LK3 jumper from Position A to Position B.

INPUT SIGNALS

Two 2-pin screw connectors are provided to connect to both the source and drain pins of the ADG1519. Additional Subminiature Version B (SMB) connectors are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can be used to place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can be used to create a simple RC filter.

The ADG1519 uses a parallel interface to control the operation of the switch channel. The switch operation can be manually controlled using the headers on LK1 and LK2, or an external controller can be interfaced directly to the control pins by using the SMB connectors (IN and EN) and removing the link headers on LK1 and LK2.

JUMPER SETTINGS

LINK HEADERS AND 0 Ω RESISTOR

The on-board link headers (LK1 and LK2) can control the [ADG1519](#) manually. [Table 1](#) lists the link headers and resistors and explains how each is used on the EVAL-ADG1519EBZ.

The LK1 and LK2 link headers control the ADG1519 switch channel selection and enable or disable the switch. Place LK2 in Position LO to disable the switch, and place LK2 in Position HI to enable the switch. With the ADG1519 enabled, place LK1 in Position LO to select the SA input, and place LK2 in Position HI to select the SB input.

The R6 resistor connects the VIN pin of the on-board [ADP7142](#) LDO regulator to the EVAL-ADG1519EBZ VDD terminal supply. Remove the R6 resistor to disconnect the LDO input if it is not required.

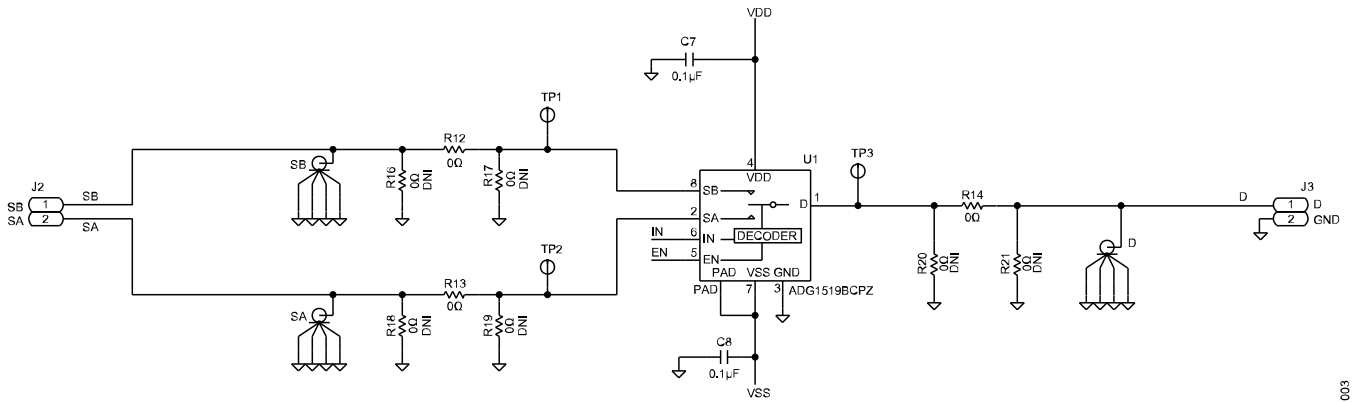
Table 1. Link Headers and Resistor Descriptions

Label	Position	Description
LK1	LO	Select Channel A
	HI	Select Channel B
LK2	LO	Switch Disabled
	HI	Switch enabled
LK3	A	On-board LDO regulator digital voltage
	B	EXT_VL digital voltage
R6	Inserted	ADP7142 Enabled
	Removed	ADP7142 Disabled

SMB CONNECTORS

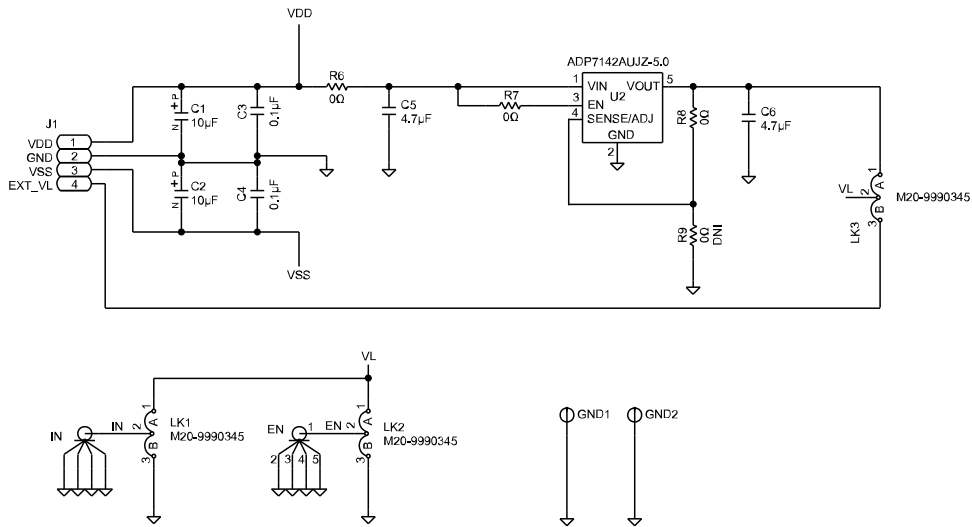
The parallel interface of the ADG1519 can either be controlled manually by using the LK1 and LK2 link headers or accessed by using the IN and EN SMB connectors. To use the SMB connectors, remove the LK1 and LK2 link headers.

EVALUATION BOARD SCHEMATICS AND ARTWORK



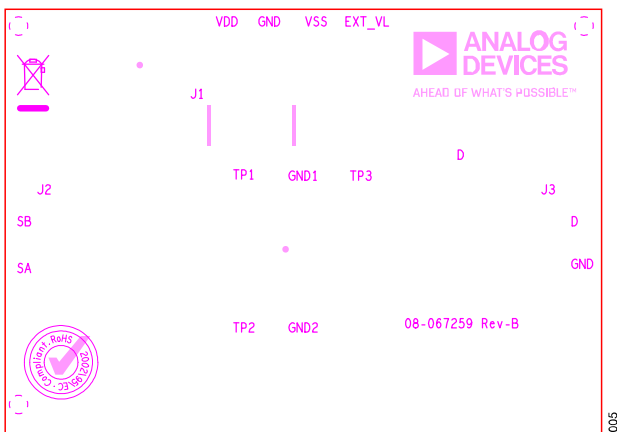
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Figure 3. EVAL-ADG1519EBZ Evaluation Board Schematic—Page 1



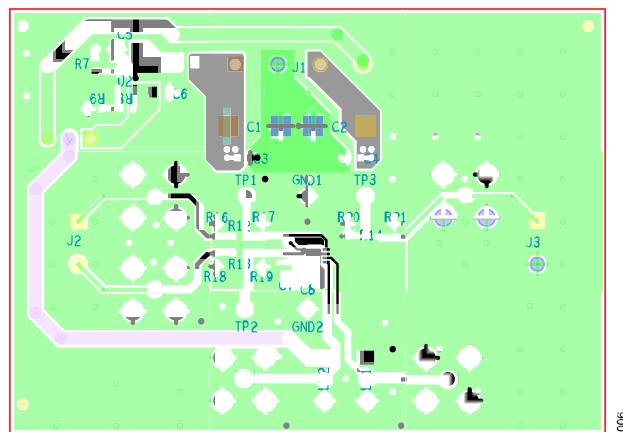
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Figure 4. EVAL-ADG1519EBZ Evaluation Board Schematic—Page 2



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Figure 5. EVAL-ADG1519EBZ Silkscreen



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Figure 6. EVAL-ADG1519EBZ Top Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

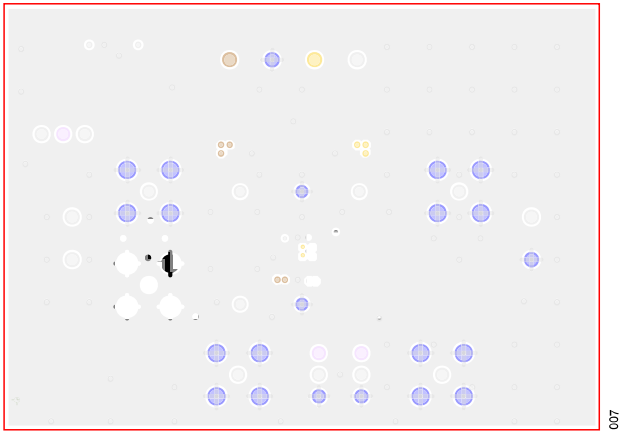


Figure 7. EVAL-ADG1519EBZ Layer 2

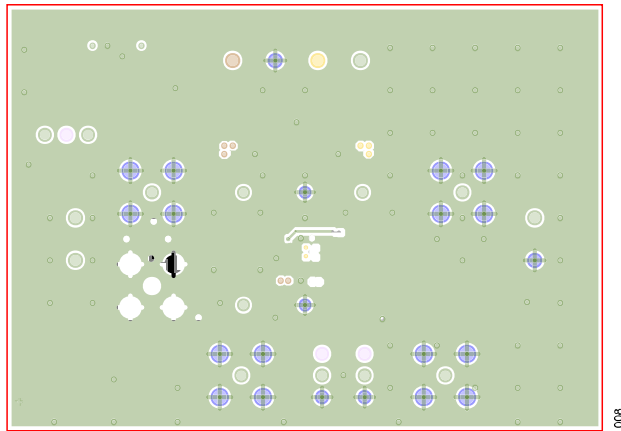


Figure 8. EVAL-ADG1519EBZ Layer 3

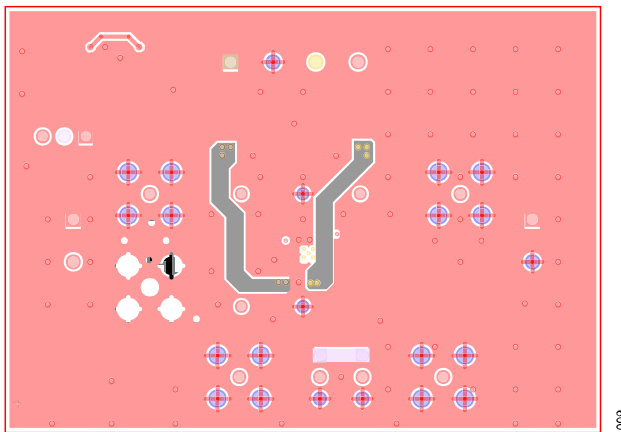


Figure 9. EVAL-ADG1519EBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer	Part Number
C1, C2	10 μ F tantalum capacitors, 50 V, Size D	AVX	TAJD106K050RNJ
C3, C4, C7, C8	0.1 μ F, multilayer, ceramic capacitors, 50 V	Vishay	VJ0603Y104KXAC31X
C5, C6	4.7 μ F, multilayer, ceramic capacitors	TDK	C2012X5R1H475K125AB
D, EN, IN, SA, SB	50 Ω , SMB sockets	Amphenol	SMB1251B1-3GT30G-50
GND1, GND2	Test points, black	Vero Technologies	20-2137
J1	4-pin terminal block, 5 mm pitch	Camdenboss LTD	CTB5000/4
J2, J3	2-pin terminal blocks, 5 mm pitch	Camdenboss LTD	CTB5000/2
LK1, LK2, LK3	3-pin headers and shorting links	Harwin	M20-9990345
R7, R8, R12, R13, R14	0 Ω resistors	Panasonic	ERJ-3GEY0R00V
R6	0 Ω resistors	Panasonic	ERJ-6GEY0R00V
TP1, TP5, TP3	Test points, red	Vero Technologies	20-313137
U1	3.8 Ω on-resistance, SPDT switch	Analog Devices, Inc.	ADG1519
U2	40 V, 200 mA, low noise, CMOS LDO linear regulator	Analog Devices	ADP7142AUJZ-5.0

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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