4.5 Ω R_{ON}, Quad SPDT ±5 V, +12 V, +5 V, and +3.3 V Switch

Data Sheet

ADG1634-KGD

FEATURES

- 4.5 Ω typical on resistance at ±5 V and 25°C
- 1 Ω typical on-resistance flatness at ±5 V and 25°C
- Up to 234 mA continuous current
- ±3.3 V to ±8 V dual-supply operation
- 3.3 V to 16 V single-supply operation
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation

APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

GENERAL DESCRIPTION

The ADG1634-KGD is a monolithic industrial CMOS (*i*CMOS®) analog switch comprising four independently selectable SPDT switches.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input on the ADG1634-KGD is used to enable or disable the device. When disabled, all channels are switched off.

The ultralow, on resistance and on-resistance flatness of this switch make the device an ideal solution for data acquisition and gain switching applications, where low distortion is critical. Its *i*CMOS construction ensures ultralow power dissipation, making the ADG1634-KGD ideally suited for portable and battery-powered instruments.

Additional application and technical information can be found in the ADG1634 data sheet.

Known Good Die (KGD): this die is fully guaranteed to data sheet specifications.

FUNCTIONAL BLOCK DIAGRAM

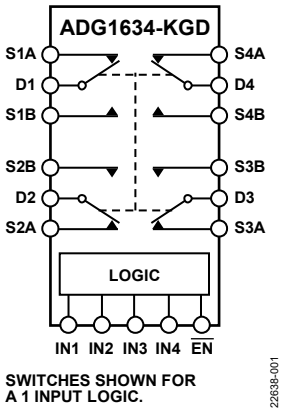

Figure 1.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

11/2020—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	4.5			Ω typ	Supply voltage (V_S) = ±4.5 V, supply current (I_S) = −10 mA, see Figure 3
	5	7	8	Ω max	V_{DD} = ±4.5 V, V_{SS} = ±4.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.3	1.7	2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±4.5 V, drain voltage (V_D) = ±4.5 V, see Figure 4
	±0.1	±1.5	±12	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±4.5 V, V_D = ±4.5 V, see Figure 4
	±0.15	±2	±20	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = ±4.5 V, see Figure 5
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	161			ns typ	Load resistance (R_L) = 300 Ω, load capacitance (C_L) = 35 pF
	200	236	264	ns max	V_S = 2.5 V, see Figure 6
t_{ON} ($\overline{EN}$)	61			ns typ	R_L = 300 Ω, C_L = 35 pF
	79	88	98	ns max	V_S = 2.5 V, see Figure 8
t_{OFF} ($\overline{EN}$)	162			ns typ	R_L = 300 Ω, C_L = 35 pF
	199	232	259	ns max	V_S = 2.5 V, see Figure 8
Break-Before-Make Time Delay, t_D	44			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	S1x voltage (V_{S1x}) = S2x voltage (V_{S2x}) = 2.5 V, see Figure 7
Charge Injection	−12.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 9
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency (f) = 1 MHz, see Figure 10
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 12
Total Harmonic Distortion + Noise, THD + N	0.3			% typ	R_L = 110 Ω, V_S = 5 V p-p, f = 20 Hz to 20 kHz, see Figure 13
−3 dB Bandwidth	103			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 11
Source Capacitance Off, C_S (Off)	19			pF typ	V_S = 0 V, f = 1 MHz
Drain Capacitance Off, C_D (Off)	33			pF typ	V_S = 0 V, f = 1 MHz
Source and Drain Capacitance On, C_D, C_S (On)	57			pF typ	V_S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Supply Current, I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
V_{DD}/V_{SS}			±3.3/±8	V min/max	

[1] Guaranteed by design but not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, and GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
R_{ON}	4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA, see Figure 3
	4.5	6.5	7.5	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
ΔR_{ON}	0.12			Ω typ	V_S = 10 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
$R_{FLAT(ON)}$	0.9			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.2	1.6	1.9	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
I_S (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 4
	±0.1	±1.5	±12	nA max	
I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 4
	±0.15	±2	±20	nA max	
I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V, see Figure 5
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
V_{INH}			2.0	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	127			ns typ	R_L = 300 Ω, C_L = 35 pF
	151	182	205	ns max	V_S = 8 V, see Figure 6
t_{ON} ($\overline{EN}$)	31			ns typ	R_L = 300 Ω, C_L = 35 pF
	38	43	47	ns max	V_S = 8 V, see Figure 8
t_{OFF} ($\overline{EN}$)	128			ns typ	R_L = 300 Ω, C_L = 35 pF
	152	180	200	ns max	V_S = 8 V, see Figure 8
t_D	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 8 V, see Figure 7
Charge Injection	−12.4			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 9
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 10
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 12

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
THD + N	0.3			% typ	R_L = 110 Ω, V_S = 5 V p-p, f = 20 Hz to 20 kHz, see Figure 13
−3 dB Bandwidth	109			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 11
C_S (Off)	19			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	32			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	56			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 12 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	Digital inputs = 0 V or V_{DD}
	375			µA typ	Digital inputs = 5 V
			600	µA max	Digital inputs = 5 V
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design but not subject to production test.

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, and GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
R_{ON}	8.5			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA, see Figure 3
	10	12.5	14	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V
ΔR_{ON}	0.15			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.3	0.35	0.4	Ω max	
$R_{FLAT(ON)}$	1.7			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	2.3	2.7	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
I_S (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, see Figure 4
	±0.1	±1.5	±12	nA max	
I_D (Off)	±0.02			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, see Figure 4
	±0.15	±2	±20	nA max	
I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 4.5 V, see Figure 5
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
V_{INH}			2.0	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	199			ns typ	R_L = 300 Ω, C_L = 35 pF
	254	303	337	ns max	V_S = 2.5 V, see Figure 6
t_{ON} ($\overline{EN}$)	68			ns typ	R_L = 300 Ω, C_L = 35 pF
	90	102	110	ns max	V_S = 2.5 V, see Figure 8
t_{OFF} ($\overline{EN}$)	201			ns typ	R_L = 300 Ω, C_L = 35 pF
	256	300	333	ns max	V_S = 2.5 V, see Figure 8

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
t_D	57			ns typ	R_L = 300 Ω, C_L = 35 pF
			37	ns min	V_{S1} = V_{S2} = 2.5 V, see Figure 7
Charge Injection	−5			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 9
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 10
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 12
THD + N	0.27			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p, see Figure 13
−3 dB Bandwidth	104			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 11
C_S (Off)	21			pF typ	V_S = 2.5 V, f = 1 MHz
C_D (Off)	37			pF typ	V_S = 2.5 V, f = 1 MHz
C_D, C_S (On)	62			pF typ	V_S = 2.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design but not subject to production test.

3.3 V SINGLE SUPPLY

V_{DD} = 3.3 V, V_{SS} = 0 V, and GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
R_{ON}	13.5	15	16.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA, see Figure 3, V_{DD} = 3.3 V, V_{SS} = 0 V
ΔR_{ON}	0.25	0.28	0.3	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
$R_{FLAT(ON)}$	5	5.5	6.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V, V_{SS} = 0 V
I_S (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V, see Figure 4
	±0.1	±1.5	±12	nA max	
I_D (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V, see Figure 4
	±0.15	±2	±20	nA max	
I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 0.6 V or 3 V, see Figure 5
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
V_{INH}			2.0	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
$t_{TRANSITION}$	309			ns typ	R_L = 300 Ω, C_L = 35 pF
	429	466	508	ns max	V_S = 1.5 V, see Figure 6
t_{ON} ($\overline{EN}$)	132			ns typ	R_L = 300 Ω, C_L = 35 pF
	184	201	210	ns max	V_S = 1.5 V, see Figure 8
t_{OFF} ($\overline{EN}$)	313			ns typ	R_L = 300 Ω, C_L = 35 pF
	416	470	509	ns max	V_S = 1.5 V, see Figure 8

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
t_D	81			ns typ	R_L = 300 Ω, C_L = 35 pF
			48	ns min	V_{S1} = V_{S2} = 1.5 V, see Figure 7
Charge Injection	−10			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 9
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 10
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 12
THD + N	0.6			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p, see Figure 13
−3 dB Bandwidth	117			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 11
C_S (Off)	22			pF typ	V_S = 1.5 V, f = 1 MHz
C_D (Off)	39			pF typ	V_S = 1.5 V, f = 1 MHz
C_D, C_S (On)	64			pF typ	V_S = 1.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design but not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +5 V, V_{SS} = −5 V				
θ_{JA} = 95°C/W	112	77	52	mA max
θ_{JA} = 30.4°C/W	220	136	73	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
θ_{JA} = 95°C/W	119	80	52	mA max
θ_{JA} = 30.4°C/W	234	140	73	mA max
V_{DD} = 5 V, V_{SS} = 0 V				
θ_{JA} = 95°C/W	87	63	42	mA max
θ_{JA} = 30.4°C/W	171	112	66	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V				
θ_{JA} = 95°C/W	70	52	35	mA max
θ_{JA} = 30.4°C/W	140	94	59	mA max

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sxx or Dx	450 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sxx or Dx[2]	Data + 15%
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C

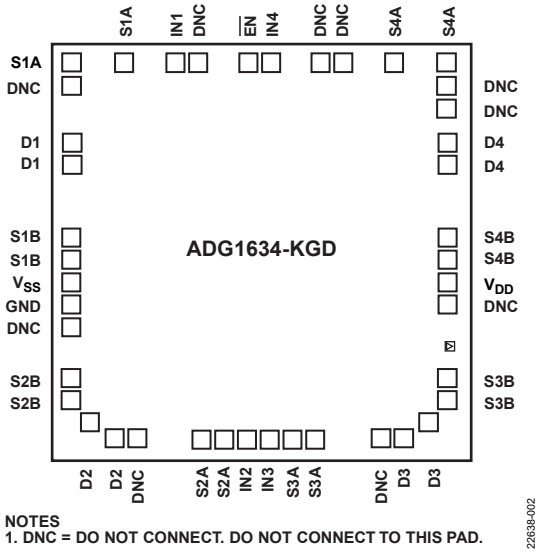
[1] Overvoltages at INx, Sxx, or Dx are clamped by internal diodes. Current should be limited to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PAD.

Figure 2. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	Mnemonic	X Coordinate	Y Coordinate	Description
1	S1A	−710	+710	Source Terminal 1A. This pad can be an input or an output.
2	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
3	D1	−710	+413	Drain Terminal 1. This pad can be an input or an output.
4	D1	−710	+328	Drain Terminal 1. This pad can be an input or an output.
5	S1B	−710	+55	Source Terminal 1B. This pad can be an input or an output.
6	S1B	−710	−30	Source Terminal 1B. This pad can be an input or an output.
7	V_{SS}	−710	−117	Most Negative Power Supply Potential. In single-supply applications, connect this pad to ground.
8	GND	−710	−203	Ground (0 V) Reference.
9	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
10	S2B	−710	−480	Source Terminal 2B. This pad can be an input or an output.
11	S2B	−710	−565	Source Terminal 2B. This pad can be an input or an output.
12	D2	−641	−651	Drain Terminal 2. This pad can be an input or an output.
13	D2	−545	−710	Drain Terminal 2. This pad can be an input or an output.
14	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
15	S2A	−215	−710	Source Terminal 2A. This pad can be an input or an output.
16	S2A	−130	−710	Source Terminal 2A. This pad can be an input or an output.
17	IN2	−43	−710	Logic Control Input 2.
18	IN3	+43	−710	Logic Control Input 3.
19	S3A	+130	−710	Source Terminal 3A. This pad can be an input or an output.
20	S3A	+215	−710	Source Terminal 3A. This pad can be an input or an output.
21	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
22	D3	+545	−710	Drain Terminal 2. This pad can be an input or an output.
23	D3	+641	−651	Drain Terminal 2. This pad can be an input or an output.

Pad No.	Mnemonic	X Coordinate	Y Coordinate	Description
24	S3B	+710	−565	Source Terminal 3B. This pad can be an input or an output.
25	S3B	+710	−480	Source Terminal 3B. This pad can be an input or an output.
26	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
27	V_{DD}	+710	−117	Most Positive Power Supply Potential.
28	S4B	+710	−30	Source Terminal 4B. This pad can be an input or an output.
29	S4B	+710	+55	Source Terminal 4B. This pad can be an input or an output.
30	D4	+710	+328	Drain Terminal 4. This pad can be an input or an output.
31	D4	+710	+413	Drain Terminal 4. This pad can be an input or an output.
32	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
33	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
34	S4A	+710	+710	Source Terminal 4A. This pad can be an input or an output.
35	S4A	+510	+710	Source Terminal 4A. This pad can be an input or an output.
36	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
37	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
38	IN4	+43	+710	Logic Control Input 4.
39	$\overline{EN}$	−43	+710	Active Low Digital Input. When this pad is high, the device is disabled, and all switches are off. When this pad is low, INx logic inputs determine the on switches.
40	DNC	Not applicable	Not applicable	Do Not Connect. Do not connect to this pad.
41	IN1	−320	+710	Logic Control Input 1.
42	S1A	−510	+710	Source Terminal 1A. This pad can be an input or an output.

Table 8. Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X (don't care)	Off	Off
0	0	Off	On
0	1	On	Off

TEST CIRCUITS

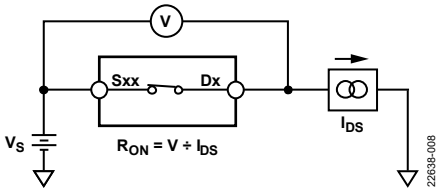


Figure 3. On Resistance (I_{DS} is the Drain to Source Current.)

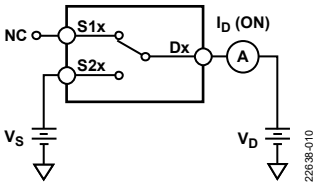


Figure 5. On Leakage

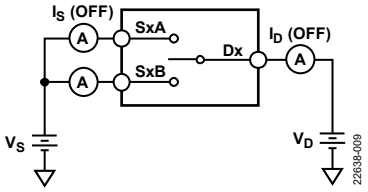


Figure 4. Off Leakage

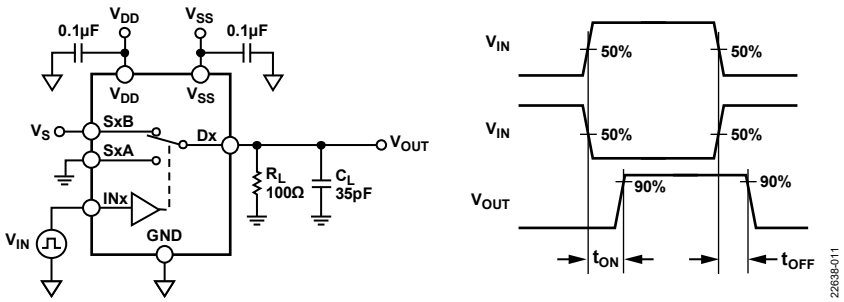


Figure 6. Switching Timings, t_{ON} and t_{OFF}

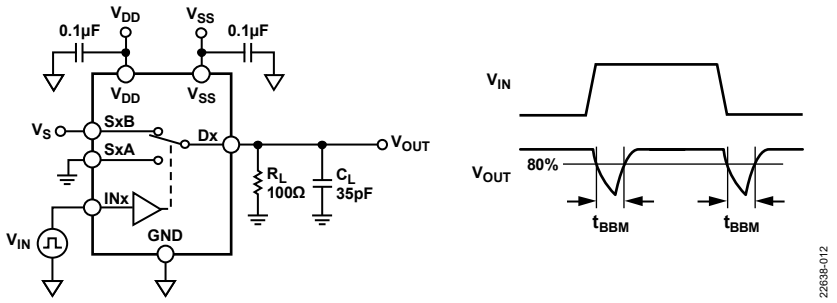


Figure 7. Break-Before-Make Delay, t_D

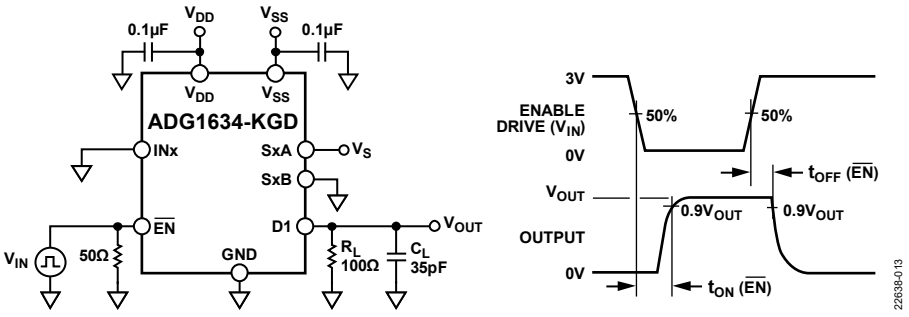


Figure 8. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

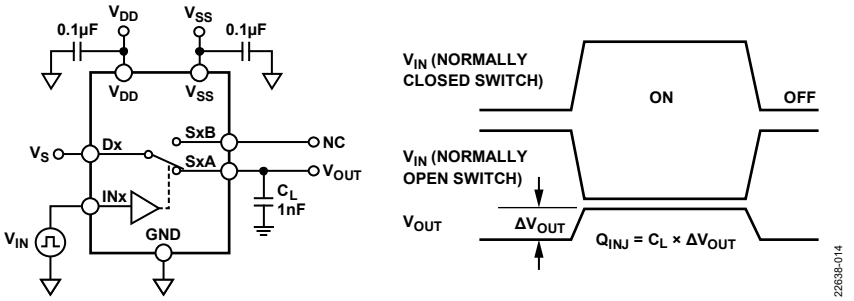


Figure 9. Charge Injection

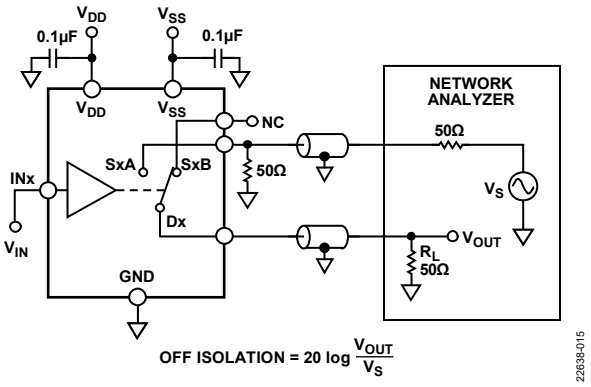


Figure 10. Off Isolation

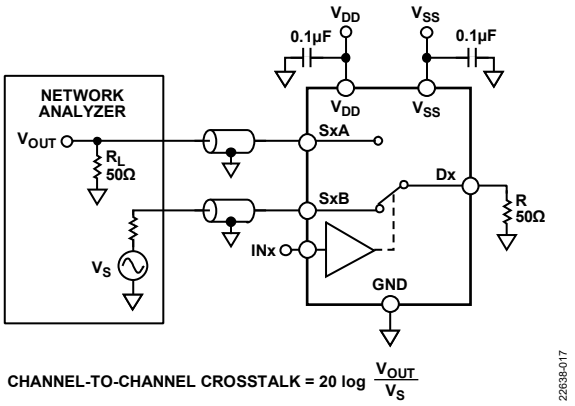


Figure 12. Channel-to-Channel Crosstalk

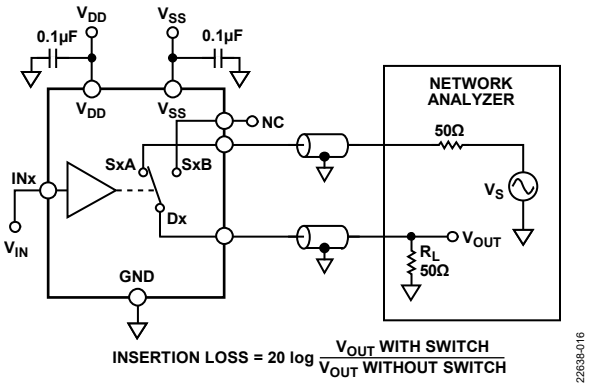


Figure 11. Bandwidth

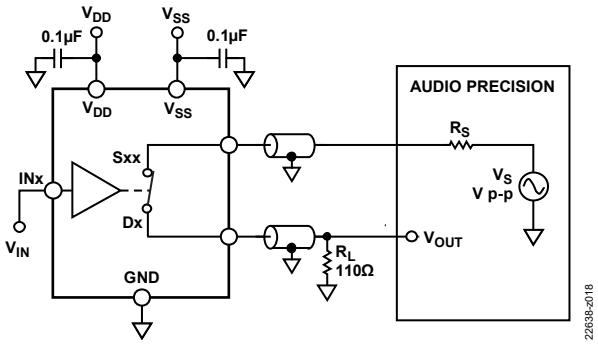


Figure 13. THD + Noise

OUTLINE DIMENSIONS

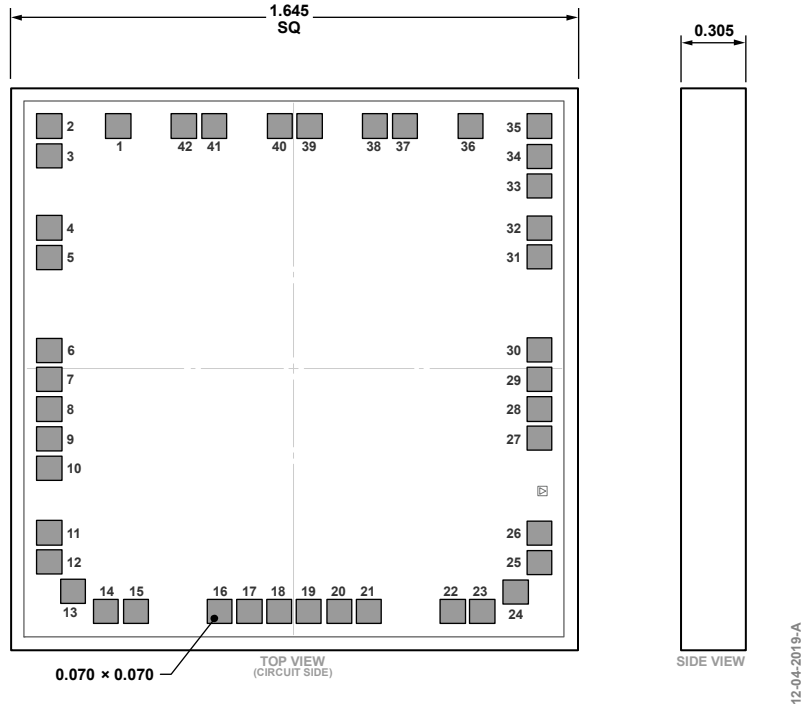


Figure 14. 42-Pad Bare Die [CHIP]
(C-42-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 9. Die Specifications

Parameter	Value	Unit
Chip Size	1565 × 1565	µm
Scribe Line Width	80 × 80	µm
Die Size	1645 × 1645	µm
Thickness	305	µm
Backside	V_{SS}	Not applicable
Passivation	Oxynitride	Not applicable
Bond Pads (Minimum)	70 × 70	µm
Bond Pad Composition	Aluminum (Al), Copper (Cu), 0.5%	Not applicable

Table 10. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy dispense
Bonding Method	Thermosonic gold ball bonding

ORDERING GUIDE

Model[1]	Temperature Range	Description	$\overline{EN}$ Pin	Package Option
ADG1634-KGD-WP	−40°C to +125°C	42-Pad Bare Die [CHIP]	Yes	C-42-1

[1] Z = RoHS Compliant Part.