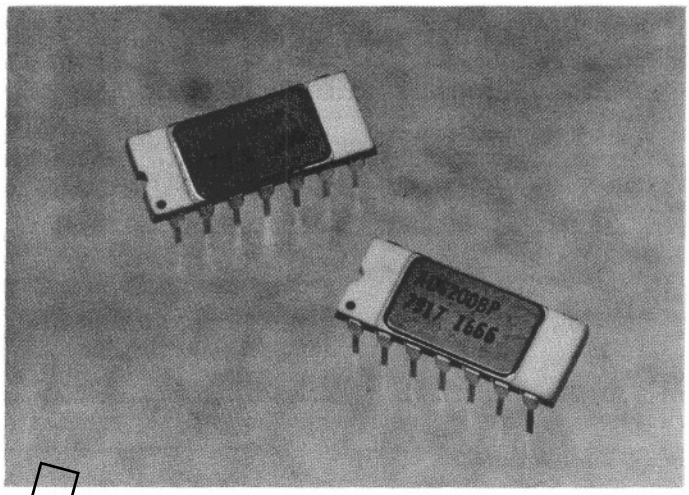
DI CMOS
Protected Dual SPST Analog Switch
ADG200

FEATURES
- Latch-Proof DI CMOS
- Overvoltage-Proof: V_{SUPPLY} ±25V
- Superior DG-200 Replacement
- Break-Before-Make Switching Action
- R_{ON}: 100Ω max over Full Temperature Range
- Direct TTL/CMOS Interface



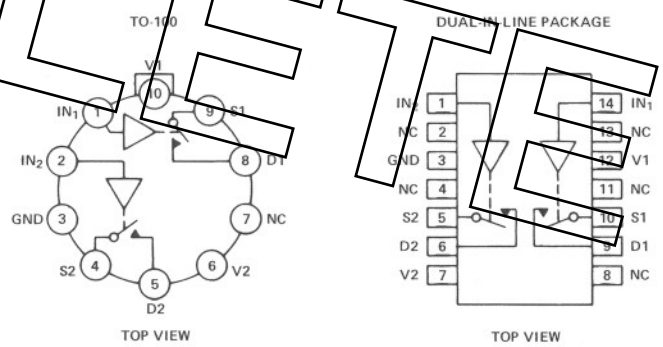
OBSOLETE

GENERAL DESCRIPTION

The ADG200 is a dual single-pole-single-throw analog switch. In the ON condition, the switch conducts current in either direction, maintaining nearly constant ON resistance over the entire analog signal range. In the OFF condition, the switch blocks voltages of peak values equal to the switch V+ and V– supplies. Switch action is break-before-make. The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated using an advanced monolithic dielectrically-isolated CMOS process, the ADG200 is a superior plug-in replacement for the DG200. The ADG200 provides additional advantages (over the DG200) of: overvoltage protection to ±25V beyond the power supplies, total latch-free operation, much lower power dissipation (30mW max) and faster switching time.

PIN CONFIGURATION



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C		Military -55°C to +125°C	
Plastic	Ceramic	TO-100	Ceramic	TO-100
ADG200CJ	ADG200BP	ADG200BA	ADG200AP	ADG200AA ADG200AA/883

Note: "/883" version is 100% screened to MIL-STD-883, class B as per note 7, page 2.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS

CHARACTERISTIC[1]		TYP[1] +25°C	MAX LIMITS AA, AP Suffix −55°C[2]	AA, AP Suffix +25°C	AA, AP Suffix +125°C	BA, BP/CJ Suffix −25/0°C[2]	BA, BP/CJ Suffix +25°C	BA, BP/CJ Suffix +85/70°C[2]	UNITS	TEST CONDITIONS[8] Unless Noted V_1 = +15V, V_2 = −15V, GND = 0V	
SWITCH											
$r_{DS(ON)}$	Drain-Source ON Resistance	60 40	70 70	70 70	100 100	80 80	80 80	100 100	Ω	V_D = 10V V_D = −10V	V_{IN} = 0.8V I_S = 0.1mA
$I_{S(OFF)}$	Source OFF Leakage Current	0.2 −0.2	500 −500	2 −2	500 −500	500 −500	5 −5	500 −500	nA	V_S = 10V, V_D = −10V V_S = −10V, V_D = 10V	V_{IN} = 2.4V
$I_{D(OFF)}$	Drain OFF Leakage Current	0.3 −0.3	500 −500	2 −2	500 −500	500 −500	5 −5	500 −500	nA	V_D = 10V, V_S = −10V V_D = −10V, V_S = 10V	V_{IN} = 2.4V
$I_{D(ON)}$[3]	Channel ON Leakage Current	0.1 −0.1	500 −500	2 −2	500 −500	500 −500	2 −2	500 −500	nA	V_D = V_S = 10V V_D = V_S = −10V	V_{IN} = 0.8V
INPUT											
I_{INH}	Input Current Input Voltage High		−10 10	−1 1	−10 10	−10 10	−1 1	−10 10	μA	V_{IN} = 2.4V V_{IN} = 15V	
$I_{IN(PEAK)}$[4]	Peak Input Current Required for Transition	NOT APPLICABLE[4]									
I_{INL}	Input Current Input Voltage Low		−10	−1	−10	−10	−1	−10	μA	V_{IN} = 0V	
DYNAMIC											
t_{ON}	Turn-ON Time[5]	300		1000[2]			1000[2]		ns	V_{IN} = 3.5V to 0V	R_L = 1kΩ, C_L = 35pF
t_{OFF}	Turn-OFF Time[5]	120		500[2]			500[2]		ns	V_{IN} = 0V to 3.5V	V_S = ±5V
$C_{S(OFF)}$	Source OFF Capacitance	11							pF	V_S = 0V, V_{IN} = 5V	
$C_{D(OFF)}$	Drain OFF Capacitance	11							pF	V_D = 0V, V_{IN} = 5V	f = 140kHz
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance	28							pF	V_D = V_S = 0V V_{IN} = 0V	
OFF Isolation[6]		64							dB	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF V_S = 7V_{rms}, f = 500kHz	
SUPPLY											
I_1	Positive Supply Current	0.02	2	1	2	2	1	2	mA	Both Channels ON; V_{IN} = 0V	
I_2	Negative Supply Current	−0.02	−2	−1	−2	−2	−1	−2	mA		
I_1	Positive Supply Current	0.1	2	1	2	2	1	2	mA	Both Channels OFF; V_{IN} = 5V	
I_2	Negative Supply Current	−0.02	−2	−1	−2	−2	−1	−2	mA		

PRICES	1–24	25–99	100–499	500–999	1K	$
ADG200CJ	3.50	3.00	2.50	2.25	2.00	
ADG200BP	11.00	8.50	7.00	7.00	6.50	
ADG200AP	13.00	10.00	8.50	8.50	7.75	
ADG200BA	3.50	3.00	2.50	2.25	2.00	
ADG200AA	11.00	9.00	7.75	7.75	7.00	
ADG200AA/883[7]	15.00	12.75	11.25	11.25	10.75	

NOTES:
[1] Typical values for information only, not guaranteed or production tested.
[2] Guaranteed, not subject to 100% production test.
[3] $I_{D(ON)}$ is leakage from driver gate into ON switch.
[4] Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.
[5] Switch action is guaranteed break-before-make.
[6] OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.
[7] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for a class B device. Final electrical tests are: $r_{DS(ON)}$, $I_{S(OFF)}$, $I_{D(OFF)}$, I_{INH}, I_{INL}, I_1, and I_2 at +25°C and +125°C (AA/883 version).
[8] Functional operation is possible for supply voltages less than ±15V, but the input logic switching threshold will shift (see page 4).

Specifications subject to change without notice.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

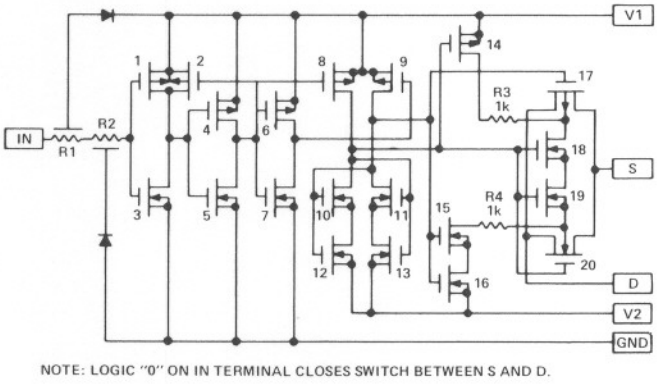
ABSOLUTE MAXIMUM RATINGS

V_{IN}(Digital Input) to Ground . . . . . -0.3V, V_1
V_S or V_D to V_1
(1 second surge) . . . . . +25V, −40V
(continuous) . . . . . +20V, −35V
V_S or V_D to V_2
(1 second surge) . . . . . −25V, +40V
(continuous) . . . . . −20V, +35V
V_1 to Ground . . . . . -0.3V, +17V
V_2 to Ground . . . . . +0.3V, −17V
Current, Any Terminal Except S or D 30mA
Current, S or D 50mA
Current, S or D Pulsed
(1ms, 10% duty cycle max) 150mA

Operating Temperature
AA, AP Suffix . . . . . -55°C to +125°C
BA, BP Suffix . . . . . -25°C to +85°C
CJ Suffix . . . . . 0°C to +70°C
Storage Temperature
CJ Suffix . . . . . -65°C to +125°C
All Others . . . . . -65°C to +150°C
Power Dissipation (Package)*
Metal Can** 450mW
14 Pin Ceramic DIP*** 825mW
14 Pin Plastic DIP**** 470mW

* Devices with all leads welded or soldered to printed circuit board
** Derate 6mW/°C above +75°C
*** Derate 11mW/°C above +75°C
**** Derate 6.5mW/°C above +25°C

CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram (1 of 2 channels)

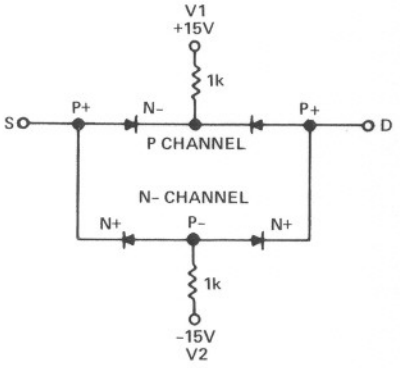


Figure 2. ADG200 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG200 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14, 15, and 16.

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2, the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG200 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices — *not* in series with the signal path between the S & D terminals.

In some applications it is possible to run on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

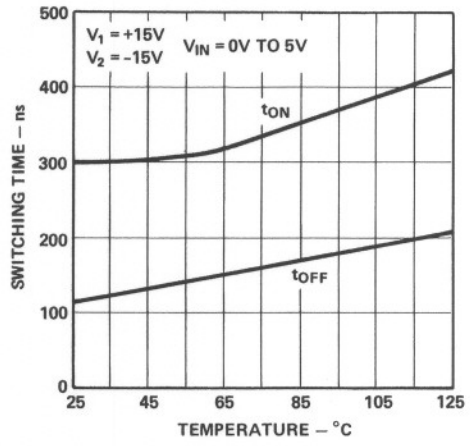


Figure 3. Switching Time vs. Temperature

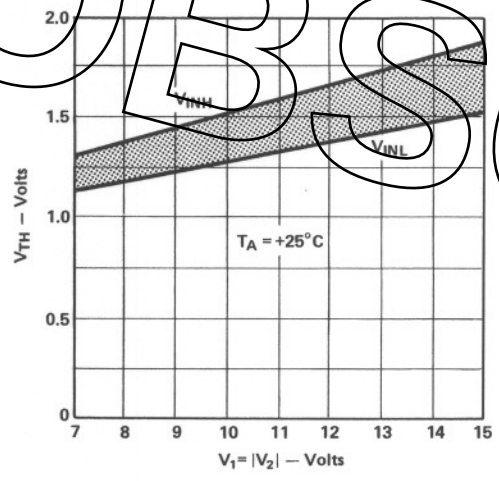
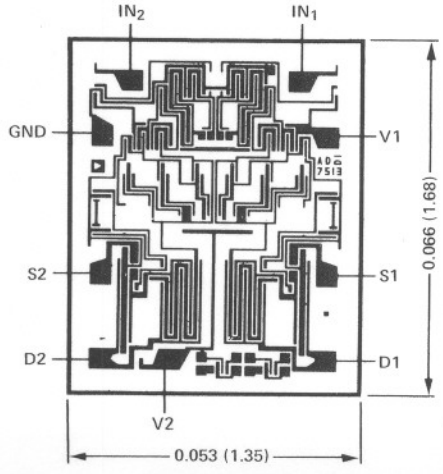


Figure 4. Input Logic Threshold vs. Power Supply Voltage

BONDING DIAGRAM

Dimensions shown in inches and (mm).

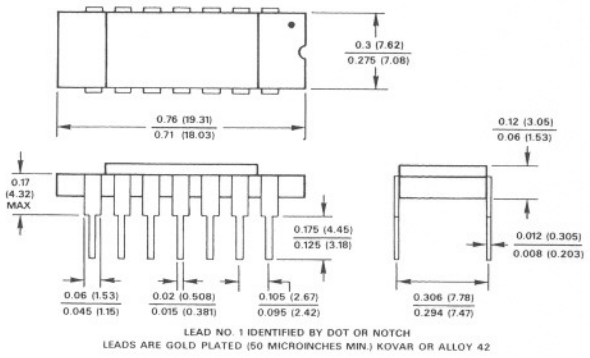


NOTES:
1. BOND GND PIN FIRST TO MINIMIZE ESD HAZARD.
2. BONDING PADS ARE 0.004 X 0.004 INCHES (0.102 X 0.102mm).

MECHANICAL INFORMATION

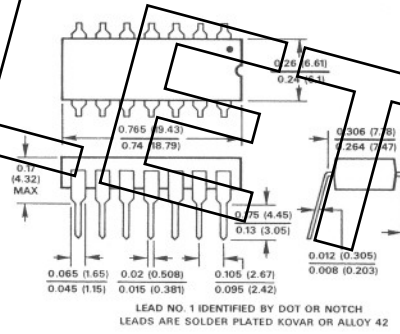
Dimensions shown in inches and (mm).

14-PIN CERAMIC DIP



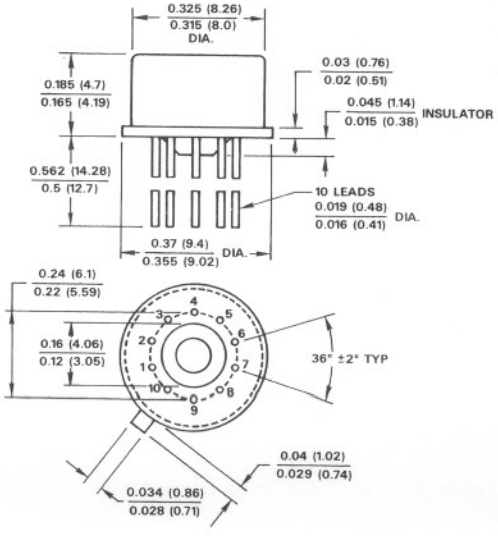
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN.) KOVAR OR ALLOY 42

14-PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER PLATED KOVAR OR ALLOY 42

TO-100



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