High Temperature, Low Voltage, 8-Channel Multiplexer

ADG798-KGD

Known Good Die

FEATURES

Extreme high temperature operation up to 210°C
3.0 V to 5.5 V single supply
±2.5 V dual supply
10 Ω on resistance, maximum
2 Ω on-resistance flatness, maximum
12 ns transition time
Single 8:1 multiplexer
Low power consumption
TTL-/CMOS-compatible inputs

APPLICATIONS

Downhole drilling and instrumentation
Avionics
Heavy industrial
High temperature environments

METAL MASK DIE IMAGE

Figure 1.

GENERAL DESCRIPTION

The ADG798-KGD is a low voltage, CMOS, analog multiplexer designed to operate at very high temperatures up to 210°C. The ADG798-KGD switches one of eight inputs (S1 to S8) to a common output (D) as determined by the 3-bit binary address lines (A0, A1, and A2). An EN input on the device enables or disables the device. When the device is disabled, all channels are switched off.

The ADG798-KGD features low power consumption and a 3.3 V to 5.5 V operating supply range. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. These switches are designed with an enhanced submicron process that provides low power dissipation, high switching speed, and very low on resistance.

The on resistance (R_{ON}) is a maximum of 10 Ω and is closely matched between switches and very flat over the full signal range. The ADG798-KGD operates equally well as either a multiplexer or a demultiplexer and has an input signal range that extends to the supplies.
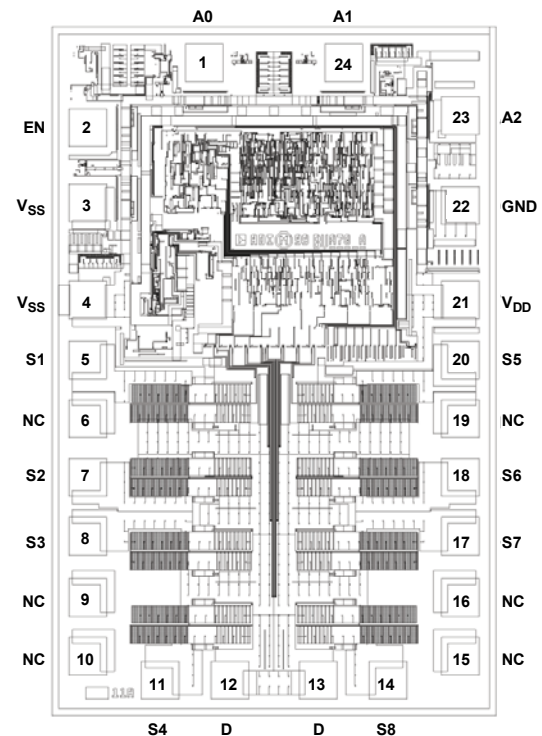
The ADG798-KGD is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

Additional application and technical information can be found in the ADG798 data sheet. Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

PRODUCT HIGHLIGHTS

1. Single-Supply/Dual-Supply Operation.
   The ADG798-KGD is fully specified and guaranteed with +3.3 V/+5 V single-supply rails and ±2.5 V dual-supply rails.
2. Low R_{ON}.
   The R_{ON} of the ADG798-KGD is specified at 5 Ω, typical, at 210°C.
3. Low Power Consumption.
   The power consumption of the ADG798-KGD is specified at <0.01 µW.
4. Break-Before-Make Switching Action.

TABLE OF CONTENTS

REVISION HISTORY

10/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	−55°C ≤ T_A ≤ +175°C Min	Typ[1]	Max	−55°C ≤ T_A ≤ +210°C Min	Typ[1]	Max	Unit
ANALOG SWITCH									
Analog Signal Range			0		V_{DD}	0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to V_{DD}, I_{DS} = 10 mA, see Figure 3		4.5	9		5	10	Ω
Matching Between Channels	ΔR_{ON}	V_S = 0 V to V_{DD}, I_{DS} = 10 mA		0.6	1.2		1.25	1.5	Ω
Flatness	$R_{FLAT (ON)}$	V_S = 0 V to V_{DD}, I_{DS} = 10 mA			1.5		0.75	2	Ω
LEAKAGE CURRENTS		V_{DD} = 5.5 V							
Source Off Leakage	I_S (Off)	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V, see Figure 4	−50	±0.01	+50	−180	±0.01	+180	nA
Drain Off Leakage	I_D (Off)	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V, see Figure 5	−650	±0.01	+650	−2600	±0.01	+2600	nA
Channel On Leakage	I_D, I_S (On)	V_D = V_S = 1 V or 4.5 V, see Figure 6	−650	±0.01	+650	−2600	±0.01	+2600	nA
DIGITAL INPUTS									
Input Voltage									
High	V_{INH}		2.4			2.4			V
Low	V_{INL}				0.8			0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{INL} or V_{INH}	−800	+0.005	+800	−800	+0.005	+800	nA
Digital Input Capacitance	C_{IN}			2			2		pF
DYNAMIC CHARACTERISTICS									
Transition Time	$t_{TRANSITION}$	R_L = 150 Ω, C_L = 15 pF, see Figure 7, V_{S1} = 3 V/0 V, V_{S8} = 0 V/3 V		12	21		12	23	ns
Break-Before-Make Time Delay	t_{OPEN}	R_L = 150 Ω, C_L = 15 pF, V_S = 3 V, see Figure 8	1	8		1	8		ns
		T_A = maximum temperature		9			9		ns
On Time	t_{ON} (EN)	R_L = 150 Ω, C_L = 15 pF, V_S = 3 V, see Figure 9		11	17		11	20	ns
Off Time	t_{OFF} (EN)	R_L = 150 Ω, C_L = 15 pF, V_S = 3 V, see Figure 9		5.5	11		5.5	12	ns
Charge Injection	Q_{INJ}	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 10		±3			±3		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		−60			−60		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 11		−80			−80		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		−60			−60		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 12		−80			−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 13		55			55		MHz
Source Capacitance, Off	C_S (Off)	f = 1 MHz		13			13		pF
Drain Capacitance, Off	C_D (Off)	f = 1 MHz		85			85		pF
Source/Drain Capacitance, On	C_D, C_S (On)	f = 1 MHz		96			96		pF
POWER REQUIREMENTS									
Supply Current	I_{DD}	V_{DD} = 5.5 V, digital inputs = 0 V or 5.5 V		5	35		40	70	μA

[1] T_A = 25°C, except for the analog switch and power requirements values where T_A = 175°C or 210°C.

V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V, GND = 0 V, −55°C ≤ T_A ≤ +210°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	−55°C ≤ T_A ≤ +175°C			−55°C ≤ T_A ≤ +210°C			Unit
			Min	Typ[1]	Max	Min	Typ[1]	Max	
ANALOG SWITCH									
Analog Signal Range			0		V_{DD}	0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to V_{DD}, I_{DS} = 10 mA, see Figure 3		7	15		8	20	Ω
Matching Between Channels	ΔR_{ON}	V_S = 0 V to V_{DD}, I_{DS} = 10 mA		0.4	1.2		0.5	1.5	Ω
Flatness	$R_{FLAT (ON)}$	V_S = 0 V to V_{DD}, I_{DS} = 10 mA		2.5	3.5		3	4.5	Ω
LEAKAGE CURRENTS		V_{DD} = 3.3 V							
Source Off Leakage	I_S (Off)	V_D = 2.3 V/1 V, V_S = 1 V/2.3 V, see Figure 4	−50	±0.01	+50	−180	±0.01	+180	nA
Drain Off Leakage	I_D (Off)	V_D = 2.3 V/1 V, V_S = 1 V/2.3 V, see Figure 5	−650	±0.01	+650	−2600	±0.01	+2600	nA
Channel On Leakage	I_D, I_S (On)	V_D = V_S = 1 V or 2.3 V, see Figure 6	−650	±0.01	+650	−2600	±0.01	+2600	nA
DIGITAL INPUTS									
Input Voltage									
High	V_{INH}		2.0			2.0			V
Low	V_{INL}				0.8			0.8	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{INL} or V_{INH}	−800	+0.005	+800	−800	+0.005	+800	nA
Digital Input Capacitance	C_{IN}			2			2		pF
DYNAMIC CHARACTERISTICS									
Transition Time	$t_{TRANSITION}$	R_L = 150 Ω, C_L = 15 pF, see Figure 7, V_{S1} = 2 V/0 V, V_{S8} = 0 V/2 V		18	34		18	38	ns
Break-Before-Make Time Delay	t_{OPEN}	R_L = 150 Ω, C_L = 15 pF, V_S = 2 V, see Figure 8	1	10		1	10		ns
		T_A = maximum temperature		15			15		ns
On Time	t_{ON} (EN)	R_L = 150 Ω, C_L = 15 pF, V_S = 2 V, see Figure 9		14	26		14	28	ns
Off Time	t_{OFF} (EN)	R_L = 150 Ω, C_L = 15 pF, V_S = 2 V, see Figure 9		8.5	16		8.5	17	ns
Charge Injection	Q_{INJ}	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 10		±3			±3		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		−60			−60		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 11		−80			−80		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		−60			−60		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 12		−80			−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 13		55			55		MHz
Source Capacitance, Off	C_S (Off)	f = 1 MHz		13			13		pF
Drain Capacitance, Off	C_D (Off)	f = 1 MHz		85			85		pF
Source/Drain Capacitance, On	C_D, C_S (On)	f = 1 MHz		96			96		pF
POWER REQUIREMENTS									
Supply Current	I_{DD}	V_{DD} = 3.3 V, digital inputs = 0 V or 3.3 V		5	35		40	70	μA

[1] T_A = 25°C, except for the analog switch and power requirements values where T_A = 175°C or 210°C.

DUAL SUPPLY

V_{DD} = 2.5 V ± 10%, V_{SS} = −2.5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	−55℃ ≤ T_A ≤ +175℃			−55℃ ≤ T_A ≤ +210℃			Unit
			Min	Typ[1]	Max	Min	Typ[1]	Max	
ANALOG SWITCH									
Analog Signal Range			V_{SS}		V_{DD}	V_{SS}		V_{DD}	V
On Resistance	R_{ON}	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA, see Figure 3		4.5	9		5	10	Ω
Matching Between Channels	ΔR_{ON}	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA		0.6	1.2		1.25	1.5	Ω
Flatness	$R_{FLAT (ON)}$	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA		0.5	1.5		0.6	2	Ω
LEAKAGE CURRENTS		V_{DD} = +2.75 V, V_S = −2.75 V							
Source Off Leakage	I_S (Off)	V_S = +2.25 V/−1.25 V, V_D = −1.25 V/+2.25 V, see Figure 4	−50	±0.01	+50	−180	±0.01	+180	nA
Drain Off Leakage	I_D (Off)	V_S = +2.25 V/−1.25 V, V_D = −1.25 V/+2.25 V, see Figure 5	−650	±0.01	+650	−2600	±0.01	+2600	nA
Channel On Leakage	I_D, I_S (On)	V_D = V_S = −1.25 V/+2.25 V, see Figure 6	−650	±0.01	+650	−2600	±0.01	+2600	nA
DIGITAL INPUTS									
Input Voltage									
High	V_{INH}		1.7			1.7			V
Low	V_{INL}				0.7			0.7	V
Input Current	I_{INL} or I_{INH}	V_{IN} = V_{INL} or V_{INH}	−800	+0.005	+800	−800	+0.005	+800	nA
Digital Input Capacitance	C_{IN}			2			2		pF
DYNAMIC CHARACTERISTICS									
Transition Time	$t_{TRANSITION}$	R_L = 150 Ω, C_L = 15 pF, see Figure 7, V_{S1} = 1.5 V/0 V, V_{S8} = 0 V/1.5 V		18	28		18	30	ns
Break-Before-Make Time Delay	t_{OPEN}	R_L = 150 Ω, C_L = 15 pF, V_S = 2 V, see Figure 8	1	10		1	10		ns
		T_A = maximum temperature		13			13		ns
On Time	t_{ON} (EN)	R_L = 150 Ω, C_L = 15 pF, V_S = 2 V, see Figure 9		19	28		19	30	ns
Off Time	t_{OFF} (EN)	R_L = 150 Ω, C_L = 15 pF, V_S = 2 V, see Figure 9		11.5	19		11.5	20	ns
Charge Injection	Q_{INJ}	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 10		±3			±3		pC
Off Isolation		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		−60			−60		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 11		−80			−80		dB
Channel to Channel Crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		−60			−60		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 12		−80			−80		dB
−3 dB Bandwidth		R_L = 50 Ω, C_L = 5 pF, see Figure 13		55			55		MHz
Source Capacitance, Off	C_S (Off)	f = 1 MHz		13			13		pF
Drain Capacitance, Off	C_D (Off)	f = 1 MHz		85			85		pF
Source/Drain Capacitance, On	C_D, C_S (On)	f = 1 MHz		96			96		pF
POWER REQUIREMENTS									
Supply Current	I_{DD}	V_{DD} = 2.75 V, digital inputs = 0 V or 2.75 V		5	35		40	70	µA
	I_{SS}	V_{SS} = −2.75 V, digital inputs = 0 V or 2.75 V		5	35		40	70	µA

[1] T_A = 25℃, except for the analog switch and power requirements values where T_A = 175℃ or 210℃.

CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 4.

Parameter	175°C	210°C	Unit
CONTINUOUS CURRENT PER CHANNEL, Sx OR D			
V_{DD} = 4.5 V, V_{SS} = 0 V			
θ_{JA} = 50°C/W	89.4	31	mA maximum
θ_{JA} = 70°C/W	75.5	31	mA maximum
θ_{JA} = 120°C/W	57.5	31	mA maximum
θ_{JA} = 150°C/W	51.6	31	mA maximum
V_{DD} = 3 V, V_{SS} = 0 V			
θ_{JA} = 50°C/W	63.2	31	mA maximum
θ_{JA} = 70°C/W	53.4	31	mA maximum
θ_{JA} = 120°C/W	40.8	25.3	mA maximum
θ_{JA} = 150°C/W	36.5	22.6	mA maximum

PEAK CURRENT PER CHANNEL, Sx OR D (PULSED AT 1 MS, 10% DUTY CYCLE MAXIMUM)

Table 5.

Parameter	175°C	210°C	Unit
PEAK CURRENT PER CHANNEL, Sx OR D			
V_{DD} = 4.5 V, V_{SS} = 0 V			
θ_{JA} = 50°C/W	282.7	98	mA maximum
θ_{JA} = 70°C/W	238.8	98	mA maximum
θ_{JA} = 120°C/W	181.8	98	mA maximum
θ_{JA} = 150°C/W	163.2	98	mA maximum
V_{DD} = 3 V, V_{SS} = 0 V			
θ_{JA} = 50°C/W	199.9	98	mA maximum
θ_{JA} = 70°C/W	168.9	98	mA maximum
θ_{JA} = 120°C/W	129	80	mA maximum
θ_{JA} = 150°C/W	115.4	71.5	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	7 V
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	+0.3 V to −3.5 V
Analog Inputs[1]	$V_{SS} − 0.3$ V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, Sx or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	See Table 5
Continuous Current, Sx or D[2]	Data + 5%
Operating Temperature Range	−55°C to +210°C

[1] Overvoltages at Ax, EN, Sx, or D are clamped by internal codes. Limit the current to the maximum ratings given.
[2] See Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
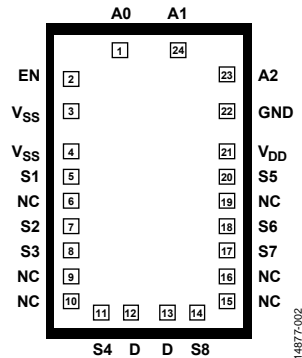
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 2. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	−185	+819	A0	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).
2	−494	+645.9	EN	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).
3	−494	+447.55	V_{SS}	Most Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, tie this pin to GND.
4	−494	+189.35	V_{SS}	Most Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, tie this pin to GND.
5	−494	+30.8	S1	Source Terminal. Can be an input or output.
6	−494	−125.2	NC	No Connect. Do not connect to this pad.
7	−494	−281.2	S2	Source Terminal. Can be an input or output.
8	−494	−437.2	S3	Source Terminal. Can be an input or output.
9	−494	−599.8	NC	No Connect. Do not connect to this pad.
10	−494	−755.8	NC	No Connect. Do not connect to this pad.
11	−302.5	−819	S4	Source Terminal. Can be an input or output.
12	−116.8	−819	D	Drain Terminal. Can be an input or output.
13	+116.8	−819	D	Drain Terminal. Can be an input or output.
14	+302.5	−819	S8	Source Terminal. Can be an input or output.
15	+494	−755.8	NC	No Connect. Do not connect to this pad.
16	+494	−599.8	NC	No Connect. Do not connect to this pad.
17	+494	−437.2	S7	Source Terminal. Can be an input or output.
18	+494	−281.2	S6	Source Terminal. Can be an input or output.
19	+494	−125.2	NC	No Connect. Do not connect to this pad.
20	+494	+30.8	S5	Source Terminal. Can be an input or output.
21	+494	+189.35	V_{DD}	Most Positive Power Supply Pin.
22	+494	+440.2	GND	Ground (0 V) Reference.
23	+494	+678.8	A2	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).
24	+184.55	+819	A1	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).

TRUTH TABLE

Table 8. Truth Table

A2	A1	A0	EN	Switch Condition
X[1]	X[1]	X[1]	0	None
0	0	0	1	S1
0	0	1	1	S2
0	1	0	1	S3
0	1	1	1	S4
1	0	0	1	S5
1	0	1	1	S6
1	1	0	1	S7
1	1	1	1	S8

[1] X means don't care.

TEST CIRCUITS
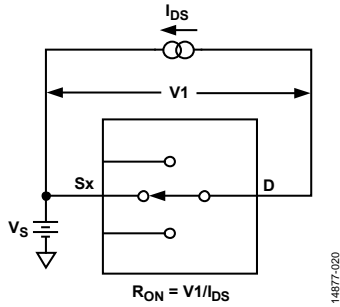
Figure 3. On Resistance
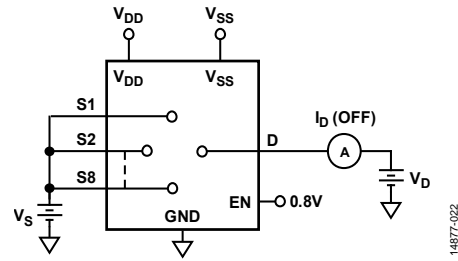
Figure 5. I_D (Off)
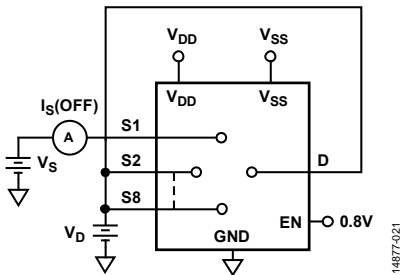
Figure 4. I_S (Off)
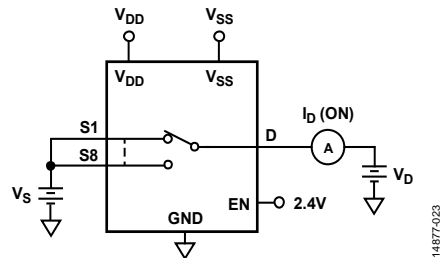
Figure 6. I_D (On)
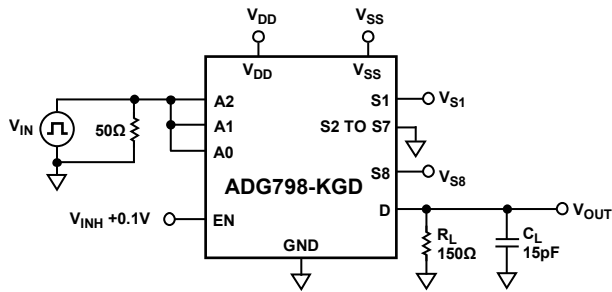
Figure 7. Switching Time of Multiplexer, $t_{TRANSITION}$
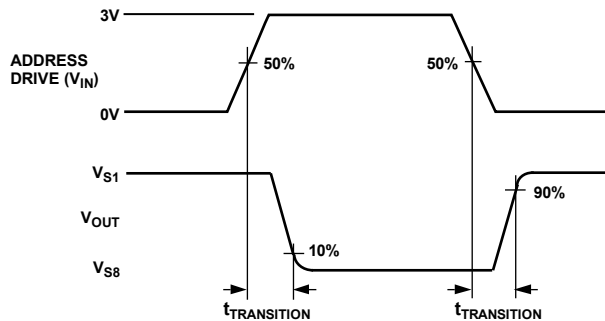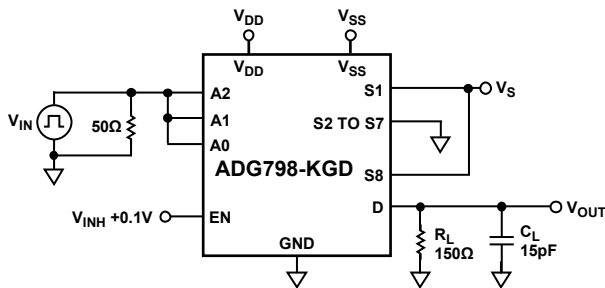
Figure 8. Break-Before-Make Delay, t_{OPEN}
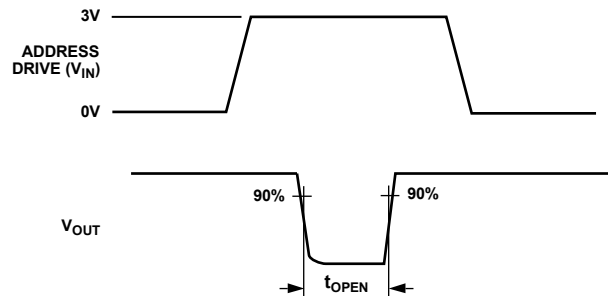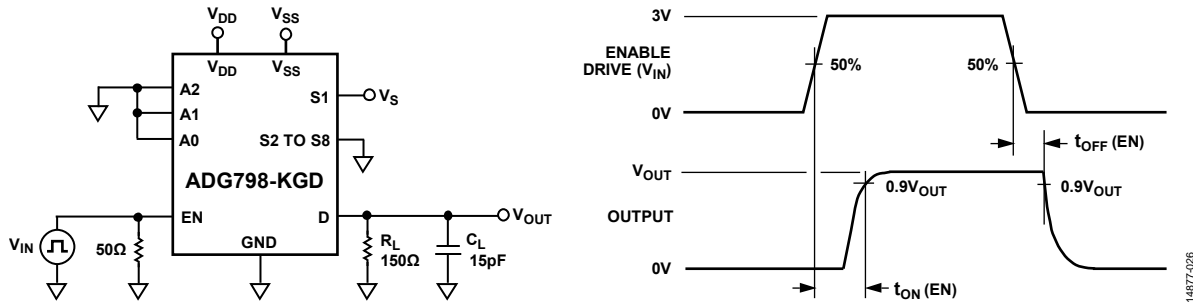
Figure 9. Enable Delay, t_{ON} (EN), t_{OFF} (EN)
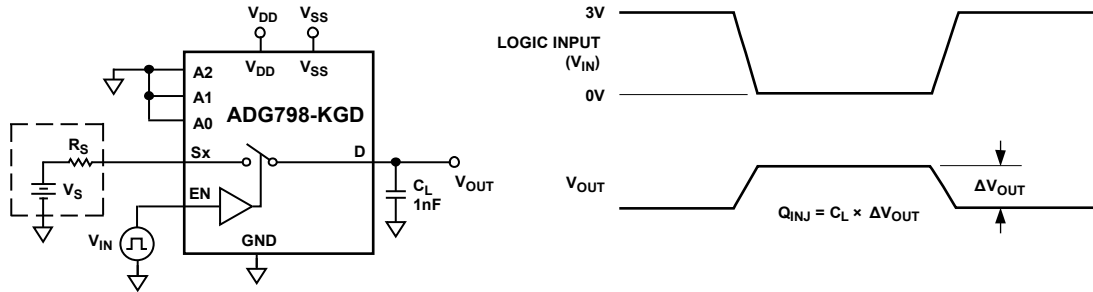
Figure 10. Charge Injection

OFF ISOLATION $= 20 \log \dfrac{V_{OUT}}{V_S}$

Figure 11. Off Isolation
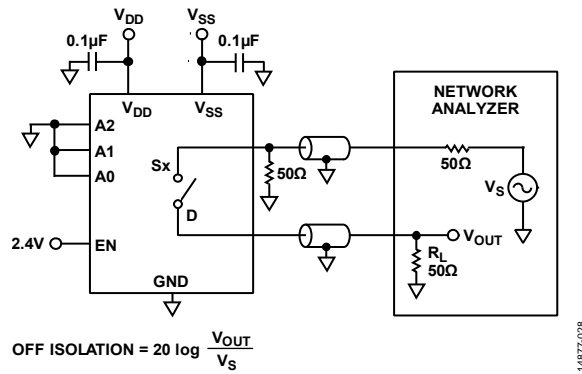
CHANNEL TO CHANNEL CROSSTALK $= 20 \log \dfrac{V_{OUT}}{V_S}$
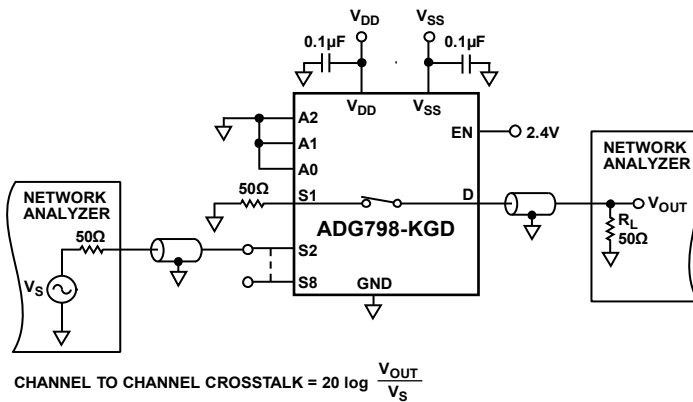
Figure 12. Channel to Channel Crosstalk
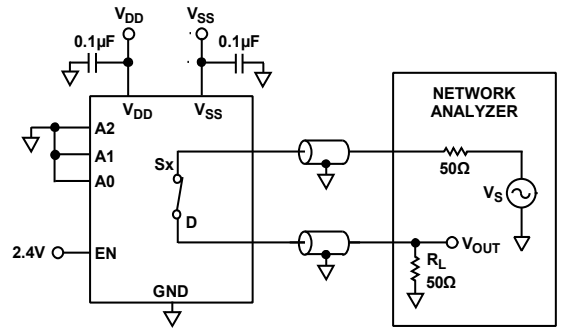
Figure 13. −3 dB Bandwidth
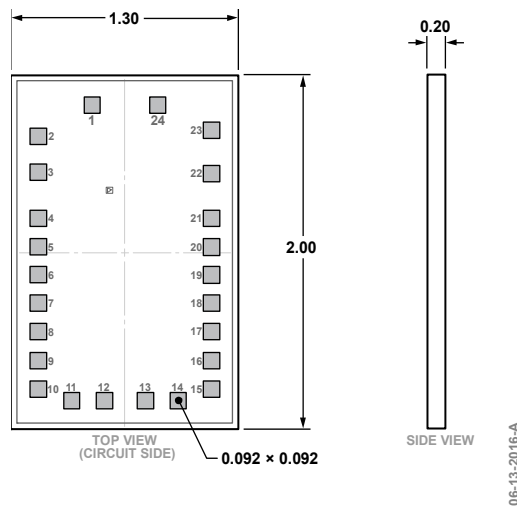
OUTLINE DIMENSIONS

Figure 14. 24-Pad Bare Die [CHIP]
(C-24-4)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 9. Die Specifications

Parameter	Value	Unit
Chip Size	1200×1850	µm
Scribe Line Width	100×150	µm
Die Size	1300×2000	µm
Thickness	200	µm
Bond Pad	92×92	µm
Bond Pad Composition	0.5 (AlCu)	%
Backside	V_{SS}	Not applicable
Passivation	Oxynitride	Not applicable

Table 10. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Bonding Method	Gold ball[1] or aluminum wedge
Bonding Sequence	Bond Pad four first

[1] Evaluate the gold wire for suitability before use at elevated temperatures for extended durations.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG798-KGD-WP	−55°C to +210°C	24-Pad Bare Die [CHIP]	C-24-4

www.analog.com