Data Sheet

ADGM1001/ADGM1002/ADGM1003

0 Hz/DC to 34 GHz, SPDT MEMS Switches

FEATURES

- ADGM1001: DC to 34 GHz
- ADGM1002: DC to 20 GHz
- ADGM1003: DC to 16 GHz
- Insertion loss (ADGM1001)
  - 0.8 dB (typical) at 18 GHz
  - 1.5 dB (typical) at 34 GHz
- IIP3: 76 dBm (typical) (ADGM1001)
- Maximum RF power: 33 dBm (ADGM1001)
- On resistance: 3.4 Ω (typical)
- Maximum dc current: 200 mA (ADGM1001)
- Actuation lifetime: 100 million cycles (minimum)
- On switching time (t_{ON}): 200 µs (typical)
- Integrated 3.3 V driver for simple control with parallel and SPI
- Independently controllable switches
- Space-saving integrated passive components
- Small, 5.00 mm × 4.00 mm × 0.90 mm, 24-lead LGA package
- Temperature range: –40°C to +85°C

APPLICATIONS

- ATE load and probe boards
- DC and high speed loop back testing
- Relay replacements
- Reconfigurable filters and attenuators
- Military and microwave radios
- Cellular infrastructure: 5G mmWave
- Supports digital standards: PCIe Gen4/Gen5/Gen6, USB 3 and USB 4, and PAM 4

FUNCTIONAL BLOCK DIAGRAM

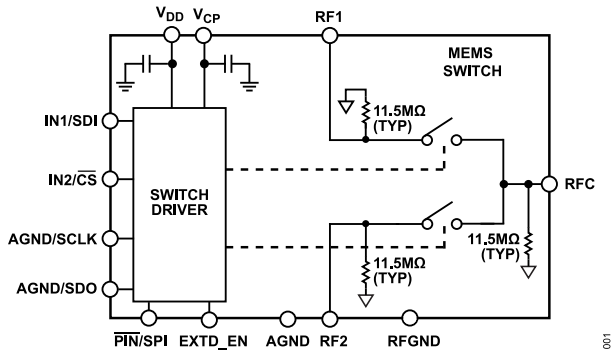

Figure 1.

GENERAL DESCRIPTION

The ADGM1001 is a wideband, single-pole, two-throw (SP2T) switch, fabricated using Analog Devices, Inc., micro-electromechanical system (MEMS) switch technology. This technology enables a small form factor, wide RF bandwidth, highly linear, low insertion loss switch that is operational down to 0 Hz/dc, making it an ideal solution for a wide range of RF and precision equipment switching needs. The device is packaged in a 24-lead, 5.00 mm × 4.00 mm × 0.90 mm, land grid array (LGA) package.

An integrated control chip generates the high voltage necessary to electrostatically actuate the switch via a complementary metal-oxide semiconductor (CMOS)-/low voltage transistor-transistor logic (LVTTL)-compatible parallel interface. All switches are independently controllable.

Multifunction pin names may be referenced by their relevant function only.

Table 1. ADGM1001/ADGM1002/ADGM1003 Key Specifications

Model	Bandwidth	Maximum RF Power (dBm)	DC Signal Range (V)	Maximum DC Current (mA)
ADGM1001	DC to 34 GHz	33	±6	200
ADGM1002	DC to 20 GHz	30	±5	150
ADGM1003	DC to 16 GHz	27	±3	75

COMPANION PRODUCTS

Quad PMU: AD5522

SP4T MEMS Switches: ADGM1304, ADGM1004

Low Noise, LDO Regulators: ADP7142, LT1962, LT3045-1

Rev. 0

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REVISION HISTORY

3/2022—Revision 0: Initial Version

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V_{DD} = 3.0 V to 3.6 V, AGND and RFGND = 0 V, and all specifications are at T_A = 25°C, unless otherwise noted.

Table 2. ADGM1001/ADGM1002/ADGM1003

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
DYNAMIC CHARACTERISTICS						
On Switching Time[3]	t_{ON}			200	µs	50% INx to 90% (0.05 dB of final insertion loss value) RFx, 50 Ω termination, −40°C to +85°C, see Figure 5 for details
Off Switching Time[3, 4]	t_{OFF}			200	µs	50% INx to 10% (0.05 dB of final insertion loss value) RFx, 50 Ω termination, –40°C to +85°C, see Figure 5 for details
Power-Up Time			4	5	ms	Vcp cap = 100 pF, –40°C to +85°C
Video Feedthrough			16		mV peak	1 MΩ termination/50 Ω termination
Actuation Frequency				2	kHz	Both switches toggled simultaneously
Internal Oscillator Frequency		8.6	10	11	MHz	
Internal Oscillator Feedthrough[5]			–123		dBm	For measurement setup details, see Note 6[6]
			–146		dBm/Hz	
CAPACITANCE PROPERTIES						At 1 MHz, includes LGA package capacitance, and the capacitance is measured with respect to ground
On Switch Channel Capacitance	C_{RF} On		3.3		pF	
Off Switch Channel Capacitance	C_{RF} Off		1.6		pF	
LEAKAGE PROPERTIES						
On Leakage		0.68	1.07	1.35	µA	RFx (off channels) = +6 V, RFC/RFx (on channel) = –6 V, maximum value tested from –40°C to +85°C
Off Leakage		0.34	0.54	0.69	µA	RFx = +6 V, RFC = –6 V, maximum value tested from –40°C to +85°C
Internal Shunt Resistor		8.7	11.5	15.2	MΩ	Typical temperature coefficient = 27.5 kΩ/°C, maximum and minimum value tested at 25°C
DIGITAL INPUTS						Minimum and maximum over –40°C to +85°C
Input High Voltage	V_{INH}	2			V	
Input Low Voltage	V_{INL}			0.8	V	
Input High and Low Current	I_{INL}/I_{INH}		0.025	1	µA	V_{IN} = V_{INL} or V_{INH}
Capacitance			5		pF	
DIGITAL OUTPUTS						Minimum and maximum over –40°C to +85°C
Output Low Voltage	V_{OL}			0.4	V_{MAX}	Sink current (I_{SINK}) = 1 mA
Output High Voltage	V_{OH}	V_{DD} – 0.4			V_{MIN}	Source current (I_{SOURCE}) = 1 mA
Capacitance			5		pF	
POWER REQUIREMENTS						Minimum and maximum over –40°C to +85°C
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}		2	2.5	mA	Digital inputs = 0 V or V_{DD}, SDO floating in SPI mode
Low Power Mode Current[7]	$I_{DD\ EXT\ VCP}$			50	µA	This value is I_{DD} in low power mode
External Drive Voltage[8]	VCP_{EXT}	79.2	80	80.8	V	
External Drive Current	$I_{CP\ EXT\ VCP}$			5	µA	

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.

[2] RFx is RF1 or RF2. INx is IN1 or IN2.

[3] Switch is settled after 200 µs. Do not apply RF power between 0 µs to 200 µs.

[4] RF power must be removed or less than 5 dBm, 50 µs prior to turning the switch off.

[5] Disable the internal oscillator to eliminate feedthrough.

SPECIFICATIONS

Table 2. ADGM1001/ADGM1002/ADGM1003

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]

[6] Spectrum analyzer setup: resolution bandwidth (RBW) = 200 Hz, video bandwidth (VBW) = 2 Hz, span = 100 kHz, input attenuator = 0 dB, detector type = peak, maximum hold = off. Measurements taken with one switch on and off switch port terminated into 50 Ω. The fundamental feedthrough noise or harmonic thereof is tested (whichever is the highest).

[7] For more details, see the Low Power Mode section.

[8] For more details, see the Internal Oscillator Feedthrough Mitigation section.

ADGM1001 SPECIFICATIONS

Table 3. ADGM1001

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
ON-RESISTANCE PROPERTIES						
Initial On-Resistance Properties						
On Resistance	R_{ON}		3.4	6.5	Ω	Drain source current (I_{DS}) = 50 mA, 0 V input bias at 1 ms after first actuation, maximum specification from –40°C to +85°C
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			1.1	Ω	Maximum value tested from –40°C to +85°C at Time 0 (T0)
On-Resistance Drift						
Over Time	$\Delta R_{ON\ TIME}$			–0.46	Ω	R_{ON} changed from 1 ms to 100 ms after first actuation, maximum value tested from 25°C to 85°C
Over Actuations	ΔR_{ON}		–0.7		Ω	After 10^6 actuations, switch is actuated at 25°C, and R_{ON} is measured at 25°C
			–1		Ω	After 100 × 10^6 actuations, switch is actuated at 25°C, and R_{ON} is measured at 25°C
				–2.3	Ω	After 7 × 10^6 actuations, switch is actuated at 85°C, R_{ON} is measured at 25°C, and actuation frequency = 1 Hz
				3	Ω	After 100 × 10^6 actuations, switch is actuated at 85°C, R_{ON} is measured at 25°C, and actuation frequency = 289 Hz
LIFETIME PROPERTIES						
Continuously On Lifetime			10		Years	Time before failure[3] at 85°C
Actuation Lifetime						
Cold Switched		100 × 10^6	500 × 10^6		Actuations	Load between toggling is 220 mA, tested at 85°C
RF Hot Switched						RF power = continuous wave, terminated into 50 Ω, 50% of test population failure point (T50)
7 dBm			1 × 10^9		Actuations	
10 dBm			60 × 10^6		Actuations	
15 dBm			4 × 10^6		Actuations	
20 dBm			23 × 10^3		Actuations	
DC Hot Switched						Terminated into 50 Ω, RFx load capacitance = 10 µF, 50% of test population failure point (T50)
0.5 V or 9 mA			1 × 10^9		Actuations	
1 V or 18 mA			650 × 10^6		Actuations	
2.5 V or 46 mA			55 × 10^3		Actuations	
3.5 V or 65 mA			6.5 × 10^3		Actuations	
5 V or 93 mA			2.5 × 10^3		Actuations	

SPECIFICATIONS

Table 3. ADGM1001

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
DYNAMIC CHARACTERISTICS						
–3 dB Frequency			39		GHz	
Operational Frequency Range		0		34	GHz	RFx to RFC
Insertion Loss			0.5		dB	DC to 6 GHz, RFC to RFx
			0.8		dB	6 GHz to 18 GHz, RFC to RFx
			1.4		dB	18 GHz to 30 GHz, RFC to RFx
			1.5		dB	30 GHz to 34 GHz, RFC to RFx
Isolation			32		dB	DC to 6 GHz, RFC to RFx
			23		dB	6 GHz to 18 GHz, RFC to RFx
			21		dB	18 GHz to 30 GHz, RFC to RFx
			19		dB	30 GHz to 34 GHz, RFC to RFx
Crosstalk			33		dB	DC to 6 GHz, RFC to RFx
			25		dB	6 GHz to 18 GHz; RFC to RFx
			19		dB	18 GHz to 30 GHz; RFC to RFx
			18		dB	30 GHz to 34 GHz; RFC to RFx
Return Loss			19		dB	DC to 6 GHz; RFC to RFx
			18		dB	6 GHz to 18 GHz; RFC to RFx
			16		dB	18 GHz to 30 GHz; RFC to RFx
			16		dB	30 GHz to 34 GHz; RFC to RFx
Input Third-Order Intermodulation Intercept	IIP3		65.5		dBm	Input: 900 MHz and 901 MHz, input power (P_{IN}) = 27 dBm
			76		dBm	Input: 2110 MHz and 2170 MHz, 3510 MHz and 3570 MHz, and P_{IN} = 30 dBm
Input Second-Order Intermodulation Intercept	IIP2		127		dBm	Input: 900 MHz and 901 MHz (P_{IN} = 27 dBm), 2110 MHz and 2170 MHz, 3510 MHz and 3570 MHz, and P_{IN} = 30 dBm
Second Harmonic Distortion	HD2		–92		dBc	Input: 5 MHz and P_{IN} = 0 dBm
			–88		dBc	Input: 150 MHz, 800 MHz, and P_{IN} = 33 dBm
Third Harmonic Distortion	HD3		–83		dBc	Input: 150 MHz, 800 MHz, and P_{IN} = 33 dBm
Total Harmonic Distortion	THD		–114		dBc	Load resistance (R_L) = 300 Ω, frequency = 1 kHz, and RFx = 2.5 V p-p
Total Harmonic Distortion Plus Noise	THD + N		–111		dBc	R_L = 300 Ω, frequency = 1 kHz, and RFx = 2.5 V p-p
Maximum RF Power				33	dBm	50 Ω termination
DC Signal Range		–6		6	V	On switch dc input bias voltage signal range, –40°C to +85°C
Stand Off Voltage		–6		+6	V	–40°C to +85°C, this specification is applied when the switch is in the off position with no RF signal applied
Maximum DC Current				200	mA	–40°C to +85°C

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.

[2] RFx is RF1 or RF2. INx is IN1 or IN2.

[3] This value shows the time it takes for 1% of a sample lot to fail.

SPECIFICATIONS

ADGM1002 SPECIFICATIONS

Table 4. ADGM1002

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
ON-RESISTANCE PROPERTIES						
Initial On-Resistance Properties						
On Resistance	R_{ON}		3.4	6.5	Ω	I_{DS} = 50 mA, 0 V input bias at 1 ms after first actuation, maximum specification from –40°C to +85°C
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			1.1	Ω	Maximum value tested from –40°C to +85°C at T0
On-Resistance Drift						
Over Time	$\Delta R_{ON\ TIME}$			–0.46	Ω	R_{ON} changed from 1 ms to 100 ms after first actuation, maximum value tested from 25°C to 85°C
Over Actuations	ΔR_{ON}		–0.7		Ω	After 10^6 actuations, switch is actuated at 25°C, and R_{ON} is measured at 25°C
			–1		Ω	After 100 × 10^6 actuations, switch is actuated at 25°C, and R_{ON} is measured at 25°C
				–2.3	Ω	After 7 × 10^6 actuations, switch is actuated at 85°C, R_{ON} is measured at 25°C, and actuation frequency = 1 Hz
				3	Ω	After 100 × 10^6 actuations, switch is actuated at 85°C, R_{ON} is measured at 25°C, and actuation frequency = 289 Hz
LIFETIME PROPERTIES						
Continuously On Lifetime			10		Years	Time before failure[3] at 85°C
Actuation Lifetime						
Cold Switched		100 × 10^6	500 × 10^6		Actuations	Load between toggling is 150 mA, tested at 85°C
RF Hot Switched						RF power = continuous wave, terminated into 50 Ω, 50% of test population failure point (T50)
7 dBm			1 × 10^9		Actuations	
10 dBm			60 × 10^6		Actuations	
15 dBm			4 × 10^6		Actuations	
20 dBm			23 × 10^3		Actuations	
DC Hot Switched						Terminated into 50 Ω, RFx load capacitance = 10 µF, 50% of test population failure point (T50)
0.5 V or 9 mA			1 × 10^9		Actuations	
1 V or 18 mA			650 × 10^6		Actuations	
2.5 V or 46 mA			55 × 10^3		Actuations	
3.5 V or 65 mA			6.5 × 10^3		Actuations	
5 V or 93 mA			2.5 × 10^3		Actuations	
DYNAMIC CHARACTERISTICS						
Frequency Range		0		20	GHz	RFx to RFC
Insertion Loss			0.5		dB	DC to 6 GHz, RFC to RFx
			0.6		dB	6 GHz to 10 GHz, RFC to RFx
			0.9		dB	10 GHz to 20 GHz, RFC to RFx
Isolation			32		dB	DC to 6 GHz, RFC to RFx
			28		dB	6 GHz to 10 GHz, RFC to RFx
			23		dB	10 GHz to 20 GHz, RFC to RFx

SPECIFICATIONS

Table 4. ADGM1002

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
Crosstalk			33		dB	DC to 6 GHz, RFC to RFx
			29		dB	6 GHz to 10 GHz, RFC to RFx
			24		dB	10 GHz to 20 GHz, RFC to RFx
Return Loss			19		dB	DC to 6 GHz, RFC to RFx
			18		dB	6 GHz to 10 GHz, RFC to RFx
			18		dB	10 GHz to 20 GHz, RFC to RFx
Input Third-Order Intermodulation Intercept	IIP3		65.5		dBm	Input: 900 MHz and 901 MHz, and P_{IN} = 27 dBm
			76		dBm	Input: 2110 MHz and 2170 MHz, 3510 MHz and 3570 MHz, and P_{IN} = 30 dBm
Input Second-Order Intermodulation Intercept	IIP2		127		dBm	Input: 900 MHz and 901 MHz (P_{IN} = 27 dBm), 2110 MHz and 2170 MHz, 3510 MHz and 3570 MHz, and P_{IN} = 30 dBm
Second Harmonic Distortion	HD2		–92		dBc	Input: 5 MHz and P_{IN} = 0 dBm
			–88		dBc	Input: 150 MHz and 800 MHz, and P_{IN} = 30 dBm
Third Harmonic Distortion	HD3		–83		dBc	Input: 150 MHz and 800 MHz, and P_{IN} = 30 dBm
Total Harmonic Distortion	THD		–114		dBc	R_L = 300 Ω, frequency = 1 kHz, and RFx = 2.5 V p-p
Total Harmonic Distortion Plus Noise	THD + N		–111		dBc	R_L = 300 Ω, frequency = 1 kHz, and RFx = 2.5 V p-p
Maximum RF Power				30	dBm	50 Ω termination
DC Signal Range		–5		5	V	On switch dc input bias voltage signal range, –40°C to +85°C
Stand Off Voltage		–5		+5	V	–40°C to +85°C, this specification is applied when the switch is in the off position with no RF signal
Maximum DC Current				150	mA	–40°C to +85°C

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.

[2] RFx is RF1 or RF2. INx is IN1 or IN2.

[3] This value shows the time it takes for 1% of a sample lot to fail.

ADGM1003 SPECIFICATIONS

Table 5. ADGM1003

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
ON-RESISTANCE PROPERTIES						
Initial On-Resistance Properties						
On Resistance	R_{ON}		3.4		Ω	I_{DS} = 50 mA, 0 V input bias at 1 ms after first actuation, maximum specification from –40°C to +85°C
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			1.1	Ω	Maximum value tested from –40°C to +85°C at T0
On-Resistance Drift						
Over Time	$\Delta R_{ON\ TIME}$		–0.15		Ω	R_{ON} changed from 1 ms to 100 ms after first actuation, maximum value tested from –40°C to +85°C
Over Actuations	ΔR_{ON}		–0.7		Ω	After 10^6 actuations, switch is actuated at 25°C, and R_{ON} is measured at 25°C
			–1		Ω	After 100 × 10^6 actuations, switch is actuated at 25°C, and R_{ON} is measured at 25°C

SPECIFICATIONS

Table 5. ADGM1003

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
RELIABILITY PROPERTIES						
Continuously On Lifetime			10		Years	Time before failure[3] at 85°C
Actuation Lifetime						
Cold Switched			100×10^6		Actuations	Load between toggling is 75 mA, tested at 85°C
Hot Switched			0		dBm	
DYNAMIC CHARACTERISTICS						
Frequency Range		0		16	GHz	RFx to RFC
Insertion Loss			0.5		dB	DC to 6 GHz, RFC to RFx
			0.6		dB	6 GHz to 10 GHz, RFC to RFx
			0.7		dB	10 GHz to 16 GHz, RFC to RFx
Isolation			32		dB	DC to 6 GHz, RFC to RFx
			28		dB	6 GHz to 10 GHz, RFC to RFx
			24		dB	10 GHz to 16 GHz, RFC to RFx
Crosstalk			33		dB	DC to 6 GHz, RFC to RFx
			29		dB	6 GHz to 10 GHz, RFC to RFx
			25		dB	10 GHz to 16 GHz, RFC to RFx
Return Loss			19		dB	DC to 6 GHz, RFC to RFx
			18		dB	6 GHz to 10 GHz, RFC to RFx
			18		dB	10 GHz to 16 GHz, RFC to RFx
Total Harmonic Distortion	THD		–114		dBc	R_L = 300 Ω, frequency = 1 kHz, and RFx = 2.5 V p-p
Total Harmonic Distortion Plus Noise	THD + N		–111		dBc	R_L = 300 Ω, frequency = 1 kHz, and RFx = 2.5 V p-p
Maximum RF Power				27	dBm	50 Ω termination
DC Signal Range		–3		+3	V	On switch dc input bias voltage signal range, –40°C to +85°C
Stand Off Voltage		–3		+3	V	–40°C to +85°C, this specification is applied when the switch is in the off position with no RF signal applied
Maximum DC Current				75	mA	–40°C to +85°C

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.

[2] RFx is RF1 or RF2. INx is IN1 or IN2.

[3] This value shows the time it takes for 1% of a sample lot to fail.

SPECIFICATIONS

TIMING CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V, AGND and RFGND = 0 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization, not production tested.

Table 6.

Parameter	Limit at T_{MIN} or T_{MAX}	Unit	Description
t_1	100	ns min	SCLK period
t_2	45	ns min	SCLK high pulse width
t_3	45	ns min	SCLK low pulse width
t_4	25	ns min	$\overline{CS}$ falling edge to SCLK active edge
t_5	20	ns min	Data setup time
t_6	20	ns min	Data hold time
t_7	25	ns min	SCLK active edge to $\overline{CS}$ rising edge
t_8	20	ns max	$\overline{CS}$ falling edge to SDO data available
t_9[1]	40	ns max	SCLK falling edge to SDO data available
t_{10}	25	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
t_{11}	100	ns min	$\overline{CS}$ high time between SPI commands
t_{12}	25	ns min	SCLK edge rejection to $\overline{CS}$ falling edge
t_{13}	25	ns min	$\overline{CS}$ rising edge to SCLK edge rejection

[1] Measured with a 20 pF load. t_9 determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

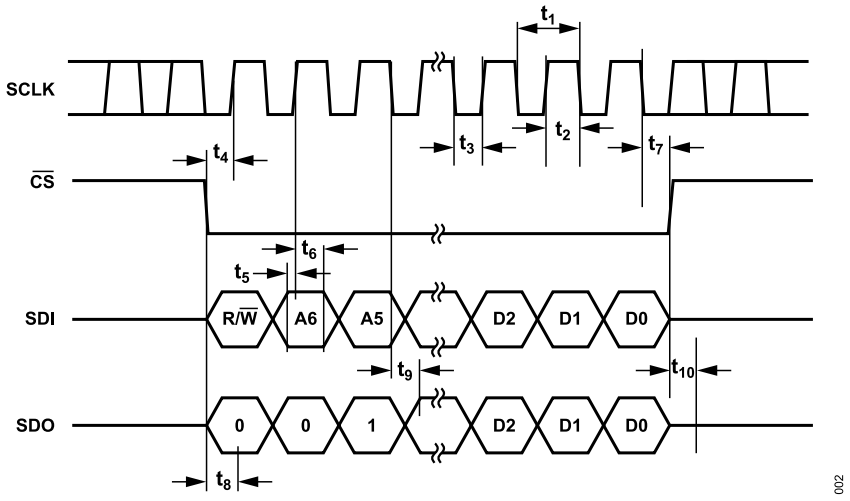

Figure 2. Addressable Mode Timing Diagram

SPECIFICATIONS

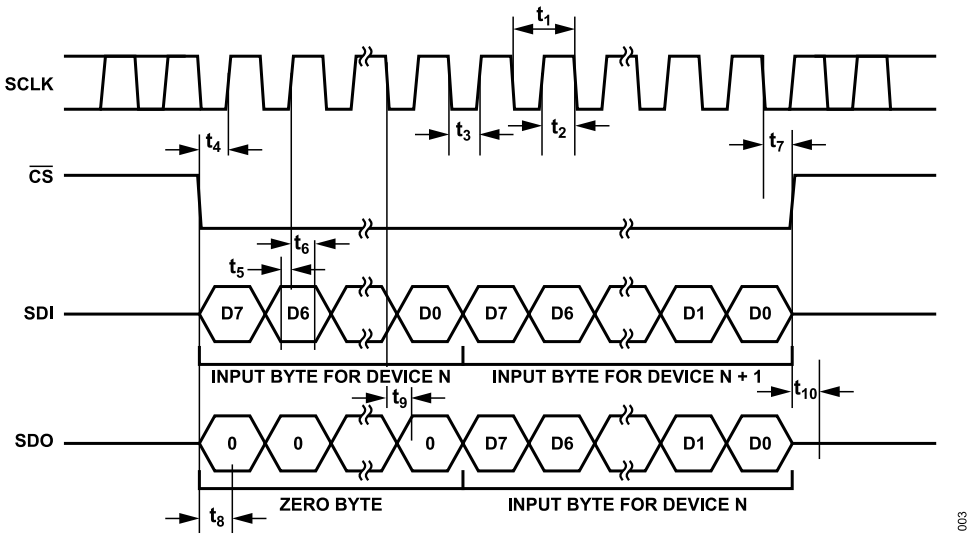

Figure 3. Daisy-Chain Timing Diagram

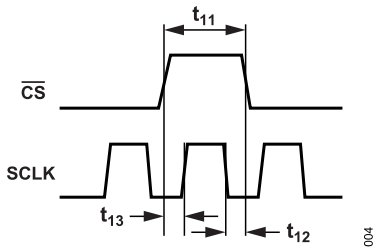

Figure 4. SCLK and CS Timing Relationship

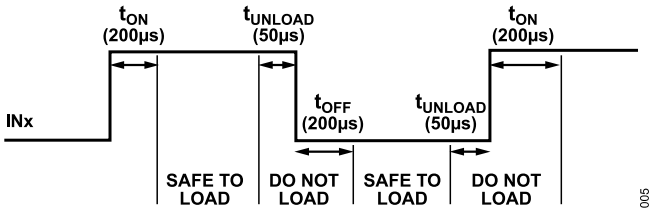

Figure 5. Switch Loading Profile

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Switch DC Rating[2]	
ADGM1001 Voltage	±7 V
ADGM1002 Voltage	±7 V
ADGM1003 Voltage	±4 V
ADGM1001 Current	220 mA
ADGM1002 Current	175 mA
ADGM1003 Current	100 mA
VCP_{EXT}	82 V
Stand Off Voltage[3]	
ADGM1001	±10 V
ADGM1002	±8 V
ADGM1003	±6 V
RF Power Rating[4]	
ADGM1001	34 dBm
ADGM1002	31 dBm
ADGM1003	28 dBm
Group D	
Mechanical Shock[5]	1500 *g* with 0.5 ms pulse
Vibration	20 Hz to 2000 Hz acceleration at 50 *g*
Constant Acceleration	30,000 g
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Reflow Soldering (Pb-Free)	
Peak	+260(+0/−5)°C
Time at Peak Temperature	10 sec to 30 sec

[1] Clamp overvoltages at INx by internal diodes. Limit the current to the maximum ratings shown.

[2] This rating is applied when the switch in the on position with no RF signal applied.

[3] This rating is with respect to the switch in the off position with no RF signal applied.

[4] This rating is with respect to the switch in the on position and terminated into 50 Ω.

[5] If a device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JCT} is the junction to the top of the case thermal resistance.

θ_{JCB} is the junction to the bottom of the case thermal resistance.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JCT}	θ_{JCB}	Unit
24-Lead LGA	161.54	155.81	123.5	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADGM1001/ADGM1002/ADGM1003

Table 9. ADGM1001/ADGM1002/ADGM1003, 24-Lead LGA

ESD Model	Withstand Threshold
HBM[1]	150 V 150 V for the RF1, RF2, and RFC pins 2 kV for all other pins
FICDM[2]	500 V

[1] Take proper precautions during handling as outlined in the Handling Precautions section.

[2] A safe automated handling and assembly process is achieved at this rating level by implementing industry-standard ESD controls.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

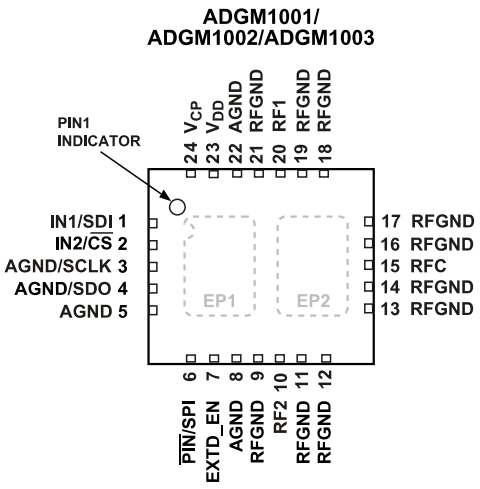

Figure 6. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1/SDI	Parallel Logic Digital Control Input 1. The voltage applied to the IN1 pin controls the gate of the MEMS switch RF1 to RFC. In SPI mode, this is the serial data input pin (SDI).
2	IN2/$\overline{CS}$	Parallel Logic Digital Control Input 2. The voltage applied to the IN2 pin controls the gate of the MEMS switch RF2 to RFC. In SPI mode, this is the chip select pin ($\overline{CS}$).
3	AGND/SCLK	In parallel logic control mode, the AGND pin must be connected to ground. In SPI mode, this is the serial clock input pin (SCLK).
4	AGND/SDO	In parallel logic control mode, the AGND pin must be connected to ground. In SPI mode, this is the serial data output pin (SDO).
5, 8, 22	AGND	Analog Ground Connection (Recommended to Connect AGND and RFGND Together).
6	$\overline{PIN}$/SPI	Parallel or Serial Logic Control Enable Pin ($\overline{PIN}$). When this pin is high, SPI enables, and when this pin is low, the parallel (IN1 and IN2) interface enables.
7	EXTD_EN	External Voltage Drive Enable. In normal operation, set EXTD_EN low to enable the built-in 10 MHz oscillator to enable the internal driver IC voltage boost circuitry. Setting EXTD_EN high disables the internal 10 MHz oscillator and driver boost circuitry. Disabling the internal oscillator eliminates any associated noise feedthrough. With the oscillator disabled, the switch can still be controlled via the logic interface pins (IN1 and IN2), but the V_{CP} pin must be driven with 80 V dc from an external voltage supply.
9, 11 to 14, 16 to 19, 21	RFGND	RF Ground Connection (Recommended to Connect AGND and RFGND Together).
10	RF2	RF2 Port. The RF2 pin can be an input or an output. If unused, the RF2 pin must be connected to GND or terminate the RF2 pin with a 50 Ω resistor to RFGND.
15	RFC	Common RF Port. The RFC pin can be an input or an output.
20	RF1	RF1 Port. The RF1 pin can be an input or an output. If unused, the RF1 pin must be connected to GND or terminate the RF1 pin with a 50 Ω resistor to RFGND.
23	V_{DD}	Positive Power Supply Input. For the recommend input voltage, see Table 3. No external ac decoupling capacitors are needed because these capacitors are integrated into the package. When no supply voltage is applied to the power supply input, all switches are in an indeterminate state.
24	V_{CP}	Driver IC Input and Output. In normal operating mode, V_{CP} outputs 80 V dc and do not load this pin externally because there is an internal decoupling capacitor connected to ground in the package. If the EXTD_EN pin is high, the internal voltage boost circuity disables, and an 80 V dc voltage must be input into V_{CP} to drive the switches via the logic interface.
	EP1	Exposed Pad 1. EP1 is internally connected to AGND. Connect EP1 to AGND or to both AGND and RFGND.
	EP2	Exposed Pad 2. EP2 is internally connected to RFGND. Connect EP2 to RFGND or to both RFGND and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

ADGM1001/ADGM1002 TYPICAL PERFORMANCE CHARACTERISTICS

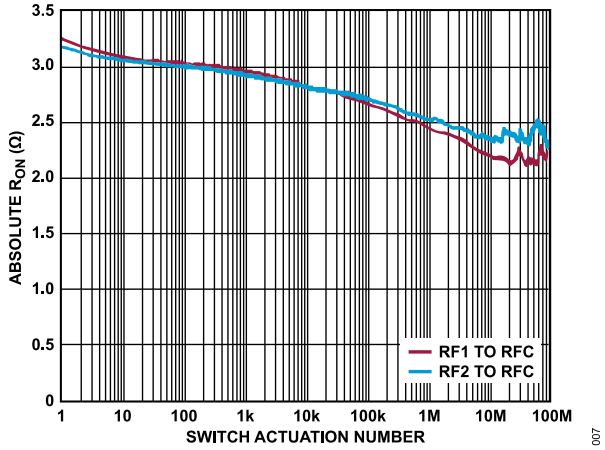

Figure 7. Absolute R_{ON} vs. Switch Actuation Number, T_A = 25°C, Load Applied During Actuations = 50 mA

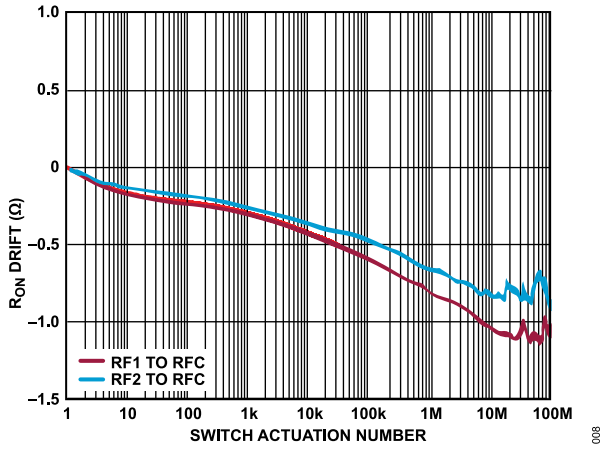

Figure 8. R_{ON} Drift vs. Switch Actuation Number, Normalized at Zero, T_A = 25°C, and Load Applied During Actuations = 50 mA

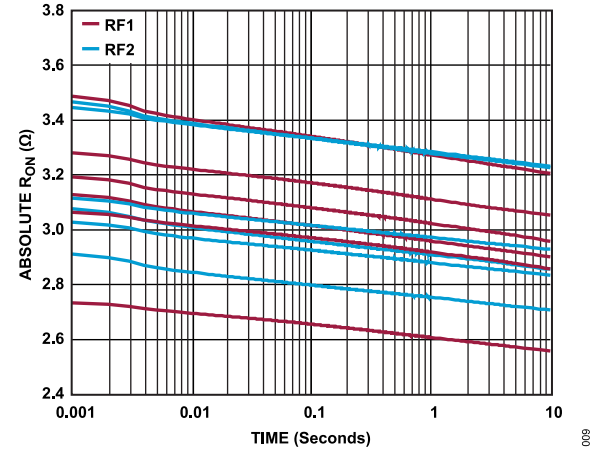

Figure 9. Absolute R_{ON} vs. Time (1 ms to 10 sec) over Different Channels, Multiple Devices, T_A = 25°C, V_{DD} = 3.3 V, Current = 50 mA

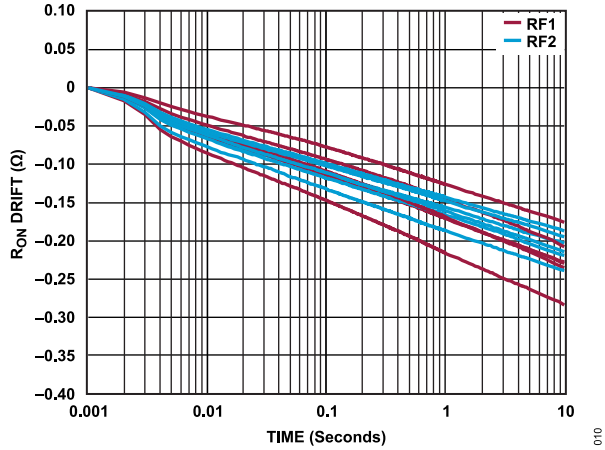

Figure 10. R_{ON} Drift vs. Time (1 ms to 10 sec) over Different Channels, Multiple Devices, Normalized at Zero, T_A = 25°C, V_{DD} = 3.3 V, Current = 50 mA

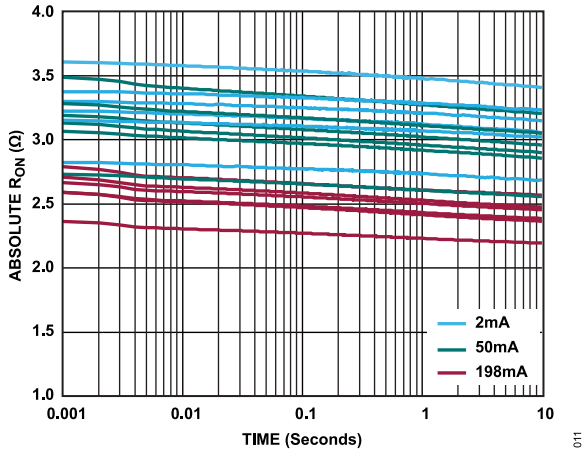

Figure 11. ADGM1001 Absolute R_{ON} vs. Time (1 ms to 10 sec) over Different Current Levels, Multiple Devices, T_A = 25°C, V_{DD} = 3.3 V, RF1 to RFC

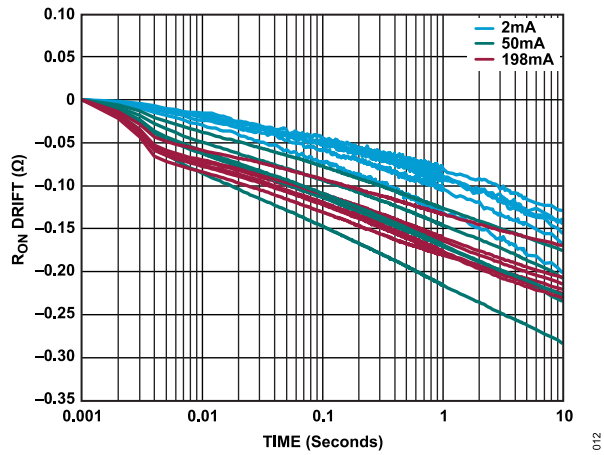

Figure 12. ADGM1001 R_{ON} Drift vs. Time (1 ms to 10 sec) over Different Current Levels, Multiple Devices, Normalized at Zero, T_A = 25°C, V_{DD} = 3.3 V, RF1 to RFC

TYPICAL PERFORMANCE CHARACTERISTICS

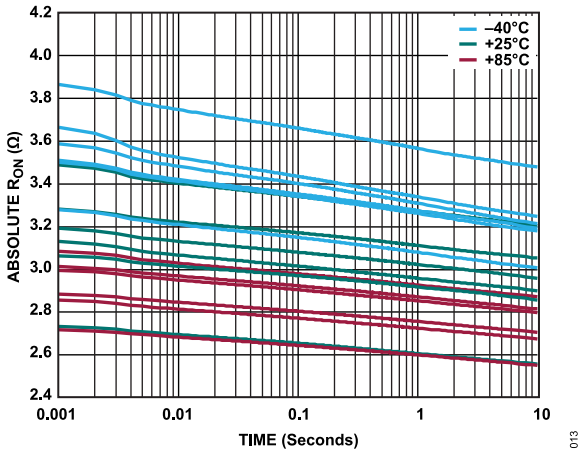

Figure 13. Absolute R_{ON} vs. Time (1 ms to 10 sec) over Temperature, Multiple Devices, Current = 50 mA, V_{DD} = 3.3 V, RF1 to RFC

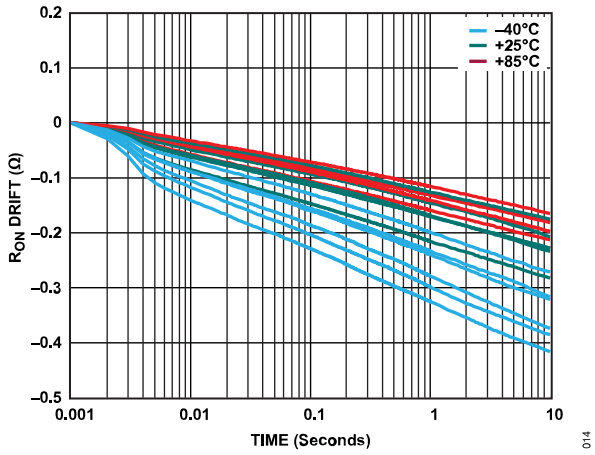

Figure 14. R_{ON} Drift vs. Time (1 ms to 10 sec) over Temperature, Multiple Devices, Normalized at Zero, Current = 50 mA, V_{DD} = 3.3 V, RF1 to RFC

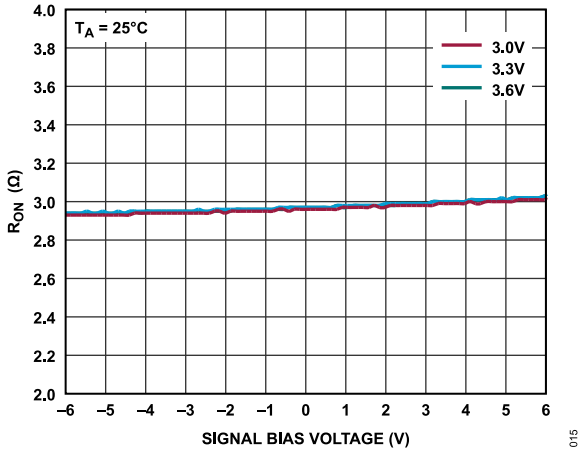

Figure 15. ADGM1001 R_{ON} vs. Signal Bias Voltage over Supply Voltages, RF1 to RFC On

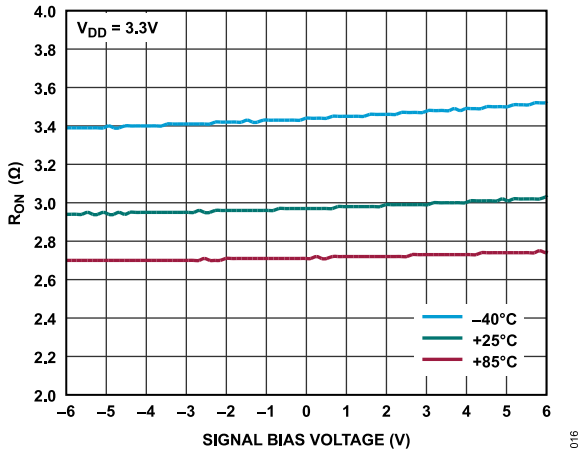

Figure 16. ADGM1001 R_{ON} vs. Signal Bias Voltage over Temperature, RF1 to RFC On

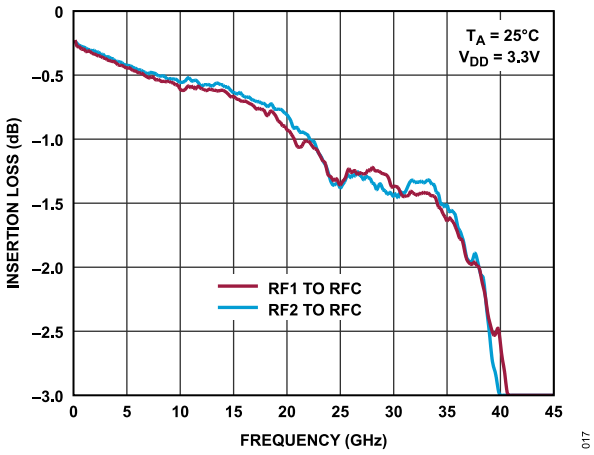

Figure 17. ADGM1001 Insertion Loss vs. Frequency, Linear Scale (V_{DD} = 3.3 V)

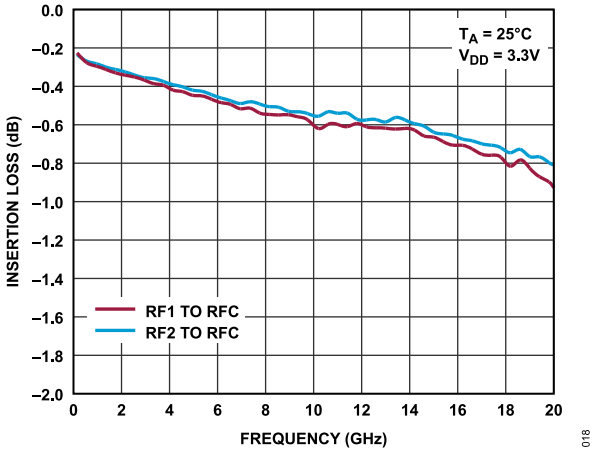

Figure 18. ADGM1002 Insertion Loss vs. Frequency, Linear Scale (V_{DD} = 3.3 V)

TYPICAL PERFORMANCE CHARACTERISTICS

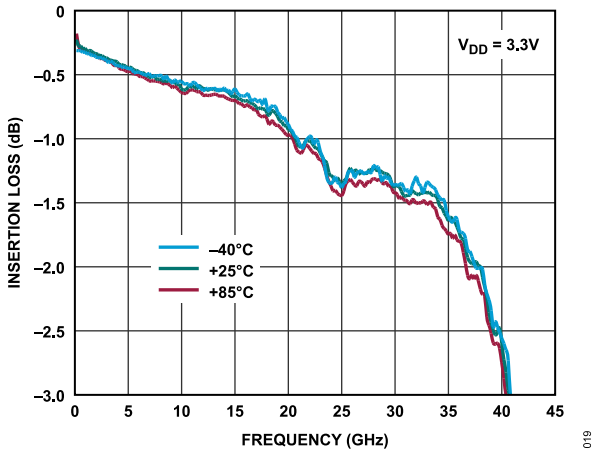

Figure 19. ADGM1001 Insertion Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

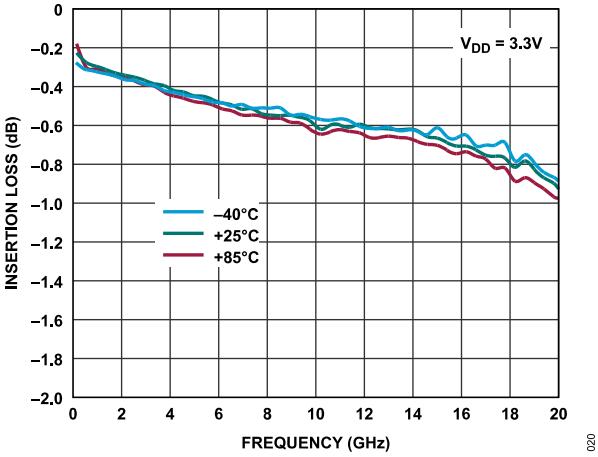

Figure 20. ADGM1002 Insertion Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

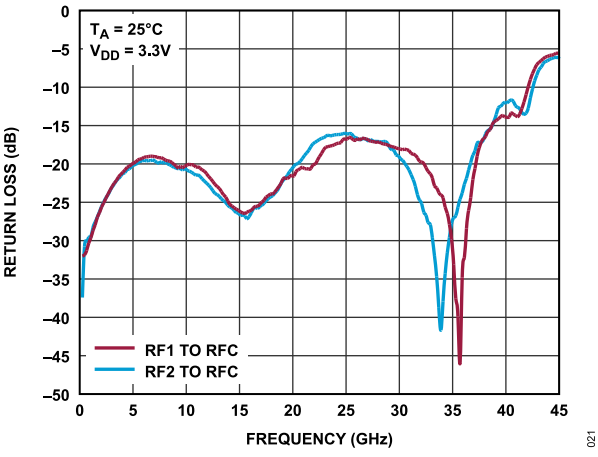

Figure 21. ADGM1001 Return Loss vs. Frequency (V_{DD} = 3.3 V)

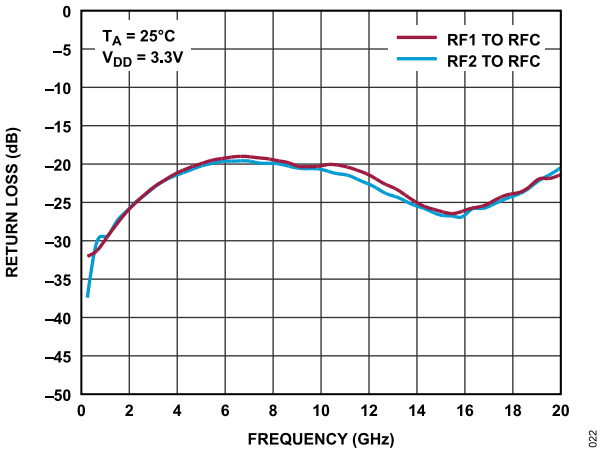

Figure 22. ADGM1002 Return Loss vs. Frequency (V_{DD} = 3.3 V)

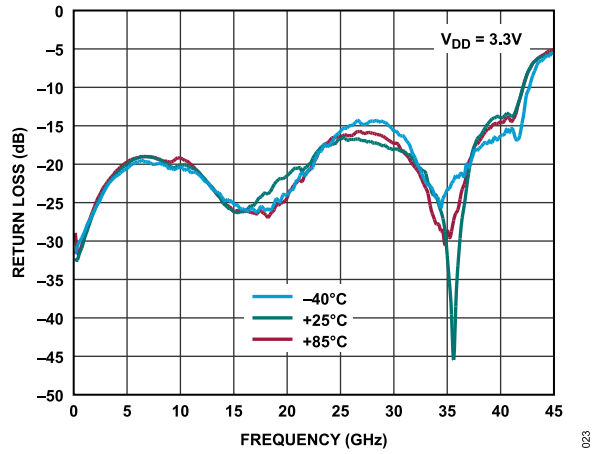

Figure 23. ADGM1001 Return Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

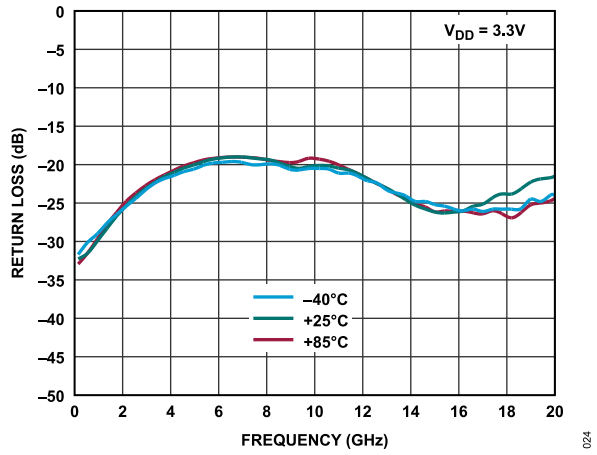

Figure 24. ADGM1002 Return Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

TYPICAL PERFORMANCE CHARACTERISTICS

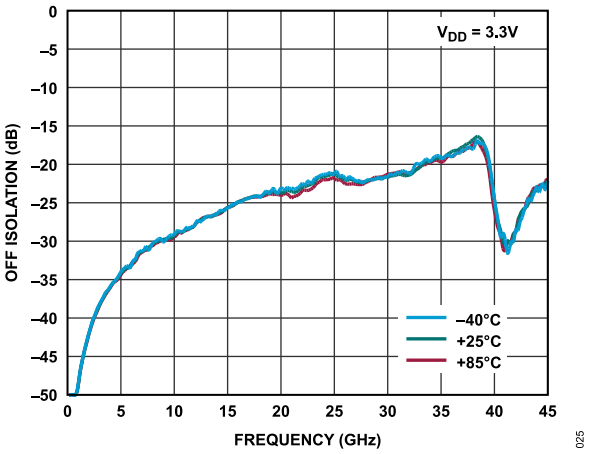

Figure 25. ADGM1001 Off Isolation vs. Frequency over Temperature, All Channels Off (V_{DD} = 3.3 V, RFx to RFC)

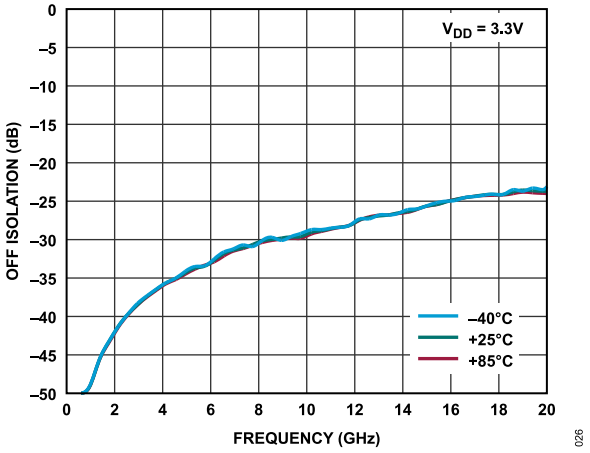

Figure 26. ADGM1002 Off Isolation vs. Frequency over Temperature, All Channels Off (V_{DD} = 3.3 V, RFx to RFC)

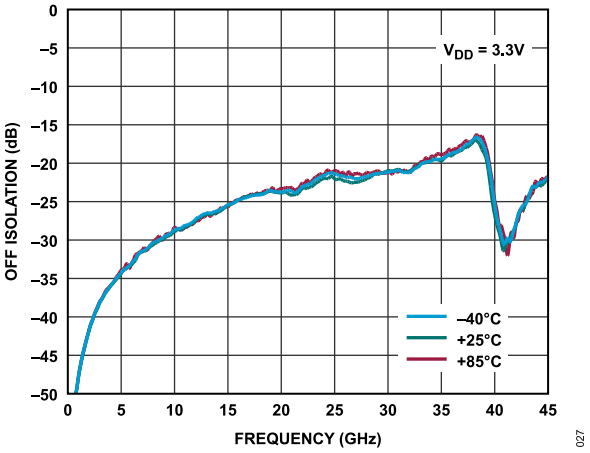

Figure 27. ADGM1001 Off Isolation vs. Frequency over Temperature, RF1 to RFC On (V_{DD} = 3.3 V)

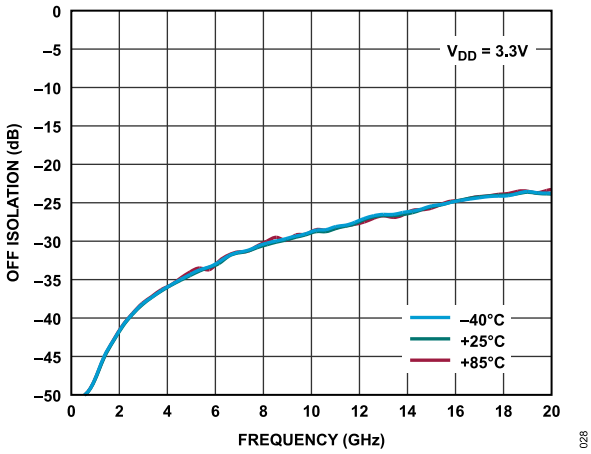

Figure 28. ADGM1002 Off Isolation vs. Frequency over Temperature, RF1 to RFC On (V_{DD} = 3.3 V)

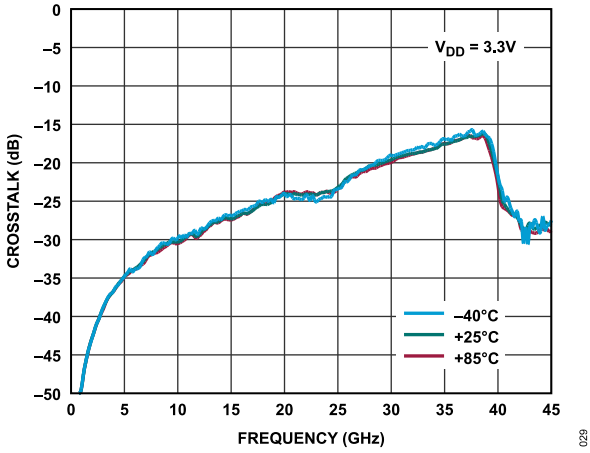

Figure 29. ADGM1001 Crosstalk vs. Frequency over Temperature (V_{DD} = 3.3 V, RFx to RFx)

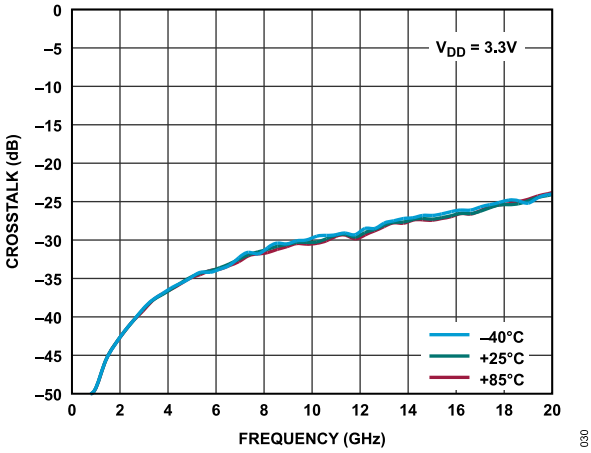

Figure 30. ADGM1002 Crosstalk vs. Frequency over Temperature (V_{DD} = 3.3 V, RFx to RFx)

TYPICAL PERFORMANCE CHARACTERISTICS

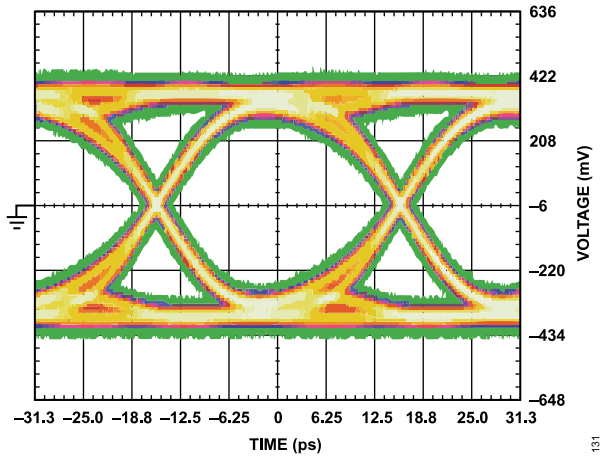

Figure 31. Reference Trace Eye Diagram at 32 Gbps (Pattern Used Pseudo Random Binary Sequence (PRBS) $2^{15} - 1$)

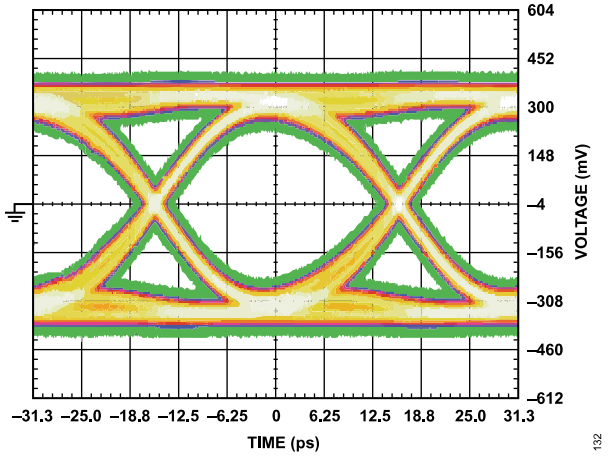

Figure 32. ADGM1001 Eye Diagram at 32 Gbps (RF1 to RFC with Reference Trace, Pattern Used PRBS $2^{15} - 1$)

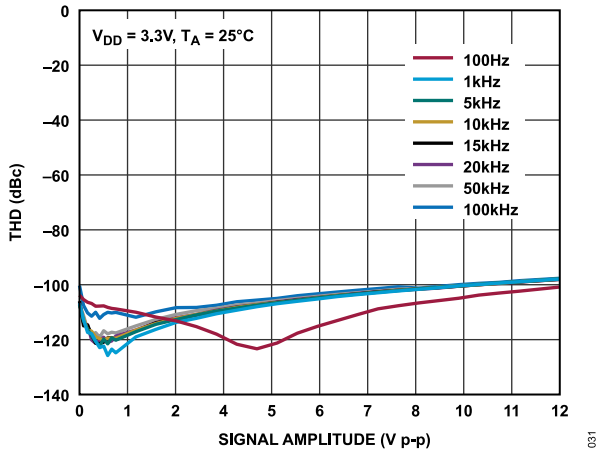

Figure 33. ADGM1001 THD vs. Signal Amplitude (V_{DD} = 3.3 V, R_L = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω)

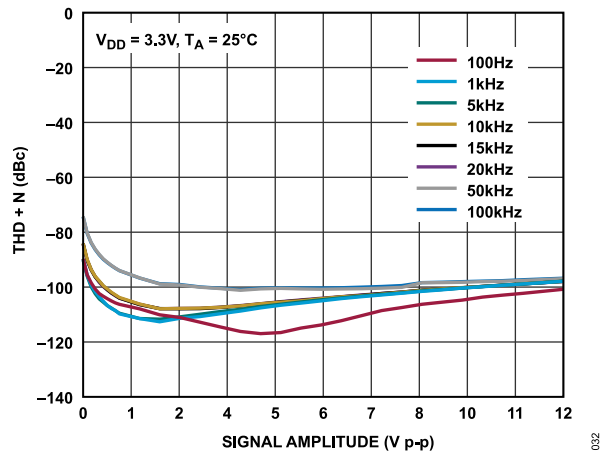

Figure 34. ADGM1001 THD + N vs. Signal Amplitude (V_{DD} = 3.3 V, R_L = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω)

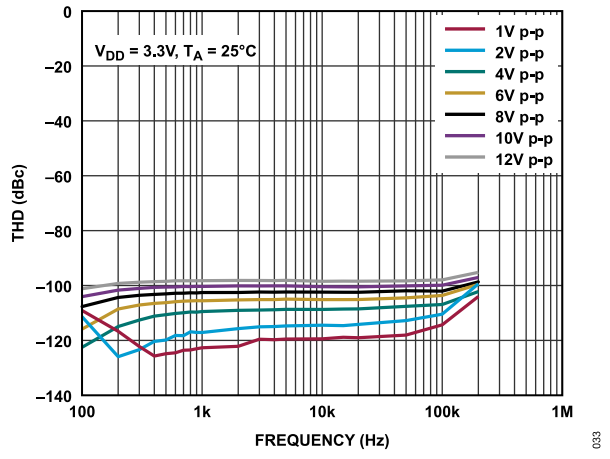

Figure 35. ADGM1001 THD vs. Frequency (V_{DD} = 3.3 V, R_L = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω)

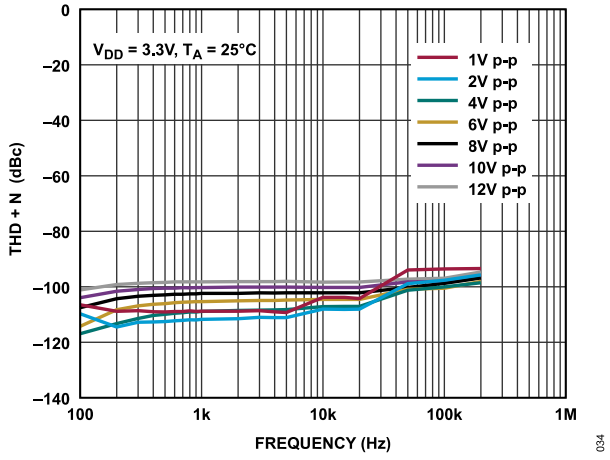

Figure 36. ADGM1001 THD + N vs. Frequency (V_{DD} = 3.3 V, R_L = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω)

TYPICAL PERFORMANCE CHARACTERISTICS

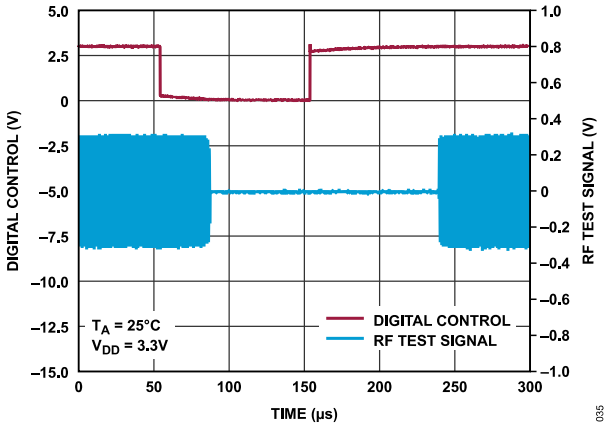

Figure 37. Digital Control and Test Signal vs. Time (V_{DD} = 3.3 V)

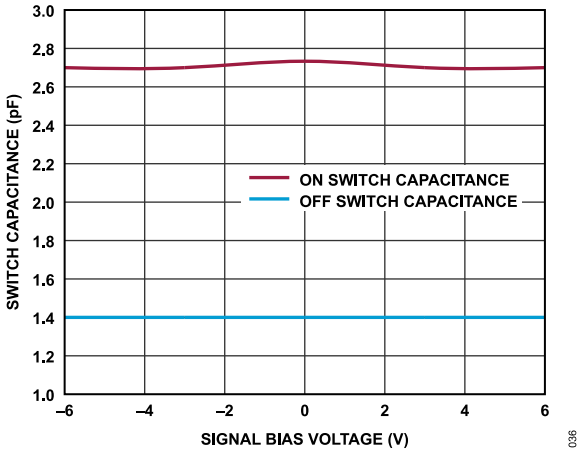

Figure 38. Switch Capacitance vs. Signal Bias Voltage

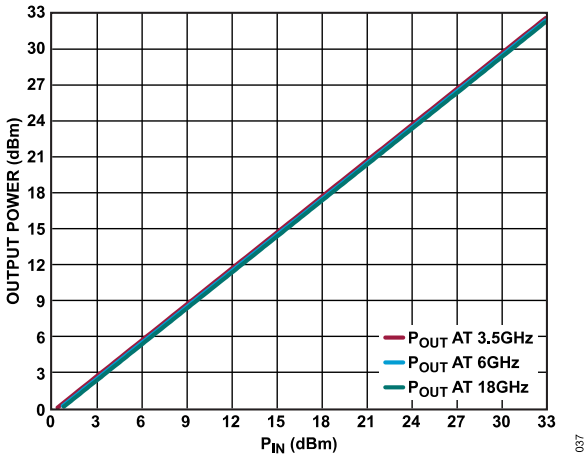

Figure 39. ADGM1001 Output Power (P_{OUT}) vs. P_{IN} (V_{DD} = 3.3 V)

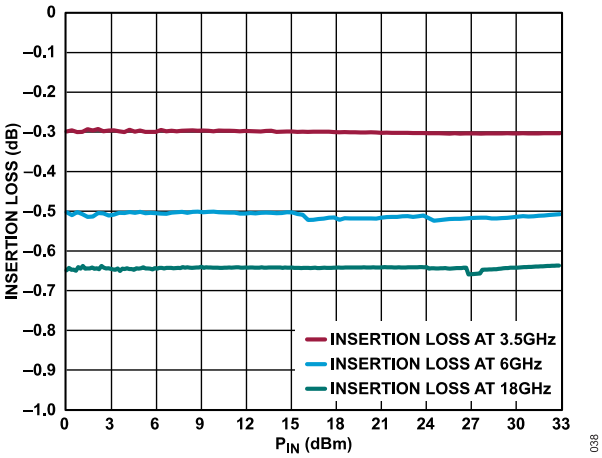

Figure 40. ADGM1001 Insertion Loss vs. P_{IN}

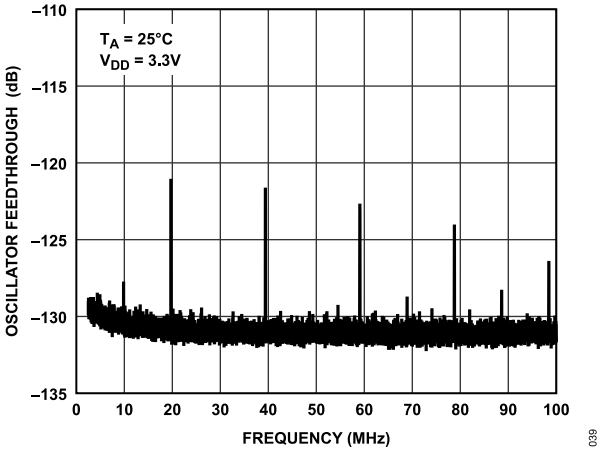

Figure 41. Oscillator Feedthrough vs. Frequency, Wide Bandwidth (V_{DD} = 3.3 V)

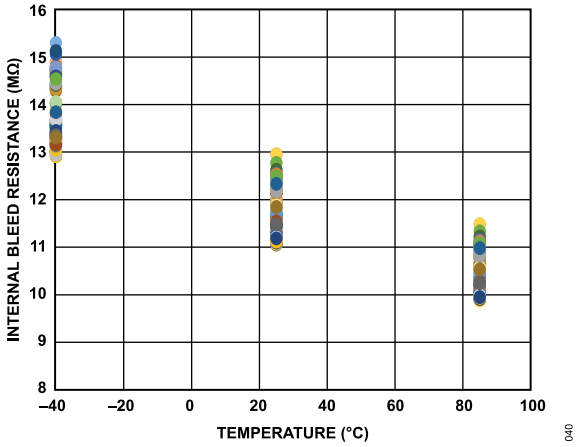

Figure 42. Internal Bleed Resistor Distribution over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

ADGM1003 TYPICAL PERFORMANCE CHARACTERISTICS

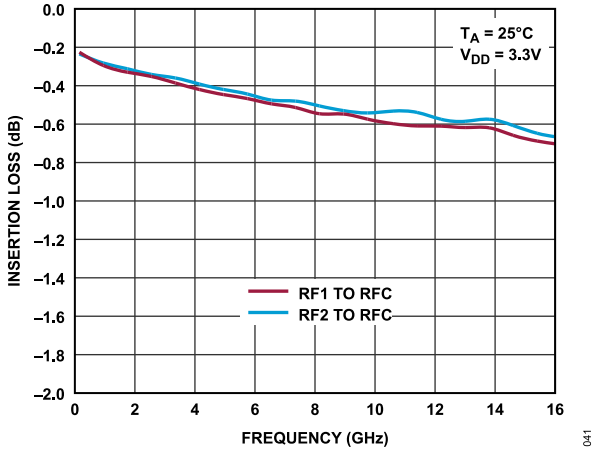

Figure 43. Insertion Loss vs. Frequency, Linear Scale (V_{DD} = 3.3 V)

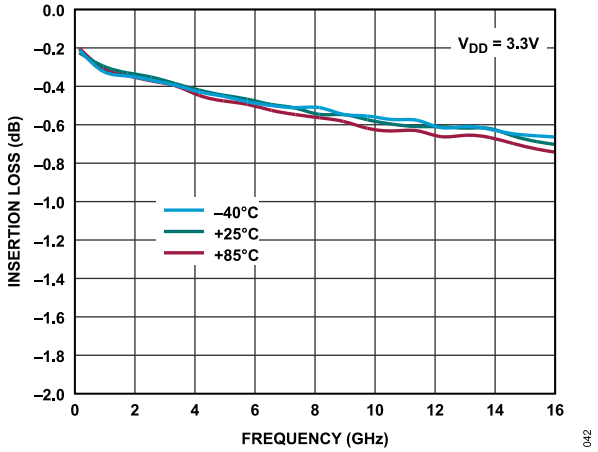

Figure 44. Insertion Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

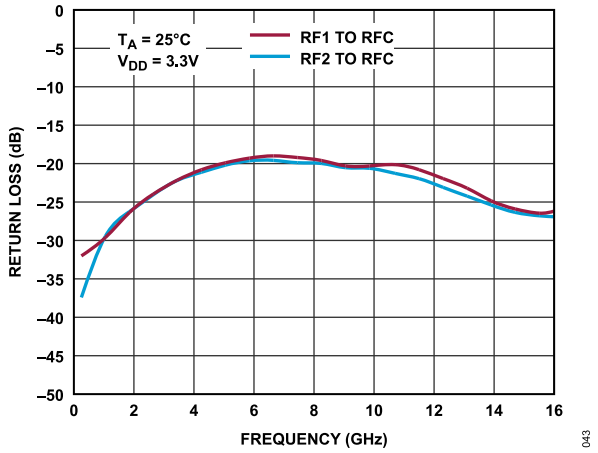

Figure 45. Return Loss vs. Frequency (V_{DD} = 3.3 V)

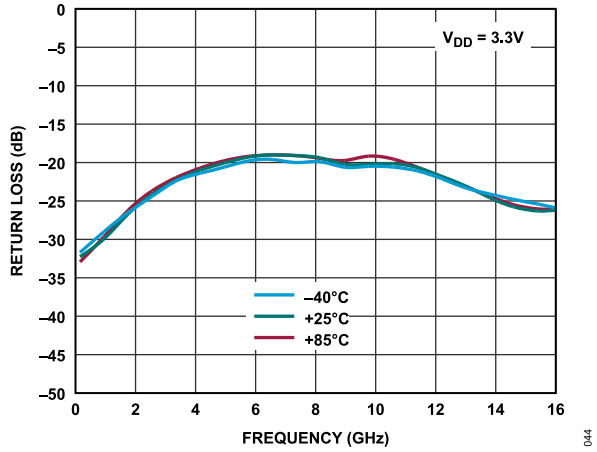

Figure 46. Return Loss vs. Frequency over Temperature (V_{DD} = 3.3 V, RF1 to RFC)

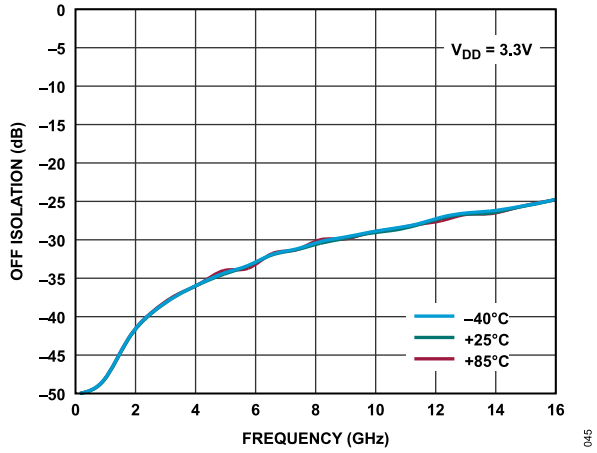

Figure 47. Off Isolation vs. Frequency over Temperature, All Channels Off (V_{DD} = 3.3 V, RF1 to RFC)

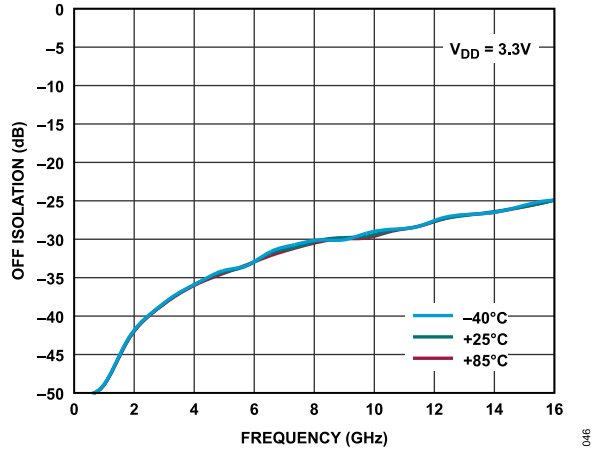

Figure 48. Off Isolation vs. Frequency over Temperature, RF1 to RFC On (V_{DD} = 3.3 V, RF2 to RFC)

TYPICAL PERFORMANCE CHARACTERISTICS

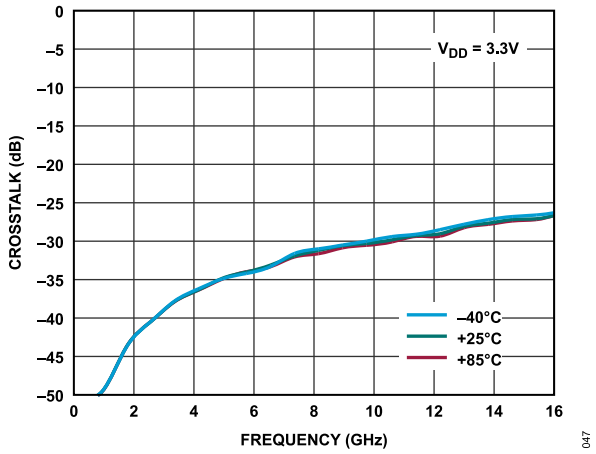

Figure 49. Crosstalk vs. Frequency over Temperature (V_{DD} = 3.3 V, RF2 to RF1)

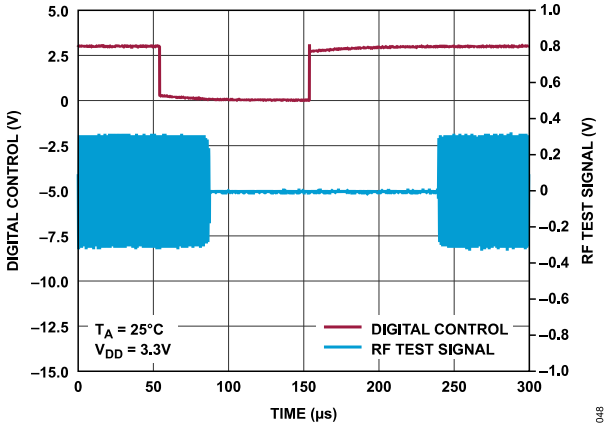

Figure 50. Digital Control and Test Signal vs. Time (V_{DD} = 3.3 V)

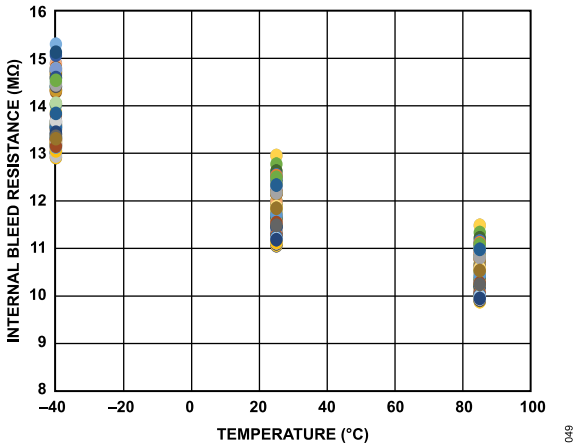

Figure 51. Internal Bleed Resistor Value Distribution over Temperature

THEORY OF OPERATION

SWITCH DESIGN

The ADGM1001 is a wideband SP2T switch fabricated using Analog Devices, Inc., MEMS switch technology. This technology enables high power, low loss, low distortion, wide bandwidth (GHz range) switches to be realized for demanding RF applications.

A key strength of the MEMS switch is that it simultaneously brings together best-in-class, high frequency RF performance and dc precision performance. This combination coupled with superior reliability and a tiny surface mountable form factor make the MEMS switch the ideal switching solution for all RF and precision signal instrumentation needs.

PARALLEL DIGITAL INTERFACE

The ADGM1001 can be controlled via a parallel interface. Standard CMOS/LVTTL signals applied through this interface control the independent actuation and release of all of the switch channels of the ADGM1001.

Setting Pin 6 ($\overline{\text{PIN}}$/SPI) low enables the parallel control interface in two-wire SP2T mode. Pin 1 and Pin 2 (IN1 and IN2) control the switching functions of the ADGM1001. When a Logic 1 is applied to one of these pins, the corresponding switch turns on. Conversely, when a Logic 0 is applied to one of these pins, the corresponding switch turns off. In SP2T mode, it is possible to connect more than one RFx input to RFC at a time. See Table 11 for the truth table.

In parallel control mode, Pin 3 and Pin 4 (AGND/SCLK and AGND/SDO, respectively) must be connected to ground.

When no supply voltage is applied to Pin 23 (V_{DD}), all switches are in an indeterminate state.

Table 11. Truth Table in Parallel Digital Interface Mode (SP2T)

Pin1 (IN1)	Pin 2 (IN2)	RF1 to RFC	RF2 to RFC
0	0	Off	Off
0	1	Off	On
1	0	On	Off
1	1	On	On

SPI DIGITAL INTERFACE

The ADGM1001 can be controlled via an SPI digital interface when Pin 6 ($\overline{\text{PIN}}$/SPI) is high. SPI Mode 0 or Mode 3 can be used with the ADGM1001, and it operates with SCLK frequencies up to 10 MHz. When the SPI is active, addressable mode is the default mode by which the device registers are accessed by a 16-bit SPI command that is bounded by the state of the $\overline{\text{CS}}$ pin. The ADGM1001 can also operate in daisy-chain mode.

The SPI pins of the ADGM1001 are $\overline{\text{CS}}$, SCLK, SDI, and SDO. Hold $\overline{\text{CS}}$ low when using the SPI. The data on the SDI is captured on the rising edge of the SCLK, and data is propagated out on the SDO on the falling edge of the SCLK. The SDO has a push-pull output driver architecture; therefore, it does not require pull-up resistors. The two available SPI operation modes are addressable and daisy-chain.

Addressable Mode

Addressable mode is the default mode for the ADGM1001 upon power-up. A single SPI frame in addressable mode is bounded by a $\overline{\text{CS}}$ falling edge and the succeeding $\overline{\text{CS}}$ rising edge. It is composed of 16 SCLK cycles. The timing diagram for addressable mode is shown in Figure 52 for SPI Mode 0.

The first SDI bit indicates if the SPI command is a read or write command. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command because during these clock cycles SDO propagates out the data contained in the addressed register.

In Mode 0, during any SPI command, SDO sends out eight alignment bits on the $\overline{\text{CS}}$ falling edge and the first seven SCLK falling edges (in Mode 3, the first SCLK falling edge is ignored as shown in Figure 53) The alignment bits observed at the SDO are 0x25.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on the SDO from the 8th to the 15th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

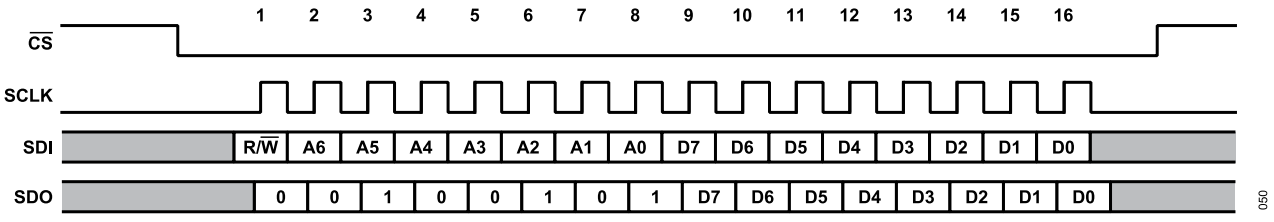

Figure 52. Addressable Mode Timing Diagram (Mode 0)

THEORY OF OPERATION

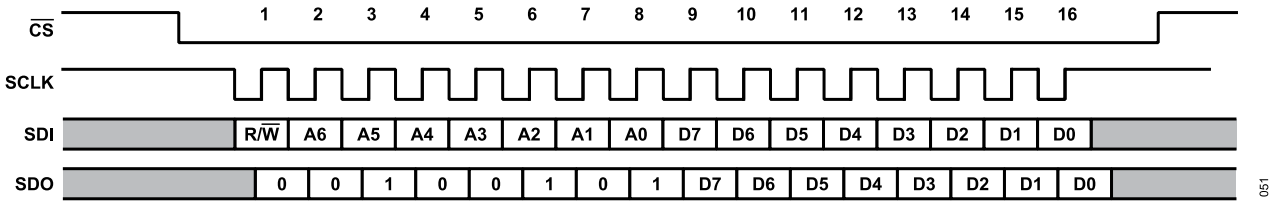

Figure 53. Addressable Mode Timing Diagram (Mode 3)

THEORY OF OPERATION

Daisy-Chain Mode

The connection of several ADGM1001 devices in a daisy-chain configuration is possible. All devices share the same $\overline{CS}$ and SCLK line, while the SDO of a device forms a connection to the SDI of the next device creating a shift register. In daisy-chain mode, the SDO is an 8-cycle delayed version of the SDI.

The ADGM1001 can only enter daisy-chain mode from addressable mode by sending the 16-bit SPI command, 0x2500. See Figure 54 for an example of this. When the ADGM1001 receives this command, the SDO of the devices sends out the same command because the alignment bits at the SDO are 0x25. These alignment bits allow multiple daisy connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 55. When $\overline{CS}$ goes high, Device 1 writes Command 0, Bits[7:0], to its switch data register, Device 2 writes Command 1, Bits[7:0], to its switches, and so on. The SPI block uses the last eight bits it received through the SDI to update the switches. After entering daisy-chain mode, the first eight bits sent out by the SDO are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on the SDI, while data is propagated out of the SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before $\overline{CS}$ goes high. When this is not the case, the SPI sends the last eight bits received to the switch data register.

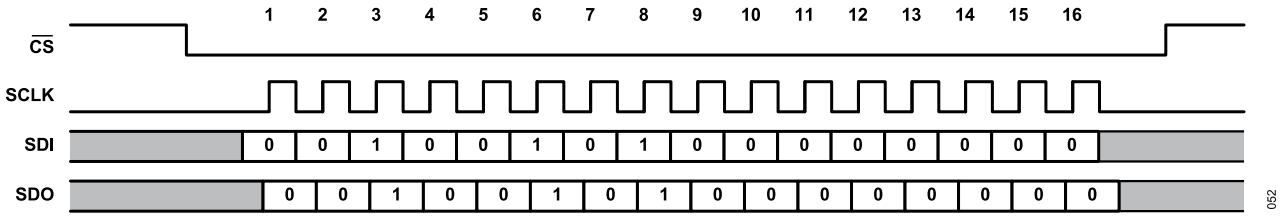

Figure 54. SPI Command to Enter Daisy-Chain Mode

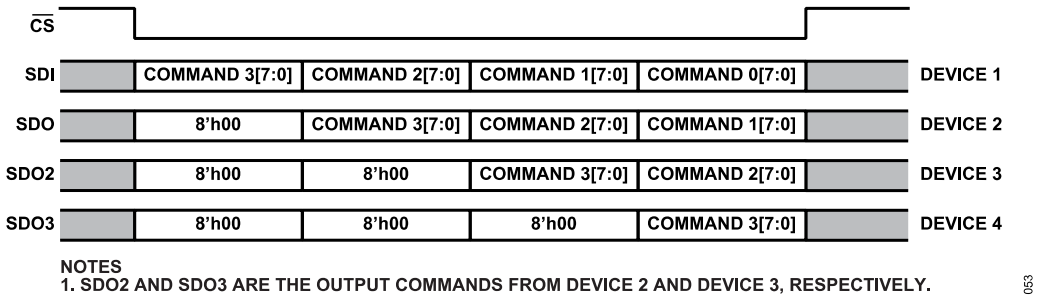

Figure 55. Example of a SPI Frame When Three ADGM1001s Are Connected in Daisy-Chain Mode

THEORY OF OPERATION

Hardware Reset

The digital section of the ADGM1001 goes through an initialization phase during V_{DD} power-up. To hardware reset the device, power cycle the V_{DD} input. After power-up or a hardware reset, ensure that there is a minimum of 10 µs from the power-up or reset time before any SPI command is issued. Ensure that V_{DD} does not drop out during the 10 µs initialization phase because it may result in incorrect operation of the ADGM1001.

Internal Error Status

When an internal error is detected in the ADGM1001, it is flagged in the internal error status bits (INTERNAL_ERROR, Bits[7:6]) of the SWITCH_DATA register. An internal error results from an error in the configuration of the device at power-up.

INTERNAL OSCILLATOR FEEDTHROUGH

The ADGM1001 has an internal oscillator running at a nominal 10 MHz. This oscillator drives the charge pump circuitry that provides the actuation voltage for each of the switch gate electrodes. Although this oscillator is low power, the 10 MHz signal is coupled to the switch and can be considered a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 2 and is typically −123 dBm when one switch is on. V_{DD} level and temperature changes affect the frequency of the noise spur. For the maximum and minimum frequency range over temperature and voltage supply range, see Table 2.

INTERNAL OSCILLATOR FEEDTHROUGH MITIGATION

In normal operation, the 80 V actuation voltage is supplied by the driver IC. Setting the EXTD_EN pin (Pin 7) low enables the built-in 10 MHz oscillator. This setting enables the charge pump circuitry to generate the 80 V required for MEMS switch actuation. The internal oscillator is a source of noise, which couples through to the RF ports. The magnitude of this feedthrough noise spur is specified in Table 2 and is typically −123 dBm when one switch is on. The internal oscillator feedthrough can be eliminated by setting the EXTD_EN pin high, which disables the internal oscillator and charge pump circuitry. When the internal oscillator and charge pump circuitry is disabled, the V_{CP} pin (Pin 24) must be driven with 80 V dc (VCP_{EXT}) from an external voltage supply, as outlined in Table 10, which is required for MEMS switch actuation. The switch can still be controlled via the digital logic interface pins.

LOW POWER MODE

Setting the EXTD_EN pin high shuts down the internal oscillator. The ADGM1001 enters a low power quiescent state, drawing only 50 µA maximum supply current.

TYPICAL OPERATING CIRCUIT

Figure 56 shows the typical operating circuit for the ADGM1001 as used in the EV-ADGM1001SDZ evaluation board. V_{DD} is connected to 3.3 V. No decoupling capacitor is required on the V_{DD} pin (Pin 23). The V_{DD} pin has an internal decoupling capacitor connected to ground in the package. RFGND is separated from AGND internally in the device.

It is recommended to connect RFGND to AGND using one large pad on the PCB to short together EP1 and EP2. EP1 and EP2 are not connected internally. Figure 56 shows the ADGM1001 configured to use the internal oscillator as the reference clock to the driver IC control circuit. Alternatively, set the EXTD_EN pin (Pin 7) high and apply 80 V dc directly to the V_{CP} pin (Pin 24) to disable the internal oscillator and eliminate all oscillator feedthrough. The switches can then be controlled as normal via the logic control interface, IN1 and IN2 (Pin 1 and Pin 2).

THEORY OF OPERATION

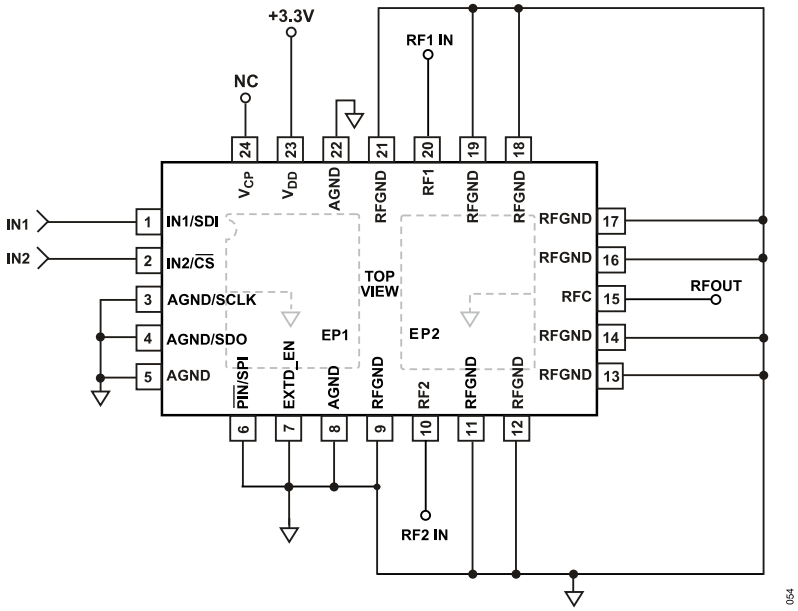

Figure 56. ADGM1001 Typical Operating Circuit in Parallel Digital Interface Mode

APPLICATIONS INFORMATION

POWER SUPPLY RAILS

The ADGM1001 can operate with unipolar supplies between 3.0 V and 3.6 V.

The device is fully specified at a 3.3 V analog supply voltage.

POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a unipolar power solution for the ADGM1001 is shown in Figure 57. The ADP7142 is a low dropout linear regulator that operates from 2.7 V to 40 V and is ideal for regulation of high performance analog and mixed-signal circuits operating from 39 V down to 1.2 V rails. The ADP7142 has 11 µV rms output noise independent of the output voltage. The ADP7142 can be used to power the supply rail for the ADGM1001, a microcontroller, and/or other devices in the signal chain.

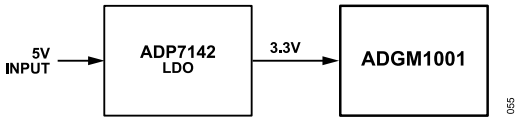

Figure 57. Unipolar Power Solution

If low noise performance at the power supply is required, the ADP7142 can be replaced by the LT1962 or the LT3045-1.

Table 12. Recommended Power Management Devices

Product	Description
ADP7142	40 V, 200 mA, low noise, CMOS LDO linear regulator
LT1962	300 mA, low noise, micropower, LDO regulator
LT3045-1	20 V, 500 mA, ultralow noise, ultrahigh PSRR linear regulator with VIOC control

HIGH SPEED DIGITAL LOOPBACK

Testing high speed input and output (HSIO), such as PICe Gen4 and PICe Gen5 interfaces, in a high volume manufacturing environment is a challenge. A common approach to validate an HSIO interface is the implementation of a high speed loopback test method. This incorporates both high speed and dc test paths in one configuration.

To perform high speed, loop back testing generally a pseudo random bit sequence (PRSB) is transmitted at high speed from the transmitter and received at the receiver end after being looped back on the load board or test board. At the receiver end, the sequence is analyzed to calculate the bit error rate (BER).

DC parametric tests are performed on the input and output pins, such as a continuity test and a leakage test to ensure device functionality. To perform these tests, pins must be connected directly to a dc instrument where the dc measurement of the pin is executed.

The ADGM1001 offers both high speed digital and dc testing capability with superior density in a small 5.00 mm × 4.00 mm × 0.90 mm LGA package as shown in Figure 58. The MEMS switch also enables communication from the tester to the device under test (DUT). The ADGM1001 provides excellent performance from dc to 34 GHz, which allows the switch to handle both high speed signals up to 64 Gbps and precision dc signals.

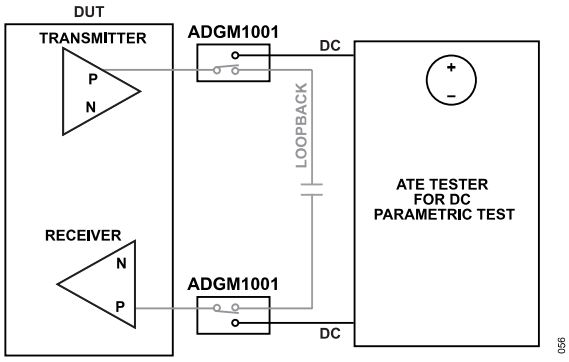

Figure 58. ADGM1001 Enabling Both High Speed Digital and DC Testing (Highlighting P Channel Only)

SWITCHABLE RF ATTENUATOR

It is common to see RF attenuator networks used in RF instrumentation equipment, such as vector network analyzers, spectrum analyzers, and signal generators. Routing RF signals through an attenuator enables the equipment to accept higher power signals and increase the dynamic range of the instrument. In RF attenuation applications, such as vector network analyzers, spectrum analyzers, and signal generators, maintaining the bandwidth of the signal after it passes through the network is critical. Any degradation of the signal reduces the performance of the equipment. Therefore, the RF characteristics of the switches used for routing are integral to the quality of an attenuator network.

The ADGM1001 MEMS switch is suited for use as a switchable RF attenuator due to its low flat insertion loss, wide RF bandwidth, and high reliability. The ADGM1001, as an SPDT switch, also provides added flexibility. Figure 59 shows an example of an attenuation network configuration using two ADGM1001 switches where one switch channel is used for an attenuated route and the other switch channel is used for a non attenuated route.

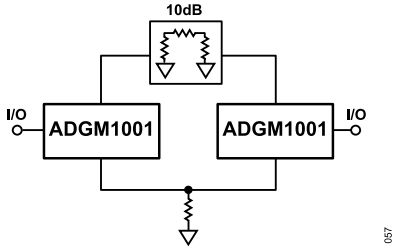

Figure 59. Switching RF Attenuators Using ADGM1001 MEMS Switches

CRITICAL OPERATIONAL REQUIREMENTS

SYSTEM ERROR CONSIDERATIONS DUE TO ON-RESISTANCE DRIFT

The R_{ON} performance of the ADGM1001 is affected by part to part variation, channel to channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

In a 50 Ω system, the on-resistance drift over switch actuations (ΔR_{ON}) can introduce system inaccuracy. Figure 60 shows the ADGM1001 connected with the load in a 50 Ω system, where R_S is the source impedance, and V_S is voltage source. To calculate the system error caused by the ADGM1001 on-resistance drift, use the following equation:

$$System\ Error\ (\%) = \Delta R/R_L$$

where:
ΔR is the ADGM1001 on-resistance drift.
R_L is the load impedance.

The ADGM1001 on-resistance drift also affects insertion loss, which must be considered when using the device. To calculate the on-resistance impact on insertion loss, use the following equation:

$$Insertion\ Loss = 10\log(1 + (\Delta R/R_L))$$

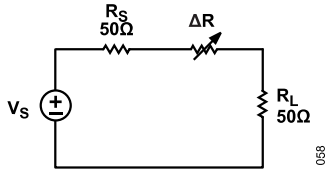

Figure 60. 50 Ω System Representation Where the ADGM1001 Is Connected with the Load

Table 13. System Error and Insertion Loss Error Due to ADGM1001 R_{ON} Drift

On-Resistance Drift	System Error (%)	Insertion Loss Error (dB)
1	2	0.08
3	6	0.25

The on-resistance drift over time specification is −0.46 Ω (maximum) measured after 100 ms, as shown in Figure 9 to Figure 14. According to the plots, the on-resistance drift over time is −0.12 Ω (typical) after 100 ms. The on resistance of the ADGM1001 typically drifts by −0.05 Ω per decade. For example, after 100 ms, the on resistance drifts −0.12 Ω. After 1 sec, the on resistance drifts −0.17 Ω, and after 10 sec, it drifts −0.22 Ω. Therefore, after 1000 sec, the on resistance is expected to drift by −0.32 Ω.

ON-RESISTANCE SHIFT DUE TO TEMPERATURE SHOCK POST ACTUATIONS

When the switch is actuated multiples times at one temperature, and if there is a sudden shift in this temperature, a large shift is shown in the switch R_{ON}. Figure 61 and Figure 62 shows the absolute R_{ON} performance of the population of devices over actuations at different actuation frequencies. During this measurement, the switch is actuated at 85°C and the switch R_{ON} is measured at 25°C. Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for the ADGM1001 R_{ON} drift over actuations.

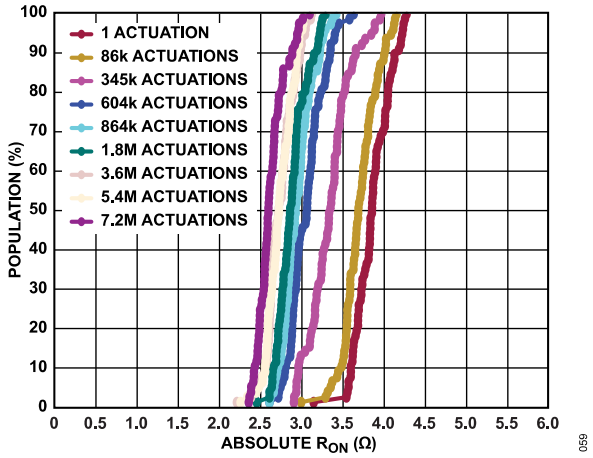

Figure 61. Population vs. Absolute R_{ON}, Switch Actuated at 85°C and R_{ON} Measured at 25°C, Actuation Frequency = 1 Hz, V_{DD} = 3.3 V

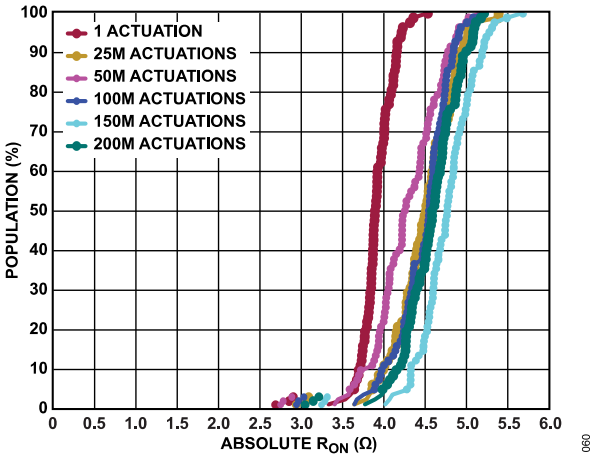

Figure 62. Population vs. Absolute R_{ON}, Switch Actuated at 85°C and R_{ON} Measured at 25°C, Actuation Frequency = 289 Hz, V_{DD} = 3.3 V

HOT SWITCHING

Hot switching occurs by cycling the switch on or off with an excessive voltage or current applied to the switch. The presence of the applied signal during the switching cycle damages the switch contacts. Hot switching damage is dependent on the current or the voltage levels. Hot switching causes a significant reduction in the cycle lifetime of the switch as shown in Figure 66 and Figure 68. Figure 63 shows the hot switching condition when the switch is turned on with 1 V present at the switch terminal during switching. With a voltage across an off switch, damage can occur as the contact or switch closes.

CRITICAL OPERATIONAL REQUIREMENTS

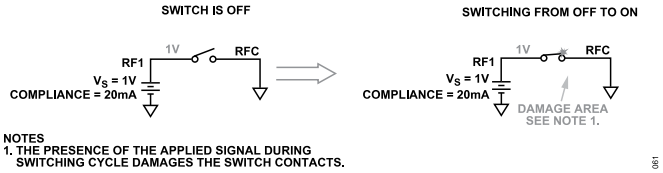

Figure 63. Hot Switching Condition When Turning the Switch from Off to On State

Figure 64 shows the hot switching condition when the switch is turned off with 10 mA passing through the switch during switching. With current passing through an on switch, damage can occur as the contact or switch opens.

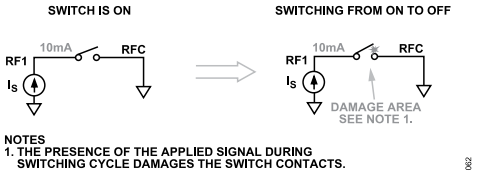

Figure 64. Hot Switching Condition When Turning the Switch from On to Off State

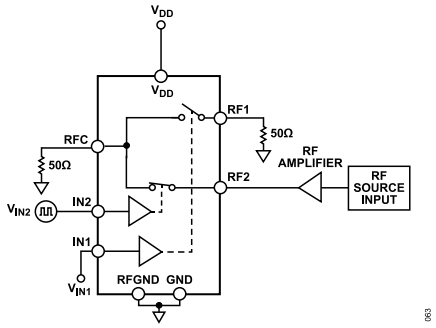

Figure 65. RF Hot Switching Setup

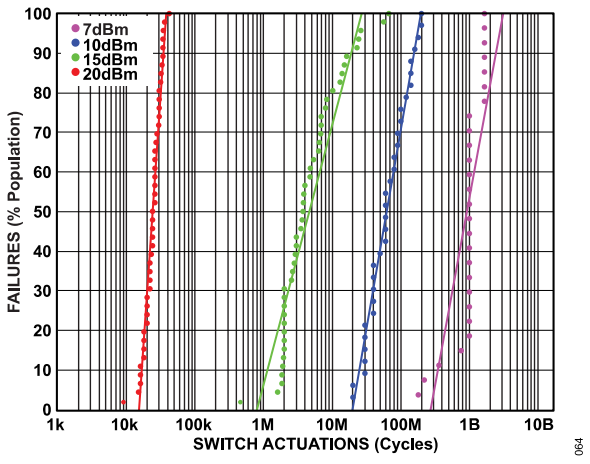

Figure 66. RF Hot Switching Probability Distribution on Log Normal (RF Power = Continuous Wave, Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V)

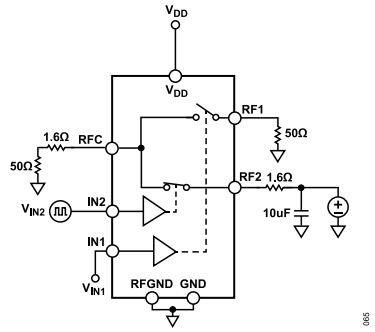

Figure 67. DC Hot Switching Setup

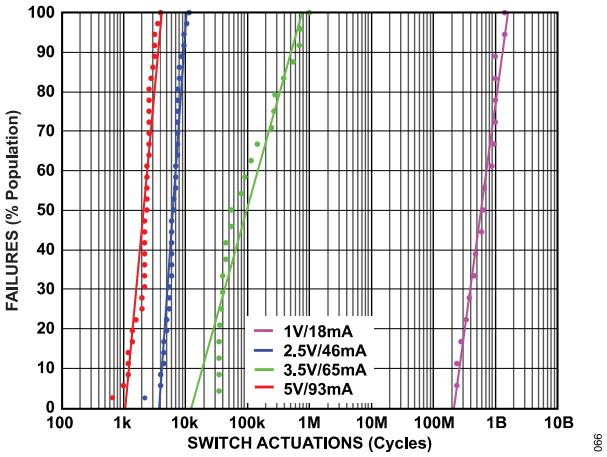

Figure 68. DC Hot Switching Probability Distribution on Log Normal (Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V)

HANDLING PRECAUTIONS

ESD Precautions

All RF pins (RF1, RF2, and RFC) of the ADGM1001 pass the following ESD limits:

- 100 V, Class 0 HBM, ANSI/ESDA/JEDEC JS-001-2010
- 500 V FICDM

All the RFx pins are rated to 500 V FICDM, making the device safe for automated handling and assembly process. Take standard ESD precautions during manufacturing.

The 100 V HBM rating for the RF1, RF2, and RFC pins of the ADGM1001 is susceptible to ESD surge due to human body contact. Add ESD protection if human body contact is expected.

CRITICAL OPERATIONAL REQUIREMENTS

Electrical Overstress (EOS) Precautions

The ADGM1001 is susceptible to EOS. Therefore, observe the following precautions:

- The ADGM1001 is an ESD sensitive device that observes all normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- Avoid running measurement instruments, such as digital multimeters (DMMs), in autorange modes. Some instruments can generate large transient compliance voltages when switching between ranges.
- Use the highest practical DMM range setting (the lowest resolution) for resistance measurements to minimize compliance voltages, particularly during switching.
- Coaxial cables can store charge and lead to EOS when directly connected to the switch. Discharge cables before connecting directly to the switch.
- Avoid connecting capacitive terminations directly to the switch, as shown in Figure 69. A shunt capacitor can store a charge that can potentially lead to hot switching events when the switch opens or closes, affecting the lifetime of the switch.

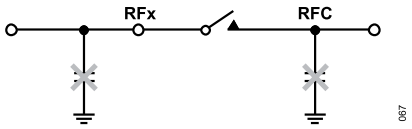

Figure 69. Avoid Large Capacitor Directly Connected to the Switch

Mechanical Shock Precautions

The ADGM1001 passes Group D mechanical shocks tests, as detailed in the Absolute Maximum Ratings. Do not use the device if it is dropped. To reduce excessive mechanical shock and ESD events, avoid handling of loose devices as outlined in Figure 70.

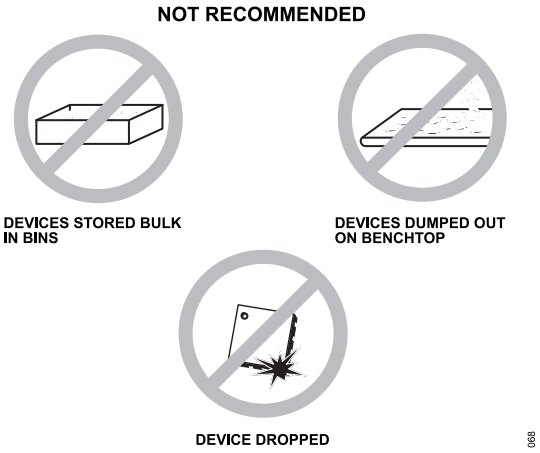

Figure 70. Situations to Avoid During Handling

CRITICAL OPERATIONAL REQUIREMENTS

SOLDER STENCIL RECOMMENDATION

To avoid solder voids under the ADGM1001, it is recommended to use a 0.0767 mm (3 mil) thick solder stencil with nano coating. The aperture size for the solder stencil must be 1:1, and divide the paste mask with multiple pads as shown in Figure 71. Poor soldering may impact the RF performance of the ADGM1001.

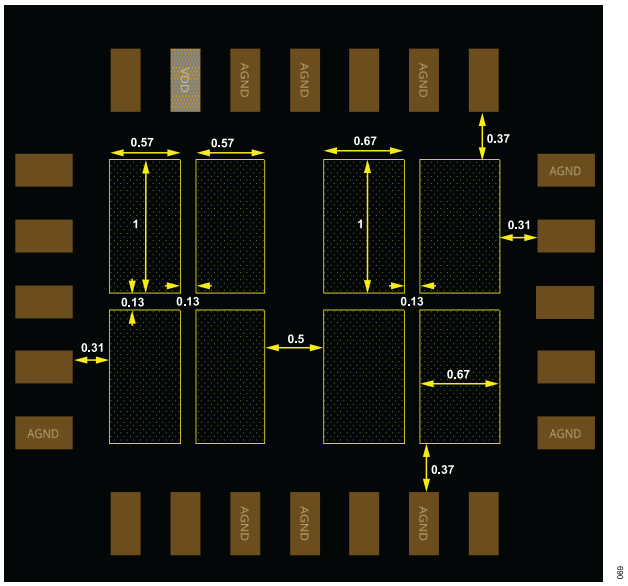

Figure 71. Solder Stencil Recommendation for ADGM1001 (Dimensions Shown in Millimeters)

REGISTER SUMMARY

Table 14. Register Summary

Register (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
0x20	SWITCH_DATA	INTERNAL_ERROR			RESERVED			SW2_EN	SW1_EN	0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x20, Reset: 0x00, Name: SWITCH_DATA

The switch data register controls the status of the two switches of the ADGM1001.

Table 15. Bit Descriptions for SWITCH_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	INTERNAL_ERROR		These bits determine if an internal error has occurred.	0x0	R
		00	No error detected.		
		01	Error detected.		
		10	Error detected.		
		11	Error detected.		
[5:2]	RESERVED		These bits are reserved. Set these bits to 0.	0x0	R
1	SW2_EN		Enable bit for Switch 2.	0x0	R/W
		0	Switch 2 open.		
		1	Switch 2 closed.		
0	SW1_EN		Enable bit for Switch 1.	0x0	R/W
		0	Switch 1 open.		
		1	Switch 1 closed.		

OUTLINE DIMENSIONS

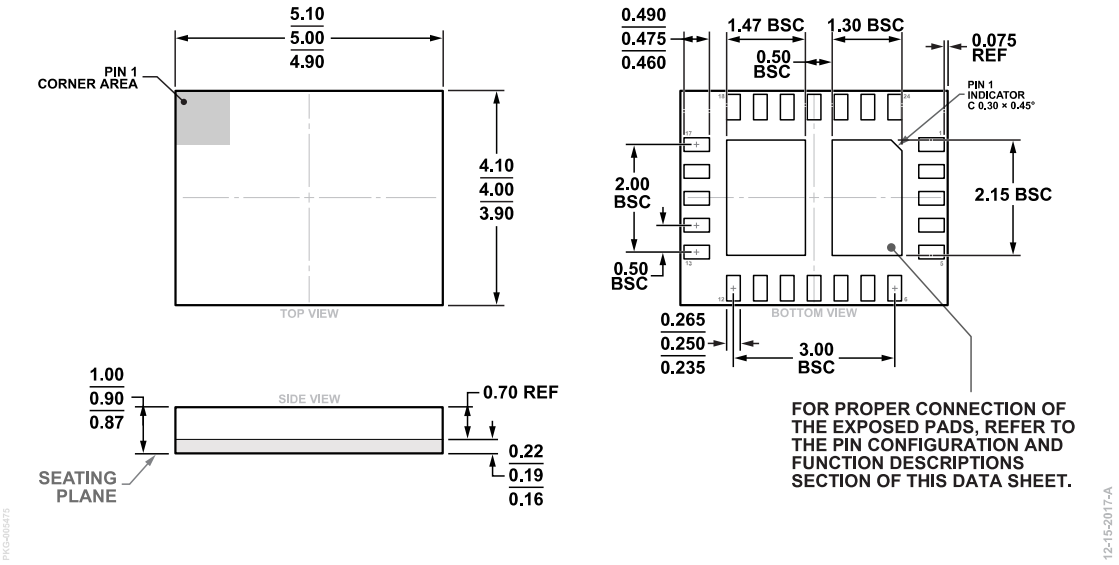

Figure 72. 24-Lead Land Grid Array [LGA]
(CC-24-9)
Dimensions shown in millimeters

Updated: February 26, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADGM1001BCCZ	-40°C to +85°C	LGA/CASON/CH ARRY SO NO LD	Tray, 490	CC-24-9
ADGM1002BCCZ	-40°C to +85°C	LGA/CASON/CH ARRY SO NO LD	Tray, 490	CC-24-9
ADGM1003BCCZ	-40°C to +85°C	LGA/CASON/CH ARRY SO NO LD	Tray, 490	CC-24-9

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADGM1001SDZ	Evaluation Board

[1] Z = RoHS-Complaint Part.