ADIS16350/ADIS16355 ANOMALIES

This anomaly list describes the known bugs, anomalies, and workarounds for the ADIS16350 and ADIS16355.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ANOMALY STATUS

Reference Number	Description	Status
er001	Manual flash/EE memory update failures	Fixed
er002	ALM_SMPL1/ALM_SMPL2 write causes device failure	Fixed
er003	STATUS register not clearing when read	Fixed
er004	Autonull error when calibrating for offset rates >75°/sec	Fixed
er005	Marginal sleep mode initiation	Fixed

DETAILS AND WORKAROUNDS

Manual Flash/EE Memory Update Failures [er001]

Background	The ADIS16350 uses a dual memory structure to maintain its operational configuration. The RAM register structure controls the operation of the device, and the flash/EE memory contents determine what is loaded into the RAM at startup and during reset recovery events. The flash/EE memory is updated by using a control bit in the COMMAND register of this part.
Issue	The flash/EE memory update fails 5% of the time. This issue affects parts that have a date code of 0722 or earlier.
Workaround	For affected parts, read the STATUS register after every flash/EE memory update and verify that Bit 2 (the control register update failed flag) is 0. If it is 1, perform another flash/EE memory update (via Bit 3 of the COMMAND register) and check Bit 2 of the STATUS register again. Repeat this process until the update is verified.
Related Issues	None.

ALM_SMPL1/ALM_SMPL2 Write Causes Device Failure [er002]

Background	The ALM_SMPL1 and ALM_SMPL2 registers provide critical timing configuration data for rate-of-change alarm settings; this data is written to the lower byte of each register. The upper bytes of these registers are documented as being not used.
Issue	Writing to the upper byte of these registers causes a device failure. This issue affects parts that have a date code of 0805 or earlier.
Workaround	For affected parts, do not write to Address 0x25 and Address 0x27. If these addresses are accidentally written to, a power cycle or reset is required to restore normal operation.
Related Issues	None.

STATUS Register Not Clearing When Read [er003]

Background	The STATUS register contains various diagnostic error flags, which clear when read.
Issue	The STATUS register clears when Address 0x3C is read but not when Address 0x3D is read. This issue affects parts that have a date code of 0805 or earlier.
Workaround	For affected parts, use Address 0x3C during a read sequence to clear the flags.
Related Issues	None.

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Autonull Error When Calibrating for Offset Rates >75°/sec [er004]

Background	The autonull command (controlled via the COMMAND register) reads the output registers and loads the user calibration registers with the exact opposite value, which cancels the offset bias.
Issue	When the device is in motion at angular rates >75°/sec and the autonull command is executed, incorrect data is loaded into the calibration registers, causing erroneous data outputs. This issue affects parts that have a date code of 0805 or earlier.
Workaround	Ensure that the autonull command is not in use when the device is in motion at angular rates >75°/sec.
Related Issues	None.

Marginal Sleep Mode Initiation [er005]

Background	The SLP_CNT register provides the option of placing the ADIS16350 into a low power sleep mode.
Issue	The relationship between the actual sleep time and the rising edge of the chip select line is marginal and can cause the device to enter sleep mode while the chip select signal is still low, which automatically brings the part out of sleep mode. In these cases, the part does not go into sleep mode. This issue affects parts that have a date code of 0805 or earlier.
Workaround	If this function is required and the parts do not go into sleep mode, arrange for an exchange.
Related Issues	None.

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