ANALOG DEVICES

Test Procedure EVAL-ADIS-FX3Z

Document No. : 18-059334-01 Rev B
Title : EVAL-ADIS-FX3Z Customer Evaluation Board Test Procedure

REVISION HISTORY				
Revision	**ECR #**	**Description of Change**	**Date**	**Author**
A	ECR-099921	Initial Release	3 Nov 2020	Paul E. Kern

Required Approvers	
Approver Roles	**Approver Names**
Apps Engineer	Paul E. Kern

Equipment List

- Windows PC
- EVAL-ADIS-FX3Z Eval boards to be tested
- USB cable to connect Windows PC to EVAL-ADIS-FX3Z
- FX3 Unit Test Loopback Pod. This board is documented here: https://github.com/juchong/EVAL-ADIS-FX3-Production-Test/tree/master/hardware

Hardware Requirements

In order to operate correctly, this application must be used in conjunction with an EVAL-ADIS-FX3 test mating pod. The mating pod plugs into the two FX3 headers and shorts each pair of digital I/O pins together (including all SPI pins and UART Tx) to enable testing for any shorts/opens. The table at the end of this document shows the pin connections used to enable testing. Additional details and design files are at https://github.com/juchong/EVAL-ADIS-FX3-Production-Test/tree/master/hardware.

Software Setup

Software installation

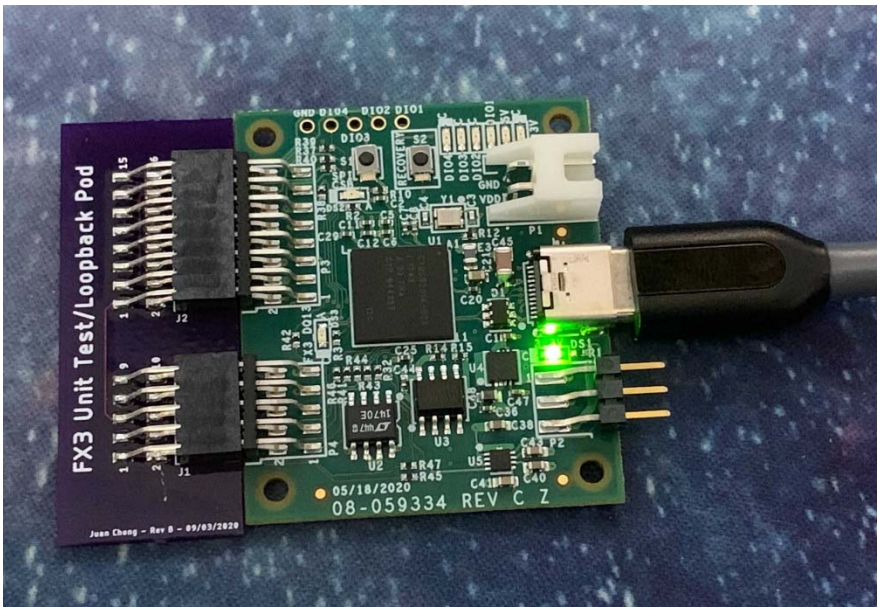
Before testing, Install the following: (This step can be skipped if the software is already installed.)

1. Signed Analog Devices FX3 driver: https://github.com/juchong/iSensor-FX3-API/blob/master/drivers/FX3DriverSetup.exe?raw=true
2. The .EXE test program. Extract this to a folder (or desktop): FX3 Production Test Software (Note that if the above link is broken, click https://github.com/juchong/EVAL-ADIS-FX3-Production-Test/releases to see if a newer version is available.)

After installation, open the folder that the test software was extracted to and double-click on:

EVAL_ADIS-FX3-Prod-Test.exe

Connecting the Hardware



EVAL-ADIS-FX3 Production Test Application

To begin the test, click on the "Start Test" box in the upper left corner of the window.

(Visit: https://github.com/juchong/EVAL-ADIS-FX3-Production-Test/blob/master/images/prod_test_animated.gif to see an animation of the test software running.)

The FX3 Unit Test / Loopback Pin Assignments

Pin 0	Pin 1
DIO1	SPI Clock (SCLK)
DIO2	SPI Chip Select (CS)
DIO3	DIO4
Reset	UART Tx
FX3_GPIO1	FX3_GPIO2
FX3_GPIO3	FX3_GPIO4

The Test Sequence

The test application currently performs the following steps:

1. Initial bootloader loading to NVM (if none is found). This step will detect many potential gross failures in the board including:
    a. Errors in NVM
    b. Errors in USB connection and enumeration
    c. Any errors with the FX3 processor or supply/clock/passive circuitry supplying processor
2. Loading application code onto the I2C EEPROM
3. NVM error log initialization (clears the log)
4. Reboots the board and verifies it correctly re-enumerates using the ADI bootloader (makes sure that bootloader was loaded to NVM correctly)
5. Loads the application code again and checks that no initialization errors have been logged by the application firmware
6. Each GPIO pair is driven high/low repeatedly and verifies the other GPIO reads the correct logic level. This verifies the connection from the FX3 processor to the connector headers for all digital I/O.
7. A 1MHz clock signal is applied to each GPIO pair. The signal frequency and duty cycle are verified using a timer configured for input capture on the other GPIO pin. This test does a better job of catching marginal failures or resistive opens that might not fail at lower frequencies.
8. For each GPIO pair, set one pin logic high and verify all other GPIO can be brought to logic low via a weak pull down resistor. Repeat for opposite polarity. This test will identify any potential shorts between connector pins.