Six Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16486

FEATURES

- Triaxial digital gyroscope, ±450°/sec dynamic range (minimum)
  - ±0.018° axis to axis misalignment error (typical)
  - 5.3°/hr in-run bias stability (typical)
  - 0.25°/√hr angular random walk (typical)
  - 0.01% FS nonlinearity
- Triaxial digital accelerometer, ±18 *g* dynamic range (minimum)
- Triaxial, delta angle, and delta velocity outputs
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C to +85°C
- SPI compatible
- Programmable operation and control
  - Automatic and manual bias correction controls
  - 4 FIR filter banks, 120 configurable taps
  - Digital input and output: data ready alarm indicator, external clock
  - Alarms for condition monitoring
  - Power-down and sleep mode for power management
  - Optional external sync input clock: 2.4 kHz (maximum)
  - Continuous self test of inertial sensors
  - On demand self test of inertial sensors
  - Continuous CRC-based memory testing
- Single VDD power supply operation: 3.0 V to 3.6 V
- 2000 *g* mechanical shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Attitude and heading reference systems
- Platform stabilization and control
- Unmanned vehicle navigation
- Robotics and instrumentation

GENERAL DESCRIPTION

The ADIS16486 is a complete inertial system that includes a triaxis gyroscope and a triaxis accelerometer. Each inertial sensor in the ADIS16486 combines industry leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). Therefore, each sensor has dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16486 provides a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, which reduces system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control. Parylene coating of all internal circuitry provides a protective barrier against moisture exposure.

The ADIS16486 uses the same footprint and connector system as the ADIS16480, ADIS16485, ADIS16487, and ADIS16488A, which greatly simplifies the upgrade process. The ADIS16486 is packaged in a module that is approximately 47 mm × 44 mm × 14 mm with a 24-lead standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

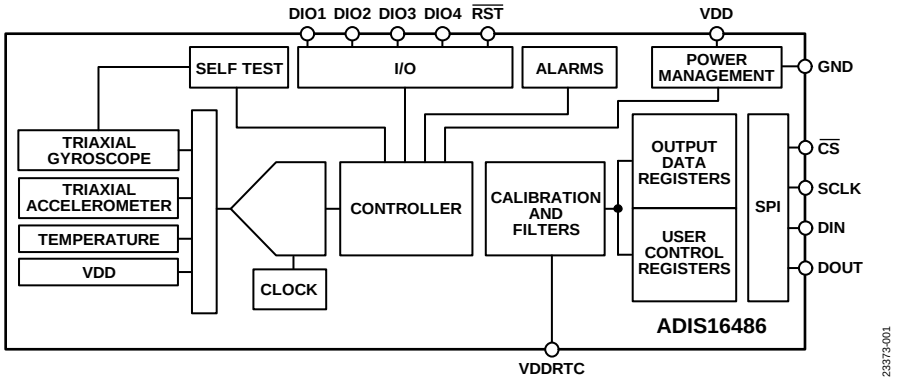

Figure 1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

1/2021—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, and dynamic range = ±450°/sec ± 1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450		±480	°/sec
Sensitivity	32-bit data format (see Table 41)		3.052×10^{-7}		°/sec/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			±1	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±25		ppm/°C
Misalignment Error	Axis to axis		±0.018		Degrees
	Axis to frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, full scale (FS) = 450°/sec		0.01		% FS
Bias					
Repeatability[1, 2]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		°/sec
In-Run Bias Stability	1 σ		5.3		°/hr
Angular Random Walk	1 σ		0.25		°/√hr
Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.0025		°/sec/°C
Error over Temperature	−15°C ≤ T_C ≤ +65°C, 10°C range		±0.0611		°/sec
Linear Acceleration Effect	Any axis, 1 σ (CONFIG, Bit 7 = 1)		0.009		°/sec/*g*
	Any axis, 1 σ (CONFIG, Bit 7 = 0)		0.015		°/sec/*g*
Noise					
Output Noise	No filtering		0.16		°/sec rms
Rate Noise Density	Frequency (f) = 10 Hz to 40 Hz, no filtering		0.0068		°/sec/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			18		kHz
ACCELEROMETERS[3]	Each axis				
Dynamic Range		±18			*g*
Sensitivity	32-bit data format (see Table 55)		1.221×10^{-8}		*g*/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			±0.5	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±25		ppm/°C
Misalignment	Axis to axis		±0.035		Degrees
	Axis to frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, ±10 *g*		10		m*g*
	Best fit straight line, ±18 *g*		90		m*g*
Bias					
Repeatability[1, 2, 4]	−40°C ≤ T_C ≤ +85°C, 1 σ		±16		m*g*
In-Run Bias Stability	1 σ		70		µ*g*
Velocity Random Walk	1 σ		0.029		m/sec/√hr
Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.1		m*g*/°C
Noise					
Output Noise	No filtering		1.29		m*g* rms
Noise Density	f = 10 Hz to 40 Hz, no filtering		0.063		m*g*/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.00565		°C/LSB
LOGIC INPUTS[5]					
Input Voltage					
High (V_{IH})		2.0			V
Low (V_{IL})				0.8	V
$\overline{RST}$ Pulse Width		1			µs
$\overline{CS}$ Wake-Up Pulse Width		20			µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Current					
Logic 1, High (I_{IH})	V_{IH} = 3.3 V			10	μA
Logic 0, Low (I_{IL})	V_{IL} = 0 V				
All Pins Except $\overline{RST}$				10	μA
$\overline{RST}$ Pin			0.33		mA
Input Capacitance (C_{IN})			10		pF
DIGITAL OUTPUTS					
Output Voltage					
High (V_{OH})	Source current (I_{SOURCE}) = 0.5 mA	2.4			V
Low (V_{OL})	Sink current (I_{SINK}) = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[6]	100,000			Cycles
Data Retention[7]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[8]	Time until data is available				
Power-On Start-Up Time				600	ms
Backup			1370	1500	ms
Reset Recovery Time[9]			390	600	ms
Sleep Mode Recovery Time			730	1000	μs
Flash Memory					
Update Time[10]			1.05	6.8	sec
Test Time			50		ms
On Demand Self Test (ODST) Time	Using internal clock (2460 Hz)		12		ms
CONVERSION RATE			2.46		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Sync Input Clock		0.7[11]		2.4	kHz
POWER SUPPLY					
VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[12]	Normal mode, μ + 1 σ		186		mA
	Sleep mode		12.2		mA
	Power-down mode		37		μA
VDDRTC[13]	Operating voltage range	3.0	3.3	3.6	V
Real-Time Clock (RTC) Supply Current	Normal mode, VDDRTC = 3.3 V		13		μA

[1] The repeatability specifications represent analytical projections based on the following drift contributions and conditions: temperature hysteresis (−40°C to +85°C), electronics drift (high temperature operating life test: +110°C, 500 hours), drift from temperature cycling (JESD22, Method A104-C, Method N, 500 cycles, −55°C to +85°C), rate random walk (10-year projection), and broadband noise.
[2] Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability relates to the in-run bias stability and noise density specifications.
[3] All specifications associated with the accelerometers relate to the full-scale range of ±18 *g*.
[4] X-ray exposure can degrade this performance metric.
[5] The digital input and output signals use a 3.3 V system.
[6] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.
[7] The data retention specification assumes a T_J of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.
[8] These times do not include thermal settling and internal filter response times, which may affect overall accuracy.
[9] The $\overline{RST}$ line must be in a low state for at least 10 μs to ensure a proper reset initiation and recovery.
[10] Monitoring the data ready signal (see Table 143 for the FNCTIO_CTRL register configuration) for the return of regular pulsing can help minimize system wait times.
[11] The device functions at clock rates below 0.7 kHz, but at reduced performance levels.
[12] Supply current transients can reach 600 mA during initial startup or reset recovery.
[13] Connecting the VDDRTC supply is a requirement, even if the application does not use the RTC function.

TIMING SPECIFICATIONS

T_C = 25°C and VDD = 3.3 V, unless otherwise noted. See Figure 2 to Figure 4 for the timing diagrams.

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	SCLK frequency	0.01		15	MHz
t_{STALL}[2]	Stall period between data	2			µs
t_{CLS}	SCLK low period	31			ns
t_{CHS}	SCLK high period	31			ns
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	32			ns
t_{DAV}	DOUT valid after SCLK edge			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			ns
t_{DR}, t_{DF}	DOUT rise and fall times, ≤100 pF loading		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to DOUT active	0		11	ns
t_{HD}	SCLK falling edge to DOUT invalid	0			ns
t_{SFS}	Last SCLK rising edge to $\overline{CS}$ deassertion	32			ns
t_{DSHI}	$\overline{CS}$ deassertion to DOUT high impedance	0		9	ns
	Data ready pulse width		11	15	µs
t_1	Input sync pulse width	5			µs
t_2	Input sync to data invalid		560	570	µs
t_3	Input sync period	417			µs

[1] Guaranteed by design and characterization, but not tested in production.
[2] See Table 3 for exceptions to the stall time rating.

Register Write Processing Times

Table 3.

Parameter	Description	Min[1]	Typ	Max	Unit
STALL TIME					
FNCTIO_CTRL, Bits[7:4]	Enabling input sync mode	75			µs
	Disabling input sync mode	147			µs
FNCTIO_CTRL, Bits[3:0]	Configure data ready	3			µs
FILTR_BNK_0	Enable and/or select finite impulse response (FIR) filter banks	101			µs
FILTR_BNK_1	Enable and/or select FIR filter banks	101			µs
NULL_CNFG	Configure autonull bias function	116			µs

[1] Monitor the data ready signal (see Table 143 for the FNCTIO_CTRL register configuration) for the return of regular pulsing to help minimize system wait times.

Timing Diagrams

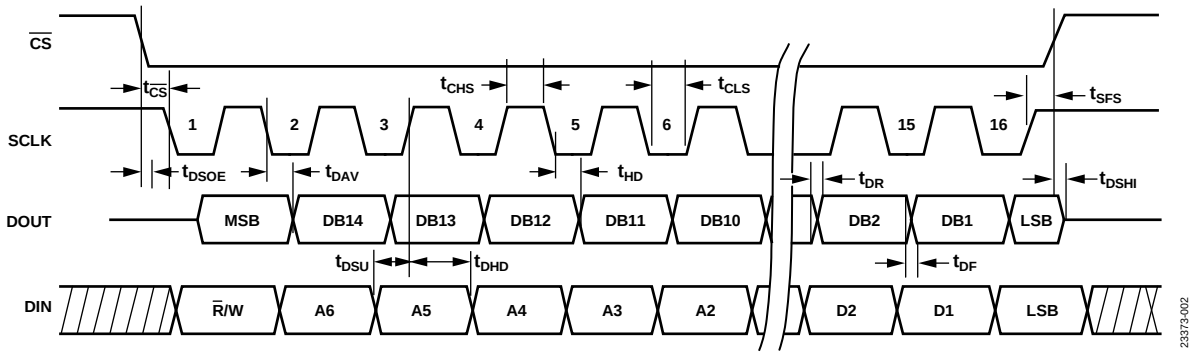


Figure 2. SPI Timing and Sequence

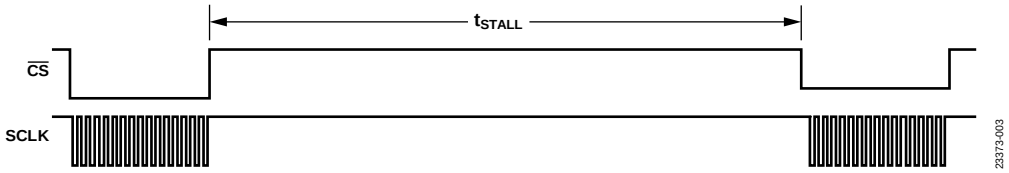


Figure 3. Stall Time and Data Rate

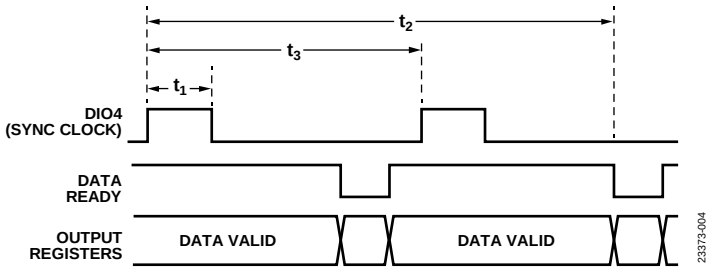


Figure 4. Input Clock Timing Diagram, FNCTIO_CTRL, Bits[7:4] = 0xFD

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Temperature Range	
Calibration	−40°C to +85°C
Operating	−40°C to +105°C
Storage[1]	−65°C to +150°C

[1] Extended exposure to temperatures that are lower than −55°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to the PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
ML-24-6	22.8°C/W	10.1°C/W	48 g

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

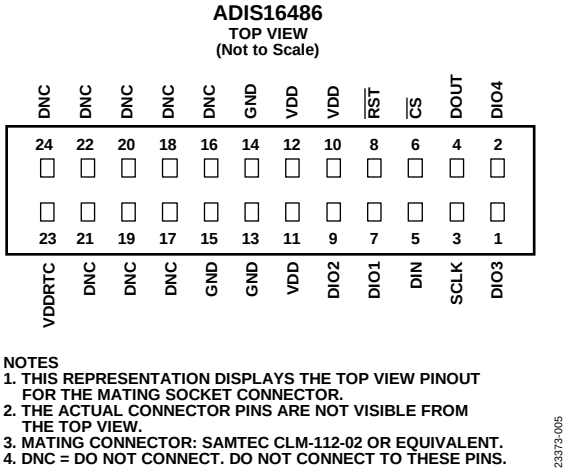


Figure 5. Pin Configuration

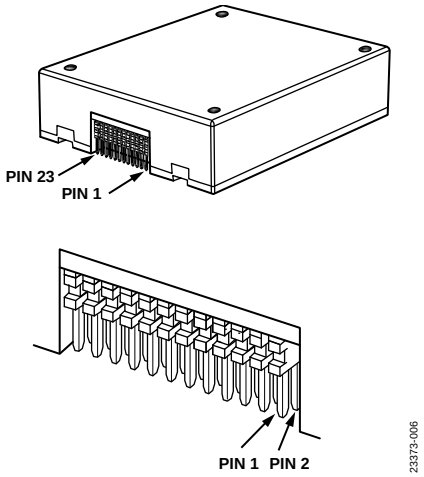


Figure 6. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input and output	Configurable Digital Input and Output 3.
2	DIO4	Input and output	Configurable Digital Input and Output 4.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on the SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DIO1	Input and output	Configurable Digital Input and Output 1.
8	$\overline{RST}$	Input	Reset.
9	DIO2	Input and output	Configurable Digital Input and Output 2.
10, 11, 12	VDD	Supply	Power Supply.
13, 14, 15	GND	Supply	Power Ground.
16 to 22, 24	DNC	Not applicable	Do Not Connect. Do not connect to these pins.
23	VDDRTC	Supply	RTC Power Supply. The VDDRTC power supply must be connected even if the RTC feature is not used.

TYPICAL PERFORMANCE CHARACTERISTICS

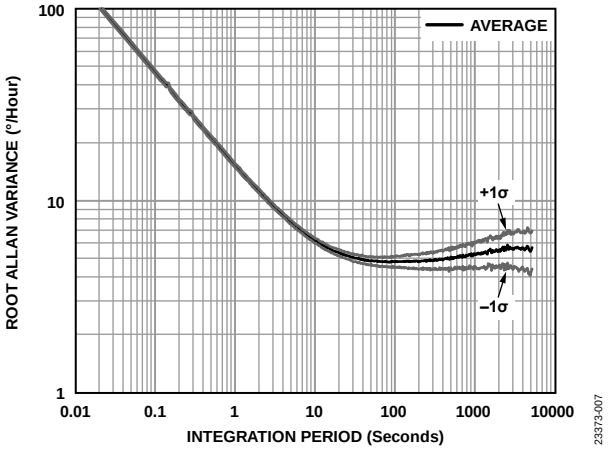


Figure 7. Gyroscope Allan Variance, 25°C

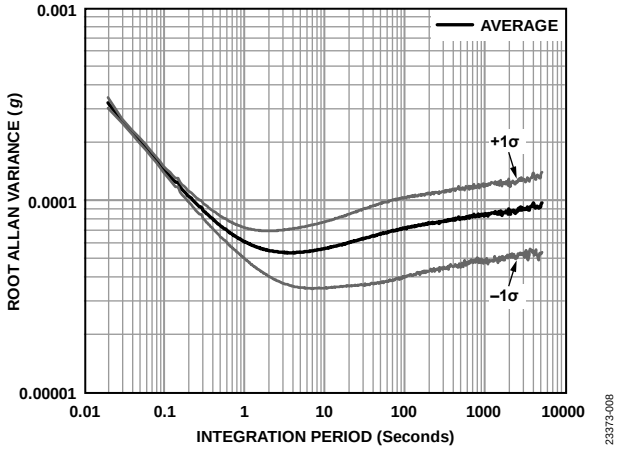


Figure 8. Accelerometer Allan Variance, 25°C

THEORY OF OPERATION

INTRODUCTION

The ADIS16486 is an autonomous sensor system that starts up on its own when it has a valid power supply. After completing its initialization process, the ADIS16486 begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port. The SPI port typically connects to a compatible port on an embedded processor (see Figure 9). See Table 7 for a list of the master processor pin names and functions. The four SPI signals facilitate synchronous serial data communication. The factory default configuration provides users with a data ready signal on the DIO2 pin to trigger consistent data acquisition (see Figure 28).

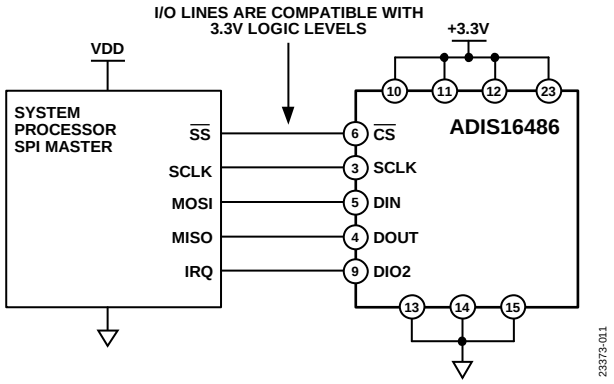


Figure 9. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ	Interrupt request

Table 8 provides a list of settings that describe the SPI protocol of the ADIS16486. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16486 operates as a slave
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register and data length

REGISTER STRUCTURE

The register structure and SPI port support a simple connection between the ADIS16486 and an embedded processor platform. The register structure contains both output data registers and control registers. The output data registers include the latest sensor data, an RTC, error flags, alarm flags, and identification data. The control registers include sample rate, filtering, input and output, alarms, calibration, and diagnostic configuration options. All communication between the ADIS16486 and an external processor involves either reading or writing to one of the user registers.

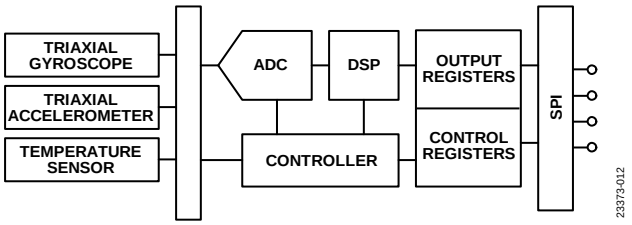


Figure 10. Basic Operation

The register structure uses a paged addressing scheme that contains 13 pages, with each page containing 64 register locations. Each register is 16 bits wide, and each byte has a unique address within the memory map of that page. The SPI port accesses one page at a time using the bit sequence in Figure 11. The user selects the desired page by writing the corresponding page ID to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 9 displays the PAGE_ID register contents for each page along with their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 9. User Accessible Page Register Assignments

Page	PAGE_ID Value	Function
0	0x00	Output data, clock, identification
1	0x01	Reserved
2	0x02	Calibration
3	0x03	Control: sample rate, filtering, input and output, alarms
4	0x04	Serial number
5	0x05	FIR Filter Bank A, Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

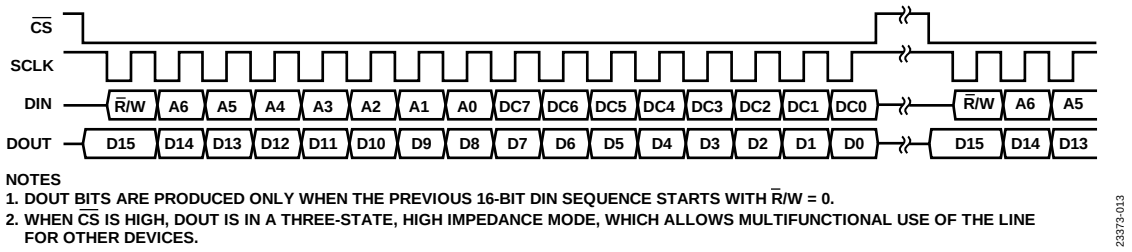


Figure 11. SPI Communication Bit Sequence

SPI COMMUNICATION

Each SPI command and response is 16 bits long and uses the digital coding shown in Figure 11.

DEVICE CONFIGURATION

Each register contains 16 bits (two bytes). Bits[7:0] contain the low byte and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 10). Update the contents of a register by writing to its low byte first and its high byte second. There are three parts to coding an SPI command (see Figure 11) to write a new byte of data to a register: the write bit ($\overline{R}/W = 1$), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 12 provides a coding example for writing 0xFEDC to the XG_BIAS_LOW register (see Table 105), assuming the PAGE_ID register already equals 0x0002.

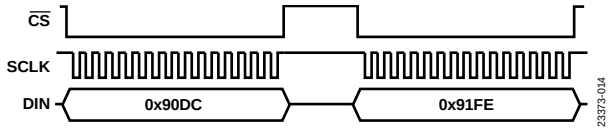


Figure 12. SPI Sequence for Writing 0xFEDC to XG_BIAS_LOW

See Table 11 for a list of the processing times for each register write. The processing time represents the time between the completion of the write command and the time that the command takes full effect on the operation of the ADIS16486.

Dual Memory Structure

The ADIS16486 uses a dual memory structure (see Figure 13) in which the static random access memory (SRAM) supports real-time operation and the flash memory provides nonvolatile storage. During the start-up process, the operating code, calibration coefficients, and user register settings load from the flash memory into the SRAM to support normal operation. The manual flash update command, GLOB_CMD, Bit 3 (see Table 141), provides a simple method for saving user register values to the flash memory. Registers with the flash backup feature are indicated by a yes in the flash backup column of Table 10. This flash backup preserves these settings for automatic recall during the next power-on or reset recovery process. The flash memory has two independent banks that operate in a ping pong manner, alternating with each manual flash update. During startup or reset recovery, the ADIS16486 performs a cyclic redundancy check (CRC) on the boot stream data in the flash memory. If an error is found, the ADIS16486 sets the error flag, SYS_E_FLAG, Bit 1, and restarts the boot process using the backup copy of the boot stream. When in operation, the ADIS16486 continually monitors critical portions of the SRAM using CRC verification and reports the errors in SYS_E_FLAG, Bit 2.

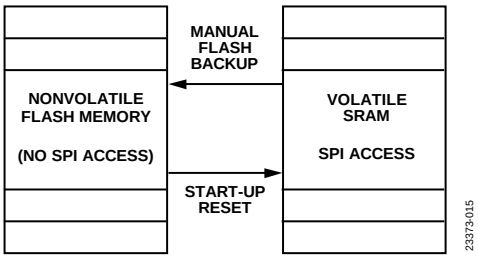


Figure 13. SRAM and Flash Memory Diagram

READING SENSOR DATA

The 16-bit command code (see Figure 11) for a read request on the SPI has three parts: the read bit ($\overline{R}/W = 0$), the address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. A read command produces the contents of the desired register on the DOUT pin during the following 16-bit communication cycle. Figure 14 provides an example that includes two register reads in succession. This example starts with DIN = 0x1A00 to request the contents of the Z_GYRO_OUT register and follows with 0x1800 to request the contents of the Z_GYRO_LOW register (assuming the PROD_ID register already equals 0x0000). Figure 14 shows an example of a full duplex mode of operation in which the ADIS16486 receives a new request while transmitting the data response from the prior request.

Figure 14. SPI Read Example

Figure 15 provides an example of the four SPI signals when reading the PROD_ID register (see Table 91) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI setup and communications because this pattern provides a clear expectation for all signals (the PROD_ID register contents never change).

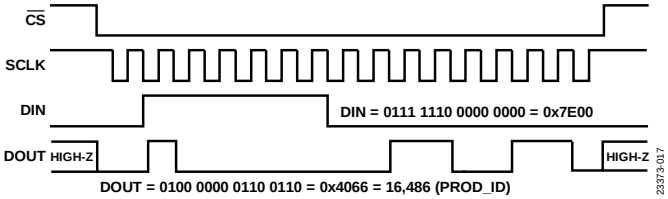


Figure 15. SPI Read Example, Second 16-Bit Sequence

USER REGISTER MEMORY MAP

Table 10. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	Page ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x00	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x00	0x02, 0x03	N/A	Reserved
DATA_CNT	R	No	0x00	0x04, 0x05	N/A	Data and sample counter
SENS_PWR	R	No	0x00	0x06, 0x07	N/A	Internal power supply monitor
SYS_E_FLAG	R	No	0x00	0x08, 0x09	0x0000	Output, status and error flag indicators
DIAG_STS	R	No	0x00	0x0A, 0x0B	0x0000	Output, self test error flags
ALM_STS	R	No	0x00	0x0C, 0x0D	0x0000	Output, alarm error flags
TEMP_OUT	R	No	0x00	0x0E, 0x0F	N/A	Output, internal temperature
X_GYRO_LOW	R	No	0x00	0x10, 0x11	N/A	Output, x-axis gyroscope, low word
X_GYRO_OUT	R	No	0x00	0x12, 0x13	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LOW	R	No	0x00	0x14, 0x15	N/A	Output, y-axis gyroscope, low word
Y_GYRO_OUT	R	No	0x00	0x16, 0x17	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LOW	R	No	0x00	0x18, 0x19	N/A	Output, z-axis gyroscope, low word
Z_GYRO_OUT	R	No	0x00	0x1A, 0x1B	N/A	Output, z-axis gyroscope, high word
X_ACCL_LOW	R	No	0x00	0x1C, 0x1D	N/A	Output, x-axis accelerometer, low word
X_ACCL_OUT	R	No	0x00	0x1E, 0x1F	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LOW	R	No	0x00	0x20, 0x21	N/A	Output, y-axis accelerometer, low word
Y_ACCL_OUT	R	No	0x00	0x22, 0x23	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LOW	R	No	0x00	0x24, 0x25	N/A	Output, z-axis accelerometer, low word
Z_ACCL_OUT	R	No	0x00	0x26, 0x27	N/A	Output, z-axis accelerometer, high word
Reserved	N/A	N/A	0x00	0x28 to 0x3F	N/A	Reserved
X_DELTANG_LOW	R	No	0x00	0x40, 0x41	N/A	Output, x-axis delta angle, low word
X_DELTANG_OUT	R	No	0x00	0x42, 0x43	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LOW	R	No	0x00	0x44, 0x45	N/A	Output, y-axis delta angle, low word
Y_DELTANG_OUT	R	No	0x00	0x46, 0x47	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LOW	R	No	0x00	0x48, 0x49	N/A	Output, z-axis delta angle, low word
Z_DELTANG_OUT	R	No	0x00	0x4A, 0x4B	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LOW	R	No	0x00	0x4C, 0x4D	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_OUT	R	No	0x00	0x4E, 0x4F	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LOW	R	No	0x00	0x50, 0x51	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_OUT	R	No	0x00	0x52, 0x53	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LOW	R	No	0x00	0x54, 0x55	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_OUT	R	No	0x00	0x56, 0x57	N/A	Output, z-axis delta velocity, high word
Reserved	N/A	N/A	0x00	0x58 to 0x77	N/A	Reserved
TIME_MS_OUT	R/W	No	0x00	0x78, 0x79	N/A	RTC: minutes and seconds
TIME_DH_OUT	R/W	No	0x00	0x7A, 0x7B	N/A	RTC: day and hour
TIME_YM_OUT	R/W	No	0x00	0x7C, 0x7D	N/A	RTC: year and month
PROD_ID	R	Yes	0x00	0x7E, 0x7F	0x4066	Output, product identification (16,486)
Reserved	N/A	N/A	0x01	0x00 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x02	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x02	0x02, 0x03	N/A	Reserved
X_GYRO_SCALE	R/W	Yes	0x02	0x04, 0x05	0x0000	Calibration, gyroscope scale, x-axis
Y_GYRO_SCALE	R/W	Yes	0x02	0x06, 0x07	0x0000	Calibration, gyroscope scale, y-axis
Z_GYRO_SCALE	R/W	Yes	0x02	0x08, 0x09	0x0000	Calibration, gyroscope scale, z-axis
X_ACCL_SCALE	R/W	Yes	0x02	0x0A, 0x0B	0x0000	Calibration, accelerometer scale, x-axis
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C, 0x0D	0x0000	Calibration, accelerometer scale, y-axis
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E, 0x0F	0x0000	Calibration, accelerometer scale, z-axis

Name	R/W	Flash Backup	Page ID	Address	Default	Register Description
XG_BIAS_LOW	R/W	Yes	0x02	0x10, 0x11	0x0000	Calibration, offset, gyroscope bias, x-axis, low word
XG_BIAS_HIGH	R/W	Yes	0x02	0x12, 0x13	0x0000	Calibration, offset, gyroscope bias, x-axis, high word
YG_BIAS_LOW	R/W	Yes	0x02	0x14, 0x15	0x0000	Calibration, offset, gyroscope bias, y-axis, low word
YG_BIAS_HIGH	R/W	Yes	0x02	0x16, 0x17	0x0000	Calibration, offset, gyroscope bias, y-axis, high word
ZG_BIAS_LOW	R/W	Yes	0x02	0x18, 0x19	0x0000	Calibration, offset, gyroscope bias, z-axis, low word
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A, 0x1B	0x0000	Calibration, offset, gyroscope bias, z-axis, high word
XA_BIAS_LOW	R/W	Yes	0x02	0x1C, 0x1D	0x0000	Calibration, offset, accelerometer bias, x-axis, low word
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E, 0x1F	0x0000	Calibration, offset, accelerometer bias, x-axis, high word
YA_BIAS_LOW	R/W	Yes	0x02	0x20, 0x21	0x0000	Calibration, offset, accelerometer bias, y-axis, low word
YA_BIAS_HIGH	R/W	Yes	0x02	0x22, 0x23	0x0000	Calibration, offset, accelerometer bias, y-axis, high word
ZA_BIAS_LOW	R/W	Yes	0x02	0x24, 0x25	0x0000	Calibration, offset, accelerometer bias, z-axis, low word
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26, 0x27	0x0000	Calibration, offset, accelerometer bias, z-axis, high word
Reserved	N/A	N/A	0x02	0x28 to 0x73	0x0000	Reserved
USER_SCR_1	R/W	Yes	0x02	0x74, 0x75	0x0000	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x02	0x76, 0x77	0x0000	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x02	0x78, 0x79	0x0000	User Scratch Register 3
USER_SCR_4	R/W	Yes	0x02	0x7A, 0x7B	0x0000	User Scratch Register 4
FLSHCNT_LOW	R/W	Yes	0x02	0x7C, 0x7D	N/A	Diagnostic, flash memory endurance counter, low word
FLSHCNT_HIGH	R/W	Yes	0x02	0x7E, 07F	N/A	Diagnostic, flash memory endurance counter, high word
PAGE_ID	R/W	No	0x03	0x00, 0x01	0x0000	Page identifier
GLOB_CMD	W	No	0x03	0x02, 0x03	0x0000	Control, global commands
Reserved	N/A	N/A	0x03	0x04, 0x05	N/A	Reserved
FNCTIO_CTRL	R/W	Yes	0x03	0x06, 0x07	0x000D	Auxiliary input and output line configuration
GPIO_CTRL	R/W	Yes	0x03	0x08, 0x09	0x00X0[1]	General-purpose input and output control
CONFIG	R/W	Yes	0x03	0x0A, 0x0B	0x00C0	Control, clock, miscellaneous configuration
DEC_RATE	R/W	Yes	0x03	0x0C, 0x0D	0x0000	Control, output, decimation filter
NULL_CNFG	R/W	Yes	0x03	0x0E, 0x0F	0x070A	Control, continuous bias estimation
SLP_CNT	R/W	No	0x03	0x10, 0x11	N/A	Control, power management
Reserved	N/A	N/A	0x03	0x12 to 0x15	N/A	Reserved
FILTR_BNK_0	R/W	Yes	0x03	0x16, 0x17	0x0000	FIR filter control
FILTR_BNK_1	R/W	Yes	0x03	0x18, 0x19	0x0000	FIR filter control
Reserved	N/A	N/A	0x03	0x1A to 0x1F	N/A	Reserved
ALM_CNFG_0	R/W	Yes	0x03	0x20, 0x21	0x0000	Alarm configuration
ALM_CNFG_1	R/W	Yes	0x03	0x22, 0x23	0x0000	Alarm configuration
Reserved	N/A	N/A	0x03	0x24 to 0x27	N/A	Reserved
XG_ALM_MAGN	R/W	Yes	0x03	0x28, 0x29	0x0000	Alarm configuration, x-axis gyroscope alarm
YG_ALM_MAGN	R/W	Yes	0x03	0x2A, 0x2B	0x0000	Alarm configuration, y-axis gyroscope alarm
ZG_ALM_MAGN	R/W	Yes	0x03	0x2C, 0x2D	0x0000	Alarm configuration, z-axis gyroscope alarm
XA_ALM_MAGN	R/W	Yes	0x03	0x2E, 0x2F	0x0000	Alarm configuration, x-axis accelerometer alarm
YA_ALM_MAGN	R/W	Yes	0x03	0x30, 0x31	0x0000	Alarm configuration, y-axis accelerometer alarm
ZA_ALM_MAGN	R/W	Yes	0x03	0x32, 0x33	0x0000	Alarm configuration, z-axis accelerometer alarm
Reserved	N/A	N/A	0x03	0x34 to 0x77	N/A	Reserved
FIRM_REV	R	Yes	0x03	0x78, 0x79	N/A	Firmware revision
FIRM_DM	R	Yes	0x03	0x7A, 0x7B	N/A	Firmware revision day and month
FIRM_Y	R	Yes	0x03	0x7C, 0x7D	N/A	Firmware revision year
BOOT_REV	R	Yes	0x03	0x7E, 0x7F	N/A	Boot revision number
PAGE_ID	R/W	No	0x04	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x04	0x02, 0x03	N/A	Reserved
CAL_SIGTR_LWR	R	Yes	0x04	0x04, 0x05	N/A	Signature CRC, calibration values, low word
CAL_SIGTR_UPR	R	Yes	0x04	0x06, 0x07	N/A	Signature CRC, calibration values, high word
CAL_DRVTN_LWR	R	No	0x04	0x08, 0x09	N/A	Derived CRC, calibration values, low word
CAL_DRVTN_UPR	R	No	0x04	0x0A, 0x0B	N/A	Derived CRC, calibration values, high word
CODE_SIGTR_LWR	R	Yes	0x04	0x0C, 0x0D	N/A	Signature CRC, program code, low word

Name	R/W	Flash Backup	Page ID	Address	Default	Register Description
CODE_SIGTR_UPR	R	Yes	0x04	0x0E, 0x0F	N/A	Signature CRC, program code, high word
CODE_DRVTN_LWR	R	No	0x04	0x10, 0x11	N/A	Derived CRC, program code, low word
CODE_DRVTN_UPR	R	No	0x04	0x12, 0x13	N/A	Derived CRC, program code, high word
Reserved	N/A	N/A	0x04	0x1C to 0x1F	N/A	Reserved
SERIAL_NUM	R	Yes	0x04	0x20, 0x21	N/A	Lot specific serial number
Reserved	N/A	N/A	0x04	0x22 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x05	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x05	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx	R/W	Yes	0x05	0x08 to 0x7F	N/A	FIR Filter Bank A, Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x06	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x06	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx	R/W	Yes	0x06	0x08 to 0x7F	N/A	FIR Filter Bank A, Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x07	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x07	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx	R/W	Yes	0x07	0x02 to 0x7E	N/A	FIR Filter Bank B, Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x08	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x08	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx	R/W	Yes	0x08	0x08 to 0x7F	N/A	FIR Filter Bank B, Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x09	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x09	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx	R/W	Yes	0x09	0x08 to 0x7F	N/A	FIR Filter Bank C, Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0A	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x0A	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx	R/W	Yes	0x0A	0x08 to 0x7F	N/A	FIR Filter Bank C, Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x0B	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x0B	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx	R/W	Yes	0x0B	0x08 to 0x7F	N/A	FIR Filter Bank D, Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0C	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x0C	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx	R/W	Yes	0x0C	0x08 to 0x7F	N/A	FIR Filter Bank D, Coefficient 60 through Coefficient 119

[1] GPIO_CTRL, Bits[7:4] reflect the logic levels on the DIOx pins and do not have a default setting.

Table 11. Processing Times for Register Writes

Registers	Processing Time (µs)
TIME_MS_OUT, TIME_DH_OUT, TIME_YM_OUT	82[1]
X_GYRO_SCALE, Y_GYRO_SCALE, Z_GYRO_SCALE, X_ACCL_SCALE, Y_ACCL_SCALE, Z_ACCL_SCALE	406.5
XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_HIGH	406.5
XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, ZA_BIAS_HIGH	406.5
XG_ALM_MAGN, YG_ALM_MAGN, ZG_ALM_MAGN, XA_ALM_MAGN, YA_ALM_MAGN, ZA_ALM_MAGN	406.5
USER_SCR_1, USER_SCR_2, USER_SCR_3, USER_SCR_4	0
GLOB_CMD	82[2]
GPIO_CTRL, DEC_RATE, CONFIG, ALM_CNFG_0, ALM_CNFG_1, SLP_CNT	82
FNCTIO_CTRL	147
NULL_CNFG	116
FILTR_BNK_0, FILTR_BNK_1	101
FIR_COEF_xxxx	0[3]

[1] The processing time for the TIME_xx_xxxx registers does not include the time it takes for these values to synchronize (≤1 sec).
[2] The processing time for the GLOB_CMD register does not include the time it takes to execute each command in this register.
[3] The processing time for the FIR_COEF_xxxx registers does not include the time it takes for the FIR filters to settle.

USER REGISTER DEFINITIONS

Page Number (PAGE_ID)

The contents in the PAGE_ID register (see Table 12 and Table 13) contain the current page setting and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

Table 12. PAGE_ID Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x00, 0x01	0x0000	R/W	No

Table 13. PAGE_ID Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Page number, binary numerical format

Data and Sample Counter (DATA_CNT)

The DATA_CNT register (see Table 14 and Table 15) is a continuous, real-time, sample counter. The counter starts at 0x0000, increments every time that the sensor output data registers update, and wraps around from 0xFFFF to 0x0000.

Table 14. DATA_CNT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x04, 0x05	Not applicable	R	No

Table 15. DATA_CNT Bit Definition

Bits	Description (No Default)
[15:0]	Data counter, binary format

Internal Power Supply Monitor (SENS_PWR)

The SENS_PWR register (see Table 16 and Table 17) is a read only register that provides a measurement of the internal power supply. Table 18 provides some examples of the data format.

Table 16. SENS_PWR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x06, 0x07	Not applicable	R	No

Table 17. SENS_PWR Bit Definition

Bits	Description (No Default)
[15:0]	Relative power supply measurement, twos complement (see Equation 1)

$$SENS\_PWR_{LSB} = \left(\frac{2.5\ \text{V}}{Supply} \times 2^{16} \right) - 2^{15} \quad (1)$$

Table 18. SENS_PWR Data Format Examples

Supply Level (V)	Decimal	Hex	Binary
4.90	+669	0x029D	0000 0010 1001 1101
4.95	+331	0x014B	0000 0001 0100 1011
5	0	0x0000	0000 0000 0000 0000
5.05	−324	0xFEBC	1111 1110 1011 1100
5.10	−643	0xFD7D	1111 1101 0111 1101

Status and Error Flag Indicators (SYS_E_FLAG)

The SYS_E_FLAG register (see Table 19 and Table 20) provides various error flags. Reading this register causes its bits to return to 0, except for Bit 7. If an error condition persists, the flag (bit) automatically returns an alarm value of 1.

Table 19. SYS_E_FLAG Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x08, 0x09	0x0000	R	No

Table 20. SYS_E_FLAG Bit Definitions

Bits	Description (Default = 0x0000)
15	Watch dog timer flag. A 1 indicates that the ADIS16486 automatically resets itself to clear an issue.
[14:9]	Not used.
8	Internal power supply monitor. A 1 indicates an issue with the power supply for the sensors. Initiate a reset to recover. Replace the ADIS16486 if this error persists.
7	Processing overrun. A 1 indicates the occurrence of a processing overrun. Initiate a reset to recover. Replace the ADIS16486 if this error persists. One potential source of this error is not providing power to the VDDRTC pin.
6	Flash memory update failure. A 1 indicates that the most recent flash memory update (GLOB_CMD, Bit 3, see Table 141) failed. Repeat the test and replace the ADIS16486 if this error persists.
5	Sensor failure. A 1 indicates the failure of at least one of the self test processes: continuous or on demand. Run the ODST (GLOB_CMD, Bit 1, see Table 141) when the unit is in not in motion. Replace the ADIS16486 if the error persists.
4	Overrange. A 1 indicates that the digital magnitude of at least one sensor has reached 99% of its maximum value. Initiate a reset to recover and replace the ADIS16486 if this error persists.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. Repeat the previous communication sequence to recover. Persistence in this error can indicate a weakness in the SPI service from the master processor.
2	SRAM error condition. A 1 indicates a failure in the CRC (period = 20 ms) between the SRAM and flash memory. Initiate a reset to recover. Replace the ADIS16486 if this error persists.
1	Boot memory failure. A 1 indicates that the CRC on the primary flash memory bank did not match the reference CRC value, and that the device automatically rebooted using the backup memory bank in flash. Replace the ADIS16486 if this error persists.
0	Alarm status flag. A 1 indicates that one of the user-programmable alarms is active. See the ALM_STS register for an indication of which alarm is active.

Self Test Error Flags (DIAG_STS)

SYS_E_FLAG, Bit 5 (see Table 20) contains the pass and fail result (0 = pass) for both CST and ODST operations, whereas the DIAG_STS register (see Table 21 and Table 22) contains pass and fail flags (0 = pass) for each inertial sensor. Reading the DIAG_STS register clears all bits to 0. The bits in the DIAG_STS register return to 1 if the error conditions persist. The CST leverages a proprietary method for detecting abnormal behavior during normal operation, whereas the ODST artificially forces each inertial sensor to simulate their response to actual motion.

Table 21. DIAG_STS Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x0A, 0x0B	0x0000	R	No

Table 22. DIAG_STS Bit Definitions

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	ODST failure, z-axis accelerometer (1 = failure)
4	ODST failure, y-axis accelerometer (1 = failure)
3	ODST failure, x-axis accelerometer (1 = failure)
2	ODST failure, z-axis gyroscope (1 = failure)
1	ODST failure, y-axis gyroscope (1 = failure)
0	ODST failure, x-axis gyroscope (1 = failure) or continuous self test (CST) failure, all gyroscope and accelerometers (1 = failure)

Alarm Error Flags (ALM_STS)

The ALM_STS register (see Table 23 and Table 24) contains the error flags for the alarm settings in the ALM_CNFG_0 (see Table 159) and ALM_CNFG_1 (see Table 161) registers. Reading the ALM_STS register clears all bits to 0. If the alarm condition is persistent, the corresponding bit returns to 1 in the next sample cycle.

Table 23. ALM_STS Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x0C, 0x0D	0x0000	R	No

Table 24. ALM_STS Bit Definitions

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	Z-axis accelerometer alarm flag (1 = alarm is active)
4	Y-axis accelerometer alarm flag (1 = alarm is active)
3	X-axis accelerometer alarm flag (1 = alarm is active)
2	Z-axis gyroscope alarm flag (1 = alarm is active)
1	Y-axis gyroscope alarm flag (1 = alarm is active)
0	X-axis gyroscope alarm flag (1 = alarm is active)

Internal Temperature (TEMP_OUT)

The TEMP_OUT register (see Table 25 and Table 26) provides a coarse measurement of the temperature inside of the ADIS16486. This data is most useful for monitoring relative changes in the thermal environment.

Table 25. TEMP_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x0E, 0x0F	Not applicable	R	No

Table 26. TEMP_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Temperature data, twos complement, 0.00565°C per LSB, 25°C = 0x0000

Table 27. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+85	+10,619	0x297B	0010 1001 0111 1011
+25 + 0.0113	+2	0x0002	0000 0000 0000 0010
+25 + 0.00565	+1	0x0001	0000 0000 0000 0001
+25	0	0x0000	0000 0000 0000 0000
+25 − 0.00565	−1	0xFFFF	1111 1111 1111 1111
+25 − 0.0113	−2	0xFFFE	1111 1111 1111 1110
−40	−11,504	0xD310	1101 0011 0001 0000

GYROSCOPE DATA

The gyroscopes in the ADIS16486 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 16 shows the orientation of each gyroscope axis, as well as the direction of rotation that produces a positive response in each of their measurements.

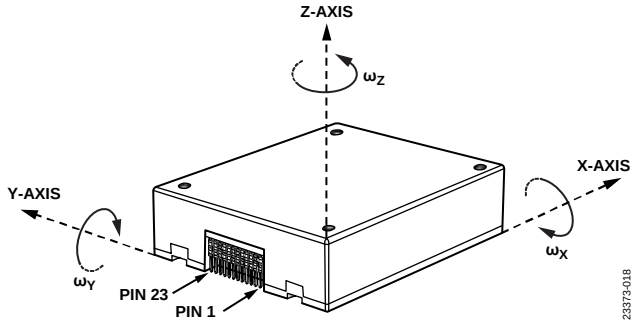


Figure 16. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 17 shows how the X_GYRO_LOW and X_GYRO_OUT registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y- and x-axes.

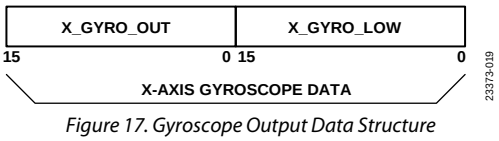


Figure 17. Gyroscope Output Data Structure

X-Axis Gyroscope (X_GYRO_LOW, X_GYRO_OUT)

The X_GYRO_LOW (see Table 28 and Table 29) and X_GYRO_OUT (see Table 30 and Table 31) registers contain the gyroscope data for the x-axis.

Table 28. X_GYRO_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x10, 0x11	Not applicable	R	No

Table 29. X_GYRO_LOW Bit Definition

Bits	Description (No Default)
[15:0]	X-axis gyroscope data, low word

Table 30. X_GYRO_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x12, 0x13	Not applicable	R	No

Table 31. X_GYRO_OUT Bit Definition

Bits	Description (No Default)
[15:0]	X-axis gyroscope data, high word, twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Y-Axis Gyroscope (Y_GYRO_LOW, Y_GYRO_OUT)

The Y_GYRO_LOW (see Table 32 and Table 33) and Y_GYRO_OUT (see Table 34 and Table 35) registers contain the gyroscope data for the y-axis.

Table 32. Y_GYRO_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x14, 0x15	Not applicable	R	No

Table 33. Y_GYRO_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis gyroscope data, low word

Table 34. Y_GYRO_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x16, 0x17	Not applicable	R	No

Table 35. Y_GYRO_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis gyroscope data, high word, twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Z-Axis Gyroscope (Z_GYRO_LOW, Z_GYRO_OUT)

The Z_GYRO_LOW (see Table 36 and Table 37) and Z_GYRO_OUT (see Table 38 and Table 39) registers contain the gyroscope data for the z-axis.

Table 36. Z_GYRO_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x18, 0x19	Not applicable	R	No

Table 37. Z_GYRO_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis gyroscope data, low word, additional resolution bits

Table 38. Z_GYRO_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x1A, 0x1B	Not applicable	R	No

Table 39. Z_GYRO_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis gyroscope data, high word, twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Gyroscope Resolution

Table 40 and Table 41 offer various numerical examples that demonstrate the format of the angular rate (gyroscopes) data in both 16-bit and 32-bit formats.

Table 40. 16-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex	Binary
+450	+22,500	0x57E4	0101 0111 1110 0100
+0.04	+2	0x0002	0000 0000 0000 0010
+0.02	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.02	−1	0xFFFF	1111 1111 1111 1111
−0.04	−2	0xFFFE	1111 1111 1111 1110
−450	−22,500	0xA81C	1010 1000 0001 1100

Table 41. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex
+450	+1,474,560,000	0x57E40000
$+0.02/2^{15}$	+2	0x00000002
$+0.02/2^{16}$	+1	0x00000001
0	0	0x00000000
$-0.02/2^{16}$	−1	0xFFFFFFFF
$-0.02/2^{15}$	−2	0xFFFFFFFE
−450	−1,474,560,000	0x73600000

ACCELERATION DATA

The accelerometers in the ADIS16486 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 18 shows the orientation of each accelerometer axis, along with the direction of acceleration that produces a positive response in each of their measurements.

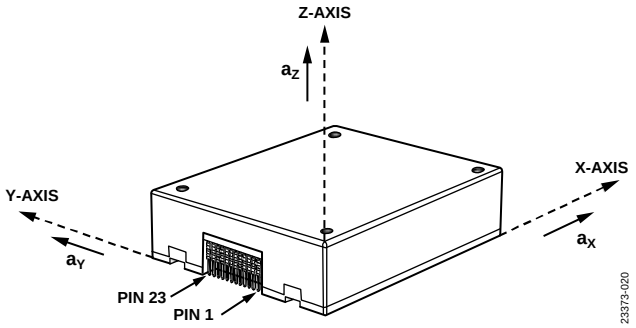


Figure 18. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 19 shows how the X_ACCL_LOW and X_ACCL_OUT registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and x-axes.

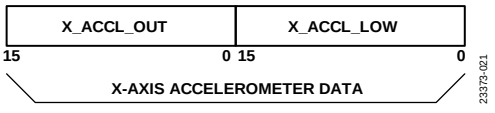


Figure 19. Accelerometer Output Data Structure

X-Axis Accelerometer (X_ACCL_LOW, X_ACCL_OUT)

The X_ACCL_LOW (see Table 42 and Table 43) and X_ACCL_OUT (see Table 44 and Table 45) registers contain the accelerometer data for the x-axis.

Table 42. X_ACCL_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x1C, 0x1D	Not applicable	R	No

Table 43. X_ACCL_LOW Bit Definition

Bits	Description (No Default)
[15:0]	X-axis accelerometer data, low word

Table 44. X_ACCL_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x1E, 0x1F	Not applicable	R	No

Table 45. X_ACCL_OUT Bit Definition

Bits	Description (No Default)
[15:0]	X-axis accelerometer data, high word, twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Y-Axis Accelerometer (Y_ACCL_LOW, Y_ACCL_OUT)

The Y_ACCL_LOW (see Table 46 and Table 47) and Y_ACCL_OUT (see Table 48 and Table 49) registers contain the accelerometer data for the y-axis.

Table 46. Y_ACCL_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x20, 0x21	Not applicable	R	No

Table 47. Y_ACCL_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis accelerometer data, low word

Table 48. Y_ACCL_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x22, 0x23	Not applicable	R	No

Table 49. Y_ACCL_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis accelerometer data, twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Z-Axis Accelerometer (Z_ACCL_LOW, Z_ACCL_OUT)

The Z_ACCL_LOW (see Table 50 and Table 51) and Z_ACCL_OUT (see Table 52 and Table 53) registers contain the accelerometer data for the z-axis.

Table 50. Z_ACCL_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x24, 0x25	Not applicable	R	No

Table 51. Z_ACCL_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis accelerometer data, low word

Table 52. Z_ACCL_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x26, 0x27	Not applicable	R	No

Table 53. Z_ACCL_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis accelerometer data, high word, twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Accelerometer Resolution

Table 54 and Table 55 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 54. 16-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex	Binary
+18 *g*	+20,000	0x4E20	0100 1110 0010 0000
+1.6 m*g*	+2	0x0002	0000 0000 0000 0010
+0.8 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−0.8 m*g*	−1	0xFFFF	1111 1111 1111 1111
−1.6 m*g*	−2	0xFFFE	1111 1111 1111 1110
−18 *g*	−20,000	0xB1E0	1011 0001 1110 0000

Table 55. 32-Bit Accelerometer Data Format Examples

Acceleration (*g*)	Decimal	Hex
+18	+1,310,720,000	0x4E200000
$+0.0008/2^{15}$	+2	0x00000002
$+0.0008/2^{16}$	+1	0x00000001
0	0	0x00000000
$-0.0008/2^{16}$	−1	0xFFFFFFFF
$-0.0008/2^{15}$	−2	0xFFFFFFFE
−18	−1,310,720,000	0xB1E00000

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16486 provides delta angle measurements that represent a computation of angular displacement between each sample update.

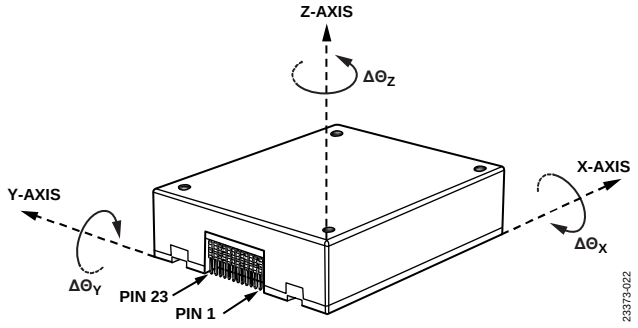


Figure 20. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (the x-axis is shown as follows):

$$\Delta\theta_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(\omega_{x,nD+d} + \omega_{x,nD+d-1} \right)$$

where:
D is the decimation rate = DEC_RATE + 1 (see Table 149).
fs is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. Ensure that the external clock frequency is at least 700 Hz to prevent overflow in the delta angle data registers at high rotation rates.

Each axis of the delta angle measurements has two output data registers. Figure 21 shows how the X_DELTANG_LOW and X_DELTANG_OUT registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and x-axes.

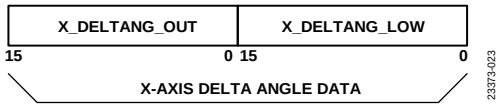


Figure 21. Delta Angle Output Data Structure

X-Axis Delta Angle (X_DELTANG_LOW, X_DELTANG_OUT)

The X_DELTANG_LOW (see Table 56 and Table 57) and X_DELTANG_OUT (see Table 58 and Table 59) registers contain the delta angle data for the x-axis.

Table 56. X_DELTANG_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x40, 0x41	Not applicable	R	No

Table 57. X_DELTANG_LOW Bit Definition

Bits	Description (No Default)
[15:0]	X-axis delta angle data, low word

Table 58. X_DELTANG_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x42, 0x43	Not applicable	R	No

Table 59. X_DELTANG_OUT Bit Definition

Bits	Description (No Default)
[15:0]	X-axis delta angle data, twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Y-Axis Delta Angle (Y_DELTANG_LOW, Y_DELTANG_OUT)

The Y_DELTANG_LOW (see Table 60 and Table 61) and Y_DELTANG_OUT (see Table 62 and Table 63) registers contain the delta angle data for the y-axis.

Table 60. Y_DELTANG_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x44, 0x45	Not applicable	R	No

Table 61. Y_DELTANG_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis delta angle data, low word

Table 62. Y_DELTANG_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x46, 0x47	Not applicable	R	No

Table 63. Y_DELTANG_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis delta angle data, twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Z-Axis Delta Angle (Z_DELTANG_LOW, Z_DELTANG_OUT)

The Z_DELTANG_LOW (see Table 64 and Table 65) and Z_DELTANG_OUT (see Table 66 and Table 67) registers contain the delta angle data for the z-axis.

Table 64. Z_DELTANG_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x48, 0x49	Not applicable	R	No

Table 65. Z_DELTANG_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis delta angle data, low word

Table 66. Z_DELTANG_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x4A, 0x4B	Not applicable	R	No

Table 67. Z_DELTANG_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis delta angle data, twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Delta Angle Resolution

Table 68 and Table 69 offer various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 68. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex	Binary
+720 × (2^{15} − 1)/2^{15}	+32,767	0x7FFF	0111 1111 1110 1111
+720/2^{14}	+2	0x0002	0000 0000 0000 0010
+720/2^{15}	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−720/2^{15}	−1	0xFFFF	1111 1111 1111 1111
−720/2^{14}	−2	0xFFFE	1111 1111 1111 1110
−720	−32,768	0x8000	1000 0000 0000 0000

Table 69. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex
$+720 \times (2^{23} - 1)/2^{23}$	+2,147,483,647	0x7FFFFFFF
$+720/2^{22}$	+2	0x00000002
$+720/2^{23}$	+1	0x00000001
0	0	0x00000000
$-720/2^{23}$	−1	0xFFFFFFFF
$-720/2^{23}$	−2	0xFFFFFFFE
−720	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16486 provides delta velocity measurements that represent a computation of linear velocity change between each sample update.

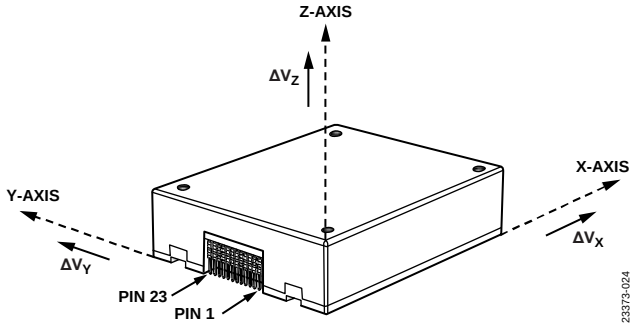


Figure 22. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (the x-axis is shown as follows):

$$\Delta V_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1} \right)$$

where:
D is the decimation rate = DEC_RATE + 1 (see Table 149).
fs is the sample rate.
d is the incremental variable in the summation formula.
a_x is the x-axis acceleration (accelerometer).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. Ensure that the frequency of the external clock is at least 700 Hz to prevent overflow in the delta velocity data registers at high acceleration levels.

Each axis of the delta velocity measurements has two output data registers. Figure 23 shows how the X_DELTVEL_LOW and X_DELTVEL_OUT registers combine to support a 32-bit, twos complement data format for the x-axis delta velocity measurements. This format also applies to the y- and x-axes.

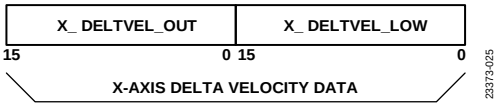


Figure 23. Delta Velocity Output Data Structure

X-Axis Delta Velocity (X_DELTVEL_LOW, X_DELTVEL_OUT)

The X_DELTVEL_LOW (see Table 70 and Table 71) and X_DELTVEL_OUT (see Table 72 and Table 73) registers contain the delta velocity data for the x-axis.

Table 70. X_DELTVEL_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x4C, 0x4D	Not applicable	R	No

Table 71. X_DELTVEL_LOW Bit Definition

Bits	Description (No Default)
[15:0]	X-axis delta velocity data, low word

Table 72. X_DELTVEL_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x4E, 0x4F	Not applicable	R	No

Table 73. X_DELTVEL_OUT Bit Definition

Bits	Description (No Default)
[15:0]	X-axis delta velocity data, high word, twos complement, ±200 m/sec range, 0 m/sec = 0x0000, 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

Y-Axis Delta Velocity (Y_DELTVEL_LOW, Y_DELTVEL_OUT)

The Y_DELTVEL_LOW (see Table 74 and Table 75) and Y_DELTVEL_OUT (see Table 76 and Table 77) registers contain the delta velocity data for the y-axis.

Table 74. Y_DELTVEL_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x50, 0x51	Not applicable	R	No

Table 75. Y_DELTVEL_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis delta velocity data, low word

Table 76. Y_DELTVEL_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x52, 0x53	Not applicable	R	No

Table 77. Y_DELTVEL_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Y-axis delta velocity data, high word, twos complement, ±200 m/sec range, 0 m/sec = 0x0000, 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

Z-Axis Delta Velocity (Z_DELTVEL_LOW, Z_DELTVEL_OUT)

The Z_DELTVEL_LOW (see Table 78 and Table 79) and Z_DELTVEL_OUT (see Table 80 and Table 81) registers contain the delta velocity data for the z-axis.

Table 78. Z_DELTVEL_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x54, 0x55	Not applicable	R	No

Table 79. Z_DELTVEL_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis delta velocity data, low word

Table 80. Z_DELTVEL_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x56, 0x57	Not applicable	R	No

Table 81. Z_DELTVEL_OUT Bit Definition

Bits	Description (No Default)
[15:0]	Z-axis delta velocity data, high word, twos complement, ±200 m/sec range, 0 m/sec = 0x0000, 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

Delta Velocity Resolution

Table 82 and Table 83 illustrate delta angle data in both 16-bit and 32-bit formats.

Table 82. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
$+200 \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+200/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+200/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-200/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-200/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
−200	−32,768	0x8000	1000 0000 0000 0000

Table 83. 32-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex
$+200 \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+200/2^{30}$	+2	0x00000002
$+200/2^{31}$	+1	0x00000001
0	0	0x00000000
$-200/2^{31}$	−1	0xFFFFFFFF
$-200/2^{30}$	−2	0xFFFFFFFE
−200	−2,147,483,648	0x80000000

REAL-TIME CLOCK (RTC)

The VDDRTC power supply pin (see Table 6, Pin 23) provides a separate supply for the RTC function. Connecting the VDDRTC pin to its own 3.3 V supply enables the RTC to keep track of time, even when the main supply (VDD) is off. Note that the VDDRTC power supply must always be connected, even when this function is not used.

Configure the RTC function by selecting one of two modes in Bit 0 of the CONFIG register (see Table 147). The RTC data is available in the TIME_MS_OUT (see Table 85), TIME_DH_OUT (see Table 87), and TIME_YM_OUT (see Table 89) registers. When using the elapsed timer mode, the time data registers start at 0x0000 when the device starts up (or resets) and begin keeping time in a similar manner to a stopwatch.

When using the clock and calendar mode, write the current time to the real-time registers in the following sequence: second(s) (TIME_MS_OUT, Bits[5:0]), minute(s) (TIME_ MS_OUT, Bits[13:8]), hour(s) (TIME_DH_OUT, Bits[5:0]), day(s) (TIME_DH_OUT, Bits[12:8]), month(s) (TIME_YM_OUT, Bits[3:0]), and year(s) (TIME_YM_OUT, Bits[14:8]).

The updates to the timer become active only after a write to TIME_YM_OUT, Bits[14:8] byte completes.

The RTC registers reflect the newly updated values only after the next seconds tick of the clock that follows the write to TIME_YM_OUT, Bits[14:8] (year(s)). Writing to TIME_YM_OUT, Bits[14:8] activates all of the timing values. Therefore, always write to this location last when updating the timer, even if the year information does not require updating.

Write the current time to each time data register after setting CONFIG, Bit 0 = 1 (DIN = 0x8003, DIN = 0x8AC1, DIN = 0x8B00). This sequence preserves the factory default for other bits in the CONFIG register. After configuring the CONFIG register, set GLOB_CMD, Bit 3 = 1 (DIN = 0x8003, DIN = 0x8204, DIN = 0x8300) to back up these settings in flash. Even though only VDDRTC must have power for time tracking, access to the time data in the TIME_xx_OUT registers requires normal operation (VDD = 3.3 V and full startup). Even when not using the RTC function, the supply voltage on VDDRTC must meet the conditions in Table 1.

RTC: Minutes and Seconds, TIME_MS_OUT

Table 84. TIME_MS_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x78, 0x79	Not applicable	R/W	No

Table 85. TIME_MS_OUT Bit Definitions

Bits	Description (No Default)
[15:14]	Not used
[13:8]	Minute(s), binary data, range = 0 to 59
[7:6]	Not used
[5:0]	Second(s), binary data, range = 0 to 59

RTC: Day and Hour, TIME_DH_OUT

Table 86. TIME_DH_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x7A, 0x7B	Not applicable	R/W	No

Table 87. TIME_DH_OUT Bit Definitions

Bits	Description (No Default)
[15:13]	Not used
[12:8]	Day(s), binary data, range = 1 to 31
[7:6]	Not used
[5:0]	Hour(s), binary data, range = 0 to 23

RTC: Year and Month, TIME_YM_OUT

Table 88. TIME_YM_OUT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x7C, 0x7D	Not applicable	R/W	No

Table 89. TIME_YM_OUT Bit Definitions

Bits	Description (No Default)
[15]	Not used
[14:8]	Year(s), binary data, range = 0 to 99, relative to 2000 AD
[7:4]	Not used
[3:0]	Month(s), binary data, range = 1 to 12

Product Identification, PROD_ID

The PROD_ID register (see Table 90 and Table 91) contains the numerical portion of the device number (16,486).

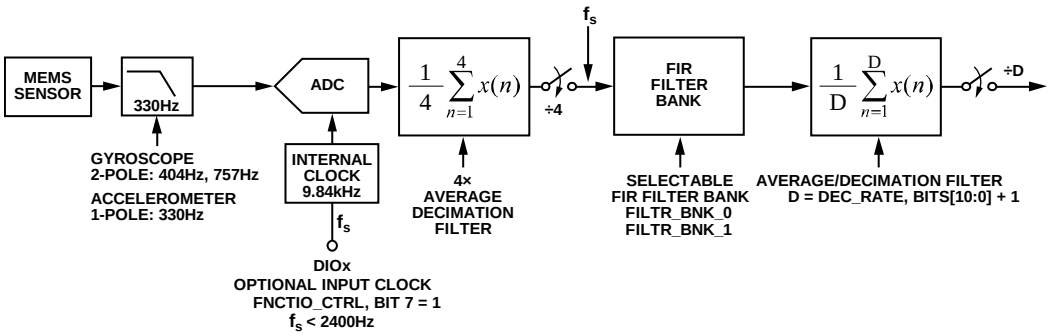
See Figure 15 for an example of how to use a looping read of this register to validate the integrity of the communication.

Table 90. PROD_ID Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x00	0x7E, 0x7F	0x4066	R	Yes

Table 91. PROD_ID Bit Definition

Bits	Description (Default = 0x4066)
[15:0]	Product identification = 0x4066



NOTES
1. WHEN FNCTIO_CTRL, BIT 7 = 1, f_S IS THE EXTERNAL INPUT CLOCK, AND EACH CLOCK PULSE ON THE DESIGNATED DIOx LINE (FNCTIO_CTRL, BITS[5:4]) STARTS A 4-SAMPLE BURST, AT A SAMPLE RATE OF 9.84 kHz. THESE FOUR SAMPLES FEED INTO THE 4× AVERAGE/DECIMATION FILTER, WHICH PRODUCES A DATA RATE THAT IS EQUAL TO THE INPUT CLOCK FREQUENCY.
2. WHEN FNCTIO_CTRL, BIT 7 = 0, f_S IS THE INTERNALLY GENERATED 2.46 kHz SAMPLE CLOCK.

23373-030

Figure 24. Sampling and Frequency Response Signal Flow

CALIBRATION

The signal chain of each inertial sensor (accelerometers and gyroscopes) includes the application of unique correction formulas, which come from extensive characterization of bias, sensitivity, alignment, and response to linear acceleration (gyroscopes) over a temperature range of −40°C to +85°C for every ADIS16486. These correction formulas are not accessible, but users can adjust bias and scale factor for each sensor individually through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain.

Calibration, Gyroscope Scale, X_GYRO_SCALE

The X_GYRO_SCALE register (see Table 92 and Table 93) allows users to adjust the scale factor for the x-axis gyroscopes. See Figure 25 for an illustration of how this scale factor influences the x-axis gyroscope data.

Table 92. X_GYRO_SCALE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x04, 0x05	0x0000	R/W	Yes

Table 93. X_GYRO_SCALE Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

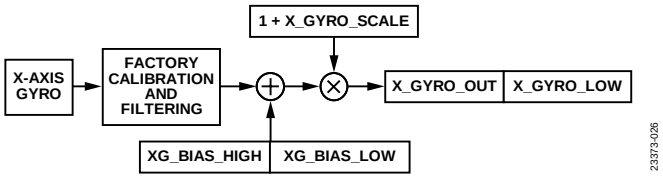


Figure 25. User Calibration Signal Path, Gyroscopes

Calibration, Gyroscope Scale, Y_GYRO_SCALE

The Y_GYRO_SCALE register (see Table 94 and Table 95) allows users to adjust the scale factor for the y-axis gyroscopes. This register influences the y-axis gyroscope measurements in the same manner that the X_GYRO_SCALE register influences the x-axis gyroscope measurements (see Figure 25).

Table 94. Y_GYRO_SCALE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x06, 0x07	0x0000	R/W	Yes

Table 95. Y_GYRO_SCALE Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Calibration, Gyroscope Scale, Z_GYRO_SCALE

The Z_GYRO_SCALE register (see Table 96 and Table 97) allows users to adjust the scale factor for the z-axis gyroscopes. This register influences the z-axis gyroscope measurements in the same manner that the X_GYRO_SCALE register influences the x-axis gyroscope measurements (see Figure 25).

Table 96. Z_GYRO_SCALE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x08, 0x09	0x0000	R/W	Yes

Table 97. Z_GYRO_SCALE Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Calibration, Accelerometer Scale, X_ACCL_SCALE

The X_ACCL_SCALE register (see Table 98 and Table 99) allows users to adjust the scale factor for the x-axis accelerometers. See Figure 26 for an illustration of how this scale factor influences the x-axis accelerometer data.

Table 98. X_ACCL_SCALE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x0A, 0x0B	0x0000	R/W	Yes

Table 99. X_ACCL_SCALE Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

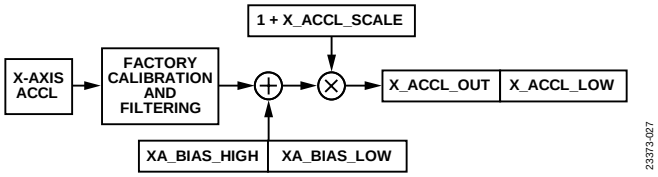


Figure 26. User Calibration Signal Path, Accelerometers

Calibration, Accelerometer Scale, Y_ACCL_SCALE

The Y_ACCL_SCALE register (see Table 100 and Table 101) allows users to adjust the scale factor for the y-axis accelerometers. This register influences the y-axis accelerometer measurements in the same manner that the X_ACCL_SCALE register influences the x-axis accelerometer measurements (see Figure 26).

Table 100. Y_ACCL_SCALE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x0C, 0x0D	0x0000	R/W	Yes

Table 101. Y_ACCL_SCALE Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Calibration, Accelerometer Scale, Z_ACCL_SCALE

The Z_ACCL_SCALE register (see Table 102 and Table 103) allows users to adjust the scale factor for the z-axis accelerometers. This register influences the z-axis accelerometer measurements in the same manner that the X_ACCL_SCALE register influences the x-axis accelerometer measurements (see Figure 26).

Table 102. Z_ACCL_SCALE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x0E, 0x0F	0x0000	R/W	Yes

Table 103. Z_ACCL_SCALE Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Calibration, Gyroscope Bias, XG_BIAS_LOW, XG_BIAS_HIGH

The XG_BIAS_LOW (see Table 104 and Table 105) and XG_BIAS_HIGH (see Table 106 and Table 107) registers combine to allow users to adjust the bias of the x-axis gyroscopes. The digital format examples in Table 40 also apply to the XG_BIAS_HIGH register, and the digital format examples in Table 41 apply to the 32-bit number that comes from combining the XG_BIAS_LOW and XG_BIAS_HIGH registers. See Figure 25 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Table 104. XG_BIAS_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x10, 0x11	0x0000	R/W	Yes

Table 105. XG_BIAS_LOW Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope offset correction, low word, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 106. XG_BIAS_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x12, 0x13	0x0000	R/W	Yes

Table 107. XG_BIAS_HIGH Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope offset correction, high word, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Calibration, Gyroscope Bias, YG_BIAS_LOW, YG_BIAS_HIGH

The YG_BIAS_LOW (see Table 108 and Table 109) and YG_BIAS_HIGH (see Table 110 and Table 111) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The digital format examples in Table 40 also apply to the YG_BIAS_HIGH register, and the digital format examples in Table 41 apply to the 32-bit number that comes from combining the YG_BIAS_LOW and YG_BIAS_HIGH registers. These registers influence the y-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 25).

Table 108. YG_BIAS_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x14, 0x15	0x0000	R/W	Yes

Table 109. YG_BIAS_LOW Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope offset correction, low word, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 110. YG_BIAS_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x16, 0x17	0x0000	R/W	Yes

Table 111. YG_BIAS_HIGH Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope offset correction, high word, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Calibration, Gyroscope Bias, ZG_BIAS_LOW, ZG_BIAS_HIGH

The ZG_BIAS_LOW (see Table 112 and Table 113) and ZG_BIAS_HIGH (see Table 114 and Table 115) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The digital format examples in Table 40 also apply to the ZG_BIAS_HIGH register, and the digital format examples in Table 41 apply to the 32-bit number that comes from combining the ZG_BIAS_LOW and ZG_BIAS_HIGH registers. These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 25).

Table 112. ZG_BIAS_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x18, 0x19	0x0000	R/W	Yes

Table 113. ZG_BIAS_LOW Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope offset correction, low word, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 114. ZG_BIAS_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x1A, 0x1B	0x0000	R/W	Yes

Table 115. ZG_BIAS_HIGH Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope offset correction, high word, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Calibration, Accelerometer Bias, XA_BIAS_LOW, XA_BIAS_HIGH

The XA_BIAS_LOW (see Table 116 and Table 117) and XA_BIAS_HIGH (see Table 118 and Table 119) registers combine to allow users to adjust the bias of the x-axis accelerometers. The digital format examples in Table 54 also apply to the XA_BIAS_HIGH register, and the digital format examples in Table 55 apply to the 32-bit number that comes from combining the XA_BIAS_LOW and XA_BIAS_HIGH registers. See Figure 26 for an illustration of how these two registers combine and influence the x-axis accelerometer measurements.

Table 116. XA_BIAS_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x1C, 0x1D	0x0000	R/W	Yes

Table 117. XA_BIAS_LOW Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g* ÷ 2^{16} = ~0.01221 μ*g*

Table 118. XA_BIAS_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x1E, 0x1F	0x0000	R/W	Yes

Table 119. XA_BIAS_HIGH Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Calibration, Accelerometer Bias, YA_BIAS_LOW, YA_BIAS_HIGH

The YA_BIAS_LOW (see Table 120 and Table 121) and YA_BIAS_HIGH (see Table 122 and Table 123) registers combine to allow users to adjust the bias of the y-axis accelerometers. The digital format examples in Table 54 also apply to the YA_BIAS_HIGH register, and the digital format examples in Table 55 apply to the 32-bit number that comes from combining the YA_BIAS_LOW and YA_BIAS_HIGH registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 26).

Table 120. YA_BIAS_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x20, 0x21	0x0000	R/W	Yes

Table 121. YA_BIAS_LOW Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g* ÷ 2^{16} = ~0.01221 μ*g*

Table 122. YA_BIAS_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x22, 0x23	0x0000	R/W	Yes

Table 123. YA_BIAS_HIGH Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Calibration, Accelerometer Bias, ZA_BIAS_LOW, ZA_BIAS_HIGH

The ZA_BIAS_LOW (see Table 124 and Table 125) and ZA_BIAS_HIGH (see Table 126 and Table 127) registers combine to allow users to adjust the bias of the z-axis accelerometers. The digital format examples in Table 54 also apply to the ZA_BIAS_HIGH register, and the digital format examples in Table 55 apply to the 32-bit number that comes from combining the ZA_BIAS_LOW and ZA_BIAS_HIGH registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 26).

Table 124. ZA_BIAS_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x24, 0x25	0x0000	R/W	Yes

Table 125. ZA_BIAS_LOW Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g* ÷ 2^{16} = ~0.01221 μ*g*

Table 126. ZA_BIAS_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x26, 0x27	0x0000	R/W	Yes

Table 127. ZA_BIAS_HIGH Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Scratch Registers, USER_SCR_x

The USER_SCR_1 (see Table 128 and Table 129), USER_SCR_2 (see Table 130 and Table 131), USER_SCR_3 (see Table 132 and Table 133), and USER_SCR_4 (see Table 134 and Table 135) registers provide four locations for users to store information.

Table 128. USER_SCR_1 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x74, 0x75	0x0000	R/W	Yes

Table 129. USER_SCR_1 Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	User defined

Table 130. USER_SCR_2 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x76, 0x77	0x0000	R/W	Yes

Table 131. USER_SCR_2 Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	User defined

Table 132. USER_SCR_3 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x78, 0x79	0x0000	R/W	Yes

Table 133. USER_SCR_3 Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	User defined

Table 134. USER_SCR_4 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x7A, 0x7B	0x0000	R/W	Yes

Table 135. USER_SCR_4 Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	User defined

Flash Memory Endurance Counter, FLSHCNT_LOW, FLSHCNT_HIGH

The FLSHCNT_LOW (see Table 136 and Table 137) and FLSHCNT_HIGH (see Table 138 and Table 139) registers combine to create a 32-bit binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 27 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

Table 136. FLSHCNT_LOW Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x7C, 0x7D	Not applicable	R/W	Yes

Table 137. FLSHCNT_LOW Bit Definition

Bits	Description (No Default)
[15:0]	Flash memory write counter, low word

Table 138. FLSHCNT_HIGH Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x02	0x7E, 0x7F	Not applicable	R/W	Yes

Table 139. FLSHCNT_HIGH Bit Definition

Bits	Description (No Default)
[15:0]	Flash memory write counter, high word

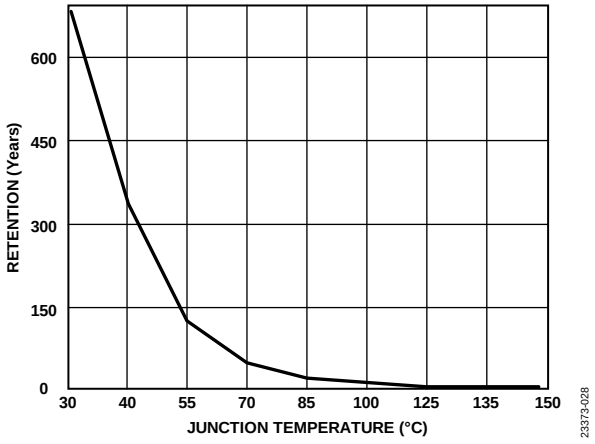


Figure 27. Flash Memory Retention

Global Commands, GLOB_CMD

The GLOB_CMD register (see Table 140 and Table 141) provides trigger bits for several operations. Write a 1 to the appropriate bit in the GLOB_CMD register to start a desired function.

Table 140. GLOB_CMD Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x02, 0x03	0x0000	W	No

Table 141. GLOB_CMD Bit Definitions

Bits	Description (Default = 0x0000)
[15:8]	Not used
7	Software reset
6	Factory calibration restore
[5:4]	Not used
3	Flash memory update
2	Not used
1	Self test
0	Bias correction update

Software Reset

Select Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 7 = 1 (DIN = 0x8280, then DIN = 0x8300) to initiate a reset of the ADIS16486. This reset removes all data, initializes all of the registers from their flash settings, and restarts data sampling and processing. This function provides a firmware alternative to providing a low pulse on the $\overline{\text{RST}}$ pin (see Table 6).

Factory Calibration Restore

Select Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 6 = 1 (DIN = 0x8240, then DIN = 0x8300) to restore the factory calibration. This restoration writes 0x0000 to the following registers: X_GYRO_SCALE, Y_GYRO_SCALE, Z_GYRO_SCALE, X_ACCL_SCALE, Y_ACCL_SCALE, Z_ACCL_SCALE, XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_HIGH, XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, and ZA_BIAS_HIGH.

Flash Memory Update

Select Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 3 = 1 (DIN = 0x8208, then DIN = 0x8300) to initiate a manual flash update. SYS_E_FLAG, Bit 6 (see Table 20) identifies success (0) or failure (1) in completing this process.

ODST

Select Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 1 = 1 (DIN = 0x8202, then DIN = 0x8300) to run the ODST routine, which executes the following steps:

1. Measure the output on each sensor.
2. Activate an internal force on the mechanical elements of each sensor, which simulates the force associated with actual inertial motion.
3. Measure the output response on each sensor.
4. Deactivate the internal force on each sensor.
5. Calculate the difference between the force on and normal operating conditions (force off).
6. Compare the difference with internal pass and fail criteria.
7. Report the pass and fail results for each sensor in DIAG_STS (see Table 22) and the overall pass and fail flag in SYS_E_FLAG, Bit 5 (see Table 20).

When using an external clock, the self test execution times may vary from the 12 ms listed in Table 1. In addition, false positive results are possible when executing the ODST while the device is in motion.

Bias Correction Update

Select Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 0 = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the continuous bias estimator (CBE). Ensure that the inertial platform is stable during the entire average time for optimal bias estimates.

Auxiliary Input and Output Line Configuration, FNCTIO_CTRL

The FNCTIO_CTRL register (see Table 142 and Table 143) provides configuration control for each input and output pin (DIO1, DIO2, DIO3, and DIO4). Each DIOx pin supports only one function at a time. In cases where a single pin has two assignments, the enable bit for the lower priority function automatically resets to zero (disabling the lower priority function). The order of priority is as follows, from highest priority to lowest priority: data ready, sync clock input, alarm indicator, and general-purpose. Changing the FNCTIO_CTRL, Bits[5:4] bit settings requires an execution time of 75 ms, whereas changing the settings of the remaining bits in the FNCTIO_CTRL register only takes 3 ms. During this execution time (75 ms or 3 ms), the operational state and the contents of the register remain unchanged. However, the SPI interface supports normal communication (for accessing other registers).

Table 142. FNCTIO_CTRL Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x06, 0x07	0x000D	R/W	Yes

Table 143. FNCTIO_CTRL Bit Definitions

Bits	Description (Default = 0x000D)
[15:12]	Not used
11	Alarm indicator: 1 = enabled, 0 = disabled
10	Alarm indicator polarity: 1 = positive, 0 = negative
[9:8]	Alarm indicator line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
7	Sync clock input enable: 1 = enabled, 0 = disabled
6	Sync clock input polarity: 1 = rising edge, 0 = falling edge
[5:4]	Sync clock input line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
3	Data ready enable: 1 = enabled, 0 = disabled
2	Data ready polarity: 1 = positive, 0 = negative
[1:0]	Data ready line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4

Data Ready Indicator

FNCTIO_CTRL, Bits[3:0] provide three configuration options for the data ready function: on and off, polarity, and which DIOx pin is used. The primary purpose of this signal is to drive the interrupt control line of an embedded processor to synchronize data collection and minimize latency. The factory default assigns the DIO2 pin as a positive polarity, data ready signal. This means that the data in the output registers is valid when the DIO2 line is high (see Figure 28). This configuration is intended when the DIO2 pin drives an interrupt service pin that activates on a low to high pulse.

Figure 28. Data Ready, when FNCTIO_CTRL, Bits[3:0] = 1101 (Default)

Use the following sequence to change this assignment to the DIO1 pin with a negative polarity:

1. Select Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL, Bits[3:0] = 1000 (DIN = 0x8608, then DIN = 0x8700).

The period of the data ready signal can vary by up to ±2%.

Input Sync and Clock Control

FNCTIO_CTRL, Bits[7:4] provide configuration options for using one of the DIOx pins as an input synchronization signal for sampling inertial sensor data. For example, use the following sequence to establish the DIO4 pin as a positive polarity, input clock pin, and to keep the factory default setting for the data ready function:

1. Select Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL, Bits[7:0] = 0xFD (DIN = 0x86FD).
3. Set FNCTIO_CTRL, Bits[15:8] = 0x00 (DIN = 0x8700).

Note that this command also disables the internal sampling clock. Therefore, data sampling does not occur if an input clock signal is not present. Use an input clock frequency of 2400 Hz for the best performance.

Alarm Indicator

FNCTIO_CTRL, Bits[11:8] provide three configuration options for using one of the DIOx pins as an alarm indicator: on and off, polarity, and the DIOx pin. The primary purpose of this signal is to provide an output signal that activates when a bit in the SYS_E_FLAG register = 1 (see Table 20). For example, use the following sequence to establish the DIO3 pin as a negative-polarity, alarm indicator, while preserving the factory default setting for the data ready function:

1. Select Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL, Bits[7:0] = 0x0D (DIN = 0x860D).
3. Set FNCTIO_CTRL, Bits[15:8] = 0x0A (DIN = 0x870A).

General-Purpose Input and Output Control, GPIO_CTRL

Table 144. GPIO_CTRL Register Definition[1]

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x08, 0x09	0x00X0	R/W	Yes

[1] GPIO_CTRL, Bits[7:4] reflect the logic levels on the DIOx pins and do not have a default setting.

Table 145. GPIO_CTRL Bit Definitions[1]

Bits	Description (Default = 0x00X0)
[15:8]	Don't care
7	General-Purpose Input and Output Line 4 (DIO4) data level
6	General-Purpose Input and Output Line 3 (DIO3) data level
5	General-Purpose Input and Output Line 2 (DIO2) data level
4	General-Purpose Input and Output Line 1 (DIO1) data level
3	DIO4 direction control (1 = output, 0 = input)
2	DIO3 direction control (1 = output, 0 = input)
1	DIO2 direction control (1 = output, 0 = input)
0	DIO1 direction control (1 = output, 0 = input)

[1] GPIO_CTRL, Bits[7:4] reflect the logic levels on the DIOx pins and do not have a default setting.

When the FNCTIO_CTRL register does not configure a DIOx pin, the GPIO_CTRL register provides register controls for general-purpose use of the pin. GPIO_CTRL, Bits[3:0] provide input and output assignment controls for each line. When the DIOx pins are inputs, monitor their level by reading GPIO_CTRL, Bits[7:4]. When the DIOx pins are used as outputs, set their level by writing to GPIO_CTRL, Bits[7:4]. For example, use the following sequence to set the DIO1 and DIO3 pins as high and low output lines, respectively, and set the DIO2 and DIO4 pins as input lines:

1. Select Page 3 (DIN = 0x8003).
2. Set GPIO_CTRL, Bits[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

Miscellaneous Configuration, CONFIG

The CONFIG register (see Table 146 and Table 147) provides configuration options for the linear *g* compensation in the gyroscopes (on and off), point of percussion alignment for the accelerometers (on and off), and the RTC function.

Table 146. CONFIG Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x0A, 0x0B	0x00C0	R/W	Yes

Table 147. CONFIG Bit Definitions

Bits	Description (Default = 0x00C0)
[15:8]	Not used
7	Linear *g* compensation for gyroscopes (1 = enabled)
6	Point of percussion alignment (1 = enabled)
[5:2]	Not used
1	RTC, daylight savings time (1: enabled, 0: disabled)
0	RTC control (1: relative and elapsed timer mode, 0: calendar mode)

Point of Percussion

CONFIG, Bit 6 offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 29. To activate this feature, select Page 3 (DIN = 0x8003) and set CONFIG, Bit 6 = 1 (DIN = 0x8A40, DIN = 0x8B00).

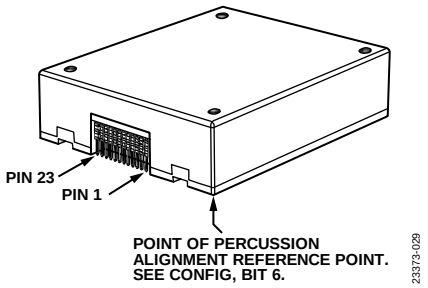


Figure 29. Point of Percussion Reference Point

Linear Acceleration Effect on Gyroscope Bias

The ADIS16486 includes first-order compensation for the linear *g* effect in the gyroscopes, which uses the following model:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} LG_{11} & LG_{12} & LG_{13} \\ LG_{21} & LG_{22} & LG_{23} \\ LG_{31} & LG_{32} & LG_{33} \end{bmatrix} \times \begin{bmatrix} A_X \\ A_Y \\ A_Z \end{bmatrix} + \begin{bmatrix} \omega_{XPC} \\ \omega_{YPC} \\ \omega_{ZPC} \end{bmatrix}$$

The linear *g* correction factors, LG_{XY}, apply correction for linear acceleration in all three directions to the data path of each gyroscope (ω_{XPC}, ω_{YPC}, and ω_{ZPC}) at the rate of the data samples (2460 SPS when using the internal clock). CONFIG, Bit 7 provides an on and off control for this compensation. The factory default value for this bit activates this compensation. To turn the compensation off, select Page 3 (DIN = 0x8003) and set CONFIG, Bit 7 = 0 (DIN = 0x8A40, then DIN = 0x8B00). This command sequence also preserves the default setting for the point of percussion alignment function (on).

Decimation Filter, DEC_RATE

The DEC_RATE register (see Table 148 and Table 149) provides user control for the final filter stage (see Figure 24), which averages and decimates the accelerometer and gyroscope data, while also extending the time that the delta angle and delta velocity track between each update. The output sample rate is equal to 2460/(DEC_RATE + 1). When using the external clock option (FNCTIO_CTRL, Bits[7:4], see Figure 24), replace 2460 in this relationship with the input clock frequency. For example, select Page 3 (DIN = 0x8003), and set DEC_RATE = 0x18 (DIN = 0x8C18, then DIN = 0x8D00) to reduce the output sample rate to 98.4 SPS (2460 ÷ 25).

Table 148. DEC_RATE Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x0C, 0x0D	0x0000	R/W	Yes

Table 149. DEC_RATE Bit Definitions

Bits	Description (Default = 0x0000)
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 2047, see Figure 24 for the impact on sample rate

Continuous Bias Estimation, NULL_CNFG

The NULL_CNFG register (see Table 150 and Table 151) provides the configuration controls for the CBE, which is associated with the bias correction update command in GLOB_CMD, Bit 0 (see Table 141). NULL_CNFG, Bits[3:0] establishes the total average time (t_A) for the bias estimates, and NULL_CNFG, Bits[13:8] provides on and off controls for each sensor. The factory default configuration for the NULL_CNFG register enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~26.64 sec. This calculation assumes that the internal sample clock (f_S = 2460 SPS) is used. If the user supplies an external clock by setting Bit 7 to 1 of the FNCTIO_CRTL register (see Table 142 and Table 143), f_S is the inertial measurement unit (IMU) sample rate before decimation.

Table 150. NULL_CNFG Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x0E, 0x0F	0x070A	R/W	Yes

Table 151. NULL_CNFG Bit Definitions

Bits	Description (Default = 0x070A)
[15:14]	Not used.
13	Z-axis acceleration bias correction enable (1 = enabled).
12	Y-axis acceleration bias correction enable (1 = enabled).
11	X-axis acceleration bias correction enable (1 = enabled).
10	Z-axis gyroscope bias correction enable (1 = enabled).
9	Y-axis gyroscope bias correction enable (1 = enabled).
8	X-axis gyroscope bias correction enable (1 = enabled).
[7:4]	Not used.
[3:0]	Time base control (TBC), range is 0 to 13 (default = 10), and time base (t_B) = $2^{TBC}/f_S$, where f_S is the IMU sample rate before decimation and is 2460 SPS if the factory default internal clock is used. The t_A required for autonull = 64 × t_B.

When a sensor bit in the NULL_CNFG register is active (equal to 1), setting GLOB_CMD, Bit 0 = 1 (DIN sequence: 0x8003, 0x8201, 0x8300) causes the corresponding bias correction register to automatically update with a value that corrects for its present bias error (from the CBE). For example, setting NULL_CNFG, Bit 8 = 1 causes an update in the XG_BIAS_LOW (see Table 105) and XG_BIAS_HIGH (see Table 107) registers.

Power Management, SLP_CNT

The SLP_CNT register (see Table 152 and Table 153) provides controls for both power-down mode and sleep mode. The trade-off between power-down mode and sleep mode is idle power and recovery time. Power-down mode offers the best power consumption but requires the most time to recover. In addition, all volatile settings are lost during power-down, whereas sleep mode preserves these settings.

Table 152. SLP_CNT Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x10, 0x11	Not applicable	R/W	No

Table 153. SLP_CNT Bit Definitions

Bits	Description (No Default)
[15:10]	Not used
9	Power-down mode
8	Normal sleep mode
[7:0]	Programmable time bits, 1 sec/LSB, 0x00 = indefinite

To initiate sleep mode for a specific period, select Page 3 (DIN = 0x8003), write the amount of sleep time to SLP_CNT, Bits[7:0], and set SLP_CNT, Bit 8 = 1 (DIN = 0x9101). Sleep mode begins when the $\overline{CS}$ line goes high after setting SLP_CNT, Bit 8 = 1. Use the following sequence to place the ADIS16486 into sleep mode for 100 sec:

1. Select Page 3 (DIN = 0x8003).
2. Set SLP_CNT, Bits[7:0] = 0x64 (DIN = 0x9064), 100 sec sleep time.
3. Set SLP_CNT, Bit 8 = 1 (DIN = 0x9101), start sleep mode.

To initiate an indefinite sleep mode, set SLP_CNT, Bits[7:0] = 0x00 (DIN = 0x9000), and then set SLP_CNT, Bit 8 = 1 (DIN = 0x9101). To initiate a power-down period of 100 sec, use the sequence for placing the ADIS16486 into sleep mode for 100 sec with one exception: set SLP_CNT, Bit 9 = 1 (DIN = 0x9102) instead of setting SLP_CNT, Bit 8 = 1 (DIN = 0x9101). To initiate an indefinite power-down, set SLP_CNT, Bits[7:0] = 0x00 first, and then set SLP_CNT, Bit 9 = 1 (DIN = 0x9102).

To wake the device from sleep or power-down mode, use one of the following options to restore normal operation:

- Assert $\overline{CS}$ from high to low.
- Pulse $\overline{RST}$ low, and then high again.
- Cycle the power.

If the sleep mode and power-down mode bits are both set to high, the normal sleep mode bit (SLP_CNT, Bit 8) takes precedence.

FIR Filter Control, FILTR_BNK_0, FILTR_BNK_1

The FILTR_BNK_0 (see Table 154 and Table 155) and FILTR_BNK_1 (see Table 156 and Table 157) registers provide the configuration controls for the FIR filter bank in the signal chain of each sensor (see Figure 24). These registers provide on and off control for the FIR bank for each inertial sensor, along with the FIR bank (A, B, C, D) that each sensor uses.

Write commands to the FILTR_BNK_0 and FILTR_BNK_1 registers, which enable or configure the FIR filters and take up to 101 µs to fully process. During this execution time, the SPI interface supports normal operation, and the register values update at the conclusion of the update process.

Table 154. FILTR_BNK_0 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x16, 0x17	0x0000	R/W	Yes

Table 155. FILTR_BNK_0 Bit Definitions

Bits	Description (Default = 0x0000)
15	Don't care
14	Y-axis accelerometer filter enable (1 = enabled)
[13:12]	Y-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
11	X-axis accelerometer filter enable (1 = enabled)
[10:9]	X-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
8	Z-axis gyroscope filter enable (1 = enabled)
[7:6]	Z-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
5	Y-axis gyroscope filter enable (1 = enabled)
[4:3]	Y-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
2	X-axis gyroscope filter enable (1 = enabled)
[1:0]	X-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Table 156. FILTR_BNK_1 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x18, 0x19	0x0000	R/W	Yes

Table 157. FILTR_BNK_1 Bit Definitions

Bits	Description (Default = 0x0000)
[15:3]	Don't care
2	Z-axis accelerometer filter enable (1 = enabled)
[1:0]	Z-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Alarm Configuration, ALM_CNFG_0, ALM_CNFG_1

The ALM_CNFG_0 (see Table 158 and Table 159) and ALM_CNFG_1 (see Table 160 and Table 161) registers provide three configuration control options for the alarm functions of each inertial sensor: on and off, polarity, and mode of operation (static and dynamic).

Table 158. ALM_CNFG_0 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x20, 0x21	0x0000	R/W	Yes

Solving for ΔX_ACCL_OUT, ΔZ_GYRO_OUT, ΔY_GYRO_OUT, and ΔX_GYRO_OUT

Use Equation 2 to Equation 5 to solve for ΔX_ACCL_OUT, ΔZ_GYRO_OUT, ΔY_GYRO_OUT, and ΔX_GYRO_OUT in Bits[13:12], Bits[9:8], Bits[5:4], and Bits[1:0] in Table 159.

$$\Delta X\_ACCL\_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} X_A(n) - \sum_{n=0}^{7} X_A(n-104)\right) \quad (2)$$

where X_A = X_ACCL_OUT.

$$\Delta Z\_GYRO\_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Z_G(n) - \sum_{n=0}^{7} Z_G(n-104)\right) \quad (3)$$

where Z_G = Z_GYRO_OUT.

$$\Delta Y\_GYRO\_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Y_G(n) - \sum_{n=0}^{7} Y_G(n-104)\right) \quad (4)$$

where Y_G = Y_GYRO_OUT.

$$\Delta X\_GYRO\_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} X_G(n) - \sum_{n=0}^{7} X_G(n-104)\right) \quad (5)$$

where X_G = X_GYRO_OUT.

Solving for ΔZ_ACCL_OUT and ΔY_ACCL_OUT

Use Equation 6 and Equation 7 to solve for ΔZ_ACCL_OUT and ΔY_ACCL_OUT in Bits[5:4] and Bits[1:0] in Table 161.

$$\Delta Z\_ACCL\_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Z_A(n) - \sum_{n=0}^{7} Z_A(n-104)\right) \quad (6)$$

where Z_A = Z_ACCL_OUT.

$$\Delta Y\_ACCL\_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Y_A(n) - \sum_{n=0}^{7} Y_A(n-104)\right) \quad (7)$$

where Y_A = Y_ACCL_OUT.

Table 159. ALM_CNFG_0 Bit Definitions

Bits	Description (Default = 0x0000)
15	X-axis accelerometer. 0: alarm is off, and 1: alarm is on.
14	Not used.
[13:12]	X-axis accelerometer polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS, Bit 3 = 1, see Table 24). 00: X_ACCL_OUT < XA_ALM_MAGN. 01: ΔX_ACCL_OUT < XA_ALM_MAGN (see Equation 2). 10: X_ACCL_OUT > XA_ALM_MAGN. 11: ΔX_ACCL_OUT > XA_ALM_MAGN (see Equation 2).
11	Z-axis gyroscope. 0: alarm is off, and 1: alarm is on.
10	Not used.
[9:8]	Z-axis gyroscope polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS, Bit 2 = 1, see Table 24). 00: Z_GYRO_OUT < ZG_ALM_MAGN. 01: ΔZ_GYRO_OUT < ZG_ALM_MAGN (see Equation 3). 10: Z_GYRO_OUT > ZG_ALM_MAGN. 11: ΔZ_GYRO_OUT > ZG_ALM_MAGN (see Equation 3).
7	Y-axis gyroscope. 0: alarm is off, and 1: alarm is on.
6	Not used.
[5:4]	Y-axis gyroscope polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS, Bit 1 = 1, see Table 24). 00: Y_GYRO_OUT < YG_ALM_MAGN. 01: ΔY_GYRO_OUT < YG_ALM_MAGN (see Equation 4). 10: Y_GYRO_OUT > YG_ALM_MAGN. 11: ΔY_GYRO_OUT > YG_ALM_MAGN (see Equation 4).

Bits	Description (Default = 0x0000)
3	X-axis gyroscope. 0: alarm is off, and 1: alarm is on.
2	Not used.
1:0	X-axis gyroscope polarity and mode settings. Select one of the four options for the condition that triggers the alarm flag (ALM_STS, Bit 0 = 1, see Table 24). 00: X_GYRO_OUT < XG_ALM_MAGN. 01: ΔX_GYRO_OUT < XG_ALM_MAGN (see Equation 5). 10: X_GYRO_OUT > XG_ALM_MAGN. 11: ΔX_GYRO_OUT > XG_ALM_MAGN (see Equation 5).

Table 160. ALM_CNFG_1 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x22, 0x23	0x0000	R/W	Yes

Table 161. ALM_CNFG_1 Bit Definitions

Bits	Description (Default = 0x0000)
[15:8]	Not used.
7	Z-axis accelerometer. 0: alarm is off, and 1: alarm is on.
6	Not used.
[5:4]	Z-axis accelerometer polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS, Bit 5 = 1, see Table 24). 00: Z_ACCL_OUT < ZA_ALM_MAGN. 01: ΔZ_ACCL_OUT < ZA_ALM_MAGN (see Equation 6). 10: Z_ACCL_OUT > ZA_ALM_MAGN. 11: ΔZ_ACCL_OUT > ZA_ALM_MAGN (see Equation 6).
4	Z-axis accelerometer mode. 0: static, and 1: dynamic.
3	Y-axis accelerometer. 0: alarm is off, and 1: alarm is on.
2	Not used.
[1:0]	Y-axis accelerometer polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS, Bit 4 = 1, see Table 24). 00: Y_ACCL_OUT < YA_ALM_MAGN. 01: ΔY_ACCL_OUT < YA_ALM_MAGN (see Equation 7). 10: Y_ACCL_OUT > YA_ALM_MAGN. 11: ΔY_ACCL_OUT > YA_ALM_MAGN (see Equation 7).

X-Axis Gyroscope Alarm, XG_ALM_MAGN

The XG_ALM_MAGN register (see Table 162 and Table 163) contains the alarm threshold for the x-axis gyroscope when ALM_CNFG_0, Bit 3 = 1 (see Table 159). This alarm is associated with the alarm flag in ALM_STS, Bit 0 (see Table 24).

Table 162. XG_ALM_MAGN Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x28, 0x29	0x0000	R/W	Yes

Table 163. XG_ALM_MAGN Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Alarm Example

Use the following sequence to configure the x-axis gyroscopes alarm to be active (ALM_STS, Bit 0 = 1) when the rate of rotation around the x-axis exceeds 100°/sec:

1. Select Page 3 (DIN = 0x8003).
2. Set XG_ALM_MAGN, Bits[7:0] = 0x88 (DIN = 0xA888).
3. Set XG_ALM_MAGN, Bits[15:8] = 0x13 (DIN = 0xA913).
4. Set ALM_CNFG_1, Bits[7:0] = 0x0C (DIN = 0xA00C).
5. Set ALM_CNFG_1, Bits[15:8] = 0x00 (DIN = 0xA100).

The value for the XG_ALM_MAGN register is 0x1388, as shown in the equation

$$100°/sec \div 0.02°/sec/LSB = 5000\ LSB = 0x1388$$

Y-Axis Gyroscope Alarm, YG_ALM_MAGN

The YG_ALM_MAGN register (see Table 164 and Table 165) contains the alarm threshold for the y-axis gyroscope when ALM_CNFG_0, Bit 7 = 1 (see Table 159). This alarm is associated with the alarm flag in ALM_STS, Bit 1 (see Table 24).

Table 164. YG_ALM_MAGN Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x2A, 0x2B	0x0000	R/W	Yes

Table 165. YG_ALM_MAGN Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Z-Axis Gyroscope Alarm, ZG_ALM_MAGN

The ZG_ALM_MAGN register (see Table 166 and Table 167) contains the alarm threshold for the z-axis gyroscope when ALM_CNFG_0, Bit 11 = 1 (see Table 159). This alarm is associated with the alarm flag in ALM_STS, Bit 2 (see Table 24).

Table 166. ZG_ALM_MAGN Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x2C, 0x2D	0x0000	R/W	Yes

Table 167. ZG_ALM_MAGN Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

X-Axis Accelerometer Alarm, XA_ALM_MAGN

The XA_ALM_MAGN register (see Table 168 and Table 169) contains the alarm threshold for the x-axis accelerometer when ALM_CNFG_0, Bit 15 = 1 (see Table 159). This alarm is associated with the alarm flag in ALM_STS, Bit 3 (see Table 24).

Table 168. XA_ALM_MAGN Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x2E, 0x2F	0x0000	R/W	Yes

Table 169. XA_ALM_MAGN Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Y-Axis Accelerometer Alarm, YA_ALM_MAGN

The YA_ALM_MAGN register (see Table 170 and Table 171) contains the alarm threshold for the y-axis accelerometer when ALM_CNFG_1, Bit 3 = 1 (see Table 161). This alarm is associated with the alarm flag in ALM_STS, Bit 4 (see Table 24).

Table 170. YA_ALM_MAGN Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x30, 0x31	0x0000	R/W	Yes

Table 171. YA_ALM_MAGN Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Z-Axis Accelerometer Alarm, ZA_ALM_MAGN

The ZA_ALM_MAGN register (see Table 172 and Table 173) contains the alarm threshold for the z-axis accelerometer when ALM_CNFG_1, Bit 7 = 1 (see Table 161). This alarm is associated with the alarm flag in ALM_STS, Bit 5 (see Table 24).

Table 172. ZA_ALM_MAGN Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x32, 0x33	0x0000	R/W	Yes

Table 173. ZA_ALM_MAGN Bit Definition

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Firmware Revision, FIRM_REV

The FIRM_REV register (see Table 174 and Table 175) provides the firmware revision for the internal firmware. This register uses a binary coded decimal (BCD) format, where each nibble represents a digit. For example, if FIRM_REV = 0x1234, the firmware revision is 12.34.

Table 174. FIRM_REV Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x78, 0x79	Not applicable	R	Yes

Table 175. FIRM_REV Bit Definitions

Bits	Description (No Default)
[15:12]	Firmware revision BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Firmware revision BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Firmware revision BCD code, tenths digit, numerical format = 4-bit binary, range = 0 to 9
[3:0]	Firmware revision BCD code, hundredths digit, numerical format = 4-bit binary, range = 0 to 9

Firmware Revision Day and Month, FIRM_DM

The FIRM_DM register (see Table 176 and Table 177) contains the month and day of the factory configuration date. FIRM_DM, Bits[15:12] and FIRM_DM, Bits[11:8] contain digits that represent the month of the factory configuration in a BCD format. For example, November is the 11th month in a year and is represented by FIRM_DM, Bits[15:8] = 0x11. FIRM_DM, Bits[7:4] and FIRM_DM, Bits[3:0] contain digits that represent the day of factory configuration in a BCD format. For example, the 27th day of the month is represented by FIRM_DM, Bits[7:0] = 0x27.

Table 176. FIRM_DM Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x7A, 0x7B	Not applicable	R	Yes

Table 177. FIRM_DM Bit Definitions

Bits	Description (No Default)
[15:12]	Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2
[11:8]	Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration day BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration day BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

Firmware Revision Year, FIRM_Y

The FIRM_Y register (see Table 178 and Table 179) contains the year of the factory configuration date. For example, the year, 2013, is represented by FIRM_Y = 0x2013.

Table 178. FIRM_Y Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x7C, 0x7D	Not applicable	R	Yes

Table 179. FIRM_Y Bit Definitions

Bits	Description (No Default)
[15:12]	Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

Boot Revision Number, BOOT_REV

Table 180. BOOT_REV Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x03	0x7E, 0x7F	Not applicable	R	Yes

Table 181. BOOT_REV Bit Definitions

Bits	Description (No Default)
[15:8]	Binary, major revision number
[7:0]	Binary, minor revision number

Continuous SRAM Testing

This device employs a CRC function on the SRAM memory blocks that contain the program code (CODE_SIGTR_xxx) and the calibration coefficients (CAL_DRVTN_xxx). This process operates in the background and generates real-time 32-bit CRC values for the program code and calibration coefficients, respectively. At the conclusion of each cycle, the processor writes these calculated

values in the CAL_SIGTR_xxx and CODE_DRVTN_xxx registers (see Table 187, Table 189, Table 195, and Table 197) and compares them with the signature values, which reflect the state of these memory locations at the time of factory configuration. When the calculation results do not match the signature values, SYS_E_FLAG, Bit 2 increases to a 1. The respective signature values are available for user access through the CAL_SIGTR_xxx and CODE_DRVTN_xxx registers (see Table 183, Table 185, Table 191, and Table 193). The following conditions must be met for SYS_E_FLAG, Bit 2 to remain at 0:

- CAL_SIGTR_LWR = CAL_DRVTN_LWR
- CAL_SIGTR_UPR = CAL_DRVTN_UPR
- CODE_SIGTR_LWR = CODE_DRVTN_LWR
- CODE_SIGTR_UPR = CODE_DRVTN_UPR

Signature CRC, Calibration Values, CAL_SIGTR_LWR

Table 182. CAL_SIGTR_LWR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x04, 0x05	Not applicable	R	Yes

Table 183. CAL_SIGTR_LWR Bit Definition

Bits	Description (No Default)
[15:0]	Factory programmed CRC value for the program code, low word

Signature CRC, Calibration Values, CAL_SIGTR_UPR

Table 184. CAL_SIGTR_UPR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x06, 0x07	Not applicable	R	Yes

Table 185. CAL_SIGTR_UPR Bit Definition

Bits	Description (No Default)
[15:0]	Factory programmed CRC value for the program code, high word

Derived CRC, Calibration Values, CAL_DRVTN_LWR

Table 186. CAL_DRVTN_LWR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x08, 0x09	Not applicable	R	No

Table 187. CAL_DRVTN_LWR Bit Definition

Bits	Description (No Default)
[15:0]	Calculated CRC value for the program code, low word

Derived CRC, Calibration Values, CAL_DRVTN_UPR

Table 188. CAL_DRVTN_UPR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x0A, 0x0B	Not applicable	R	No

Table 189. CAL_DRVTN_UPR Bit Definition

Bits	Description (No Default)
[15:0]	Calculated CRC value for the program code, high word

Signature CRC, Program Code, CODE_SIGTR_LWR

Table 190. CODE_SIGTR_LWR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x0C, 0x0D	Not applicable	R	Yes

Table 191. CODE_SIGTR_LWR Bit Definition

Bits	Description (No Default)
[15:0]	Factory programmed CRC value for the calibration coefficients, low word

Signature CRC, Program Code, CODE_SIGTR_UPR

Table 192. CODE_SIGTR_UPR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x0E, 0x0F	Not applicable	R	Yes

Table 193. CODE_SIGTR_UPR Bit Definition

Bits	Description (No Default)
[15:0]	Factory programmed CRC value for the calibration coefficients, high word

Derived CRC, Program Code, CODE_DRVTN_LWR

Table 194. CODE_DRVTN_LWR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x10, 0x11	Not applicable	R	No

Table 195. CODE_DRVTN_LWR Bit Definition

Bits	Description (No Default)
[15:0]	Calculated CRC value for the calibration coefficients, low word

Derived CRC, Program Code, CODE_DRVTN_UPR

Table 196. CODE_DRVTN_UPR Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x12, 0x13	Not applicable	R	No

Table 197. CODE_DRVTN_UPR Bit Definition

Bits	Description (No Default)
[15:0]	Calculated CRC value for the calibration coefficients, high word

Lot Specific Serial Number, SERIAL_NUM

Table 198. SERIAL_NUM Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x04	0x20, 0x21	Not applicable	R	Yes

Table 199. SERIAL_NUM Bit Definition

Bits	Description (No Default)
[15:0]	Lot specific serial number

FIR FILTERS

The ADIS16486 has four user configurable FIR filter banks. The sample rate of the FIR filter banks is identical to the IMU sample rate. Because decimation occurs after the FIR filters, the FIR sample rate is independent of the decimation rate and not affected by the setting of the DEC_RATE register. If the user selects the internally generated sample clock (which is the default setting), the nominal IMU sample rate (and FIR sample rate) is 2460 SPS. If the user supplies an external clock by setting Bit 7 to 1 of the FNCTIO_CRTL register (see Table 142 and Table 143), the FIR sample rate is the same frequency as the input synchronization clock provided to the ADIS16486.

The user can individually configure and select one of the four FIR filter banks for each individual inertial sensor using the FILTR_BNK_0 (see Table 155) and FILTR_BNK_1 (see Table 157) registers (see Figure 24). Each FIR filter bank (A, B, C, D) has 120 taps that consume two pages of memory. The coefficient associated with each tap in each filter bank has its own dedicated register that uses a 16-bit, twos complement format. The FIR filter has unity gain when the sum of all of the coefficients is equal to 32,768. For filter designs that require fewer than 120 taps, write 0x0000 to all unused registers to eliminate the latency associated with that particular tap.

FIR Filter Bank A, FIR_COEF_A000 to FIR_COEF_A119

Table 201 and Table 202 offer detailed register and bit definitions for FIR_COEF_A071, one of the FIR coefficient registers in Bank A (see Table 200).

Table 200. FIR Filter Bank A Memory Map

Page	Page ID	Address	Register
5	0x05	0x00	PAGE_ID
5	0x05	0x02 to 0x07	Not used
5	0x05	0x08	FIR_COEF_A000
5	0x05	0x0A	FIR_COEF_A001
5	0x05	0x0C to 0x7C	FIR_COEF_A002 to FIR_COEF_A058
5	0x05	0x7E	FIR_COEF_A059
6	0x06	0x00	PAGE_ID
6	0x06	0x02 to 0x07	Not used
6	0x06	0x08	FIR_COEF_A060
6	0x06	0x0A	FIR_COEF_A061
6	0x06	0x0C to 0x7C	FIR_COEF_A062 to FIR_COEF_A118
6	0x06	0x7E	FIR_COEF_A119

Table 201. FIR_COEF_A071 Register Definition

Page ID	Addresses	Default	Access	Flash Backup
0x06	0x1E, 0x1F	Not applicable	R/W	Yes

Table 202. FIR_COEF_A071 Bit Definition

Bits	Description (No Default)
[15:0]	FIR Bank A, Coefficient 71, twos complement

Use the following sequence to set the FIR_COEF_A071 register to a decimal value of −169 (0xFF57):

1. Select Page 6 (DIN = 0x8006).
2. Set FIR_COEF_A071, Bits[7:0] = 0x57 (DIN = 0x9E57).
3. Set FIR_COEF_A071, Bits[15:8] = 0xFF (DIN = 0x9FFF).

FIR Filter Bank B, FIR_COEF_B000 to FIR_COEF_B119

Table 203. Filter Bank B Memory Map

Page	Page ID	Address	Register
7	0x07	0x00	PAGE_ID
7	0x07	0x02 to 0x07	Not used
7	0x07	0x08	FIR_COEF_B000
7	0x07	0x0A	FIR_COEF_B001
7	0x07	0x0C to 0x7C	FIR_COEF_B002 to FIR_COEF_B058
7	0x07	0x7E	FIR_COEF_B059
8	0x08	0x00	PAGE_ID
8	0x08	0x02 to 0x07	Not used
8	0x08	0x08	FIR_COEF_B060
8	0x08	0x0A	FIR_COEF_B061
8	0x08	0x0C to 0x7C	FIR_COEF_B062 to FIR_COEF_B118
8	0x08	0x7E	FIR_COEF_B119

FIR Filter Bank C, FIR_COEF_C000 to FIR_COEF_C119

Table 204. Filter Bank C Memory Map

Page	Page ID	Address	Register
9	0x09	0x00	PAGE_ID
9	0x09	0x02 to 0x07	Not used
9	0x09	0x08	FIR_COEF_C000
9	0x09	0x0A	FIR_COEF_C001
9	0x09	0x0C to 0x7C	FIR_COEF_C002 to FIR_COEF_C058
9	0x09	0x7E	FIR_COEF_C059
10	0x0A	0x00	PAGE_ID
10	0x0A	0x02 to 0x07	Not used
10	0x0A	0x08	FIR_COEF_C060
10	0x0A	0x0A	FIR_COEF_C061
10	0x0A	0x0C to 0x7C	FIR_COEF_C062 to FIR_COEF_C118
10	0x0A	0x7E	FIR_COEF_C119

FIR Filter Bank D, FIR_COEF_D000 to FIR_COEF_D119

Table 205. Filter Bank D Memory Map

Page	Page ID	Address	Register
11	0x0B	0x00	PAGE_ID
11	0x0B	0x02 to 0x07	Not used
11	0x0B	0x08	FIR_COEF_D000
11	0x0B	0x0A	FIR_COEF_D001
11	0x0B	0x0C to 0x7C	FIR_COEF_D002 to FIR_COEF_D058
11	0x0B	0x7E	FIR_COEF_D059
12	0x0C	0x00	PAGE_ID
12	0x0C	0x02 to 0x07	Not used
12	0x0C	0x08	FIR_COEF_D060
12	0x0C	0x0A	FIR_COEF_D061
12	0x0C	0x0C to 0x7C	FIR_COEF_D062 to FIR_COEF_D118
12	0x0C	0x7E	FIR_COEF_D119

Default Filter Performance

The FIR filter banks have factory programmed filter designs. They are all low-pass filters that have unity dc gain. Table 206 provides a summary of each filter design, and Figure 30 shows the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

Table 206. FIR Filter Descriptions, Default Configuration

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
A	120	310
B	120	55
C	32	275
D	32	63

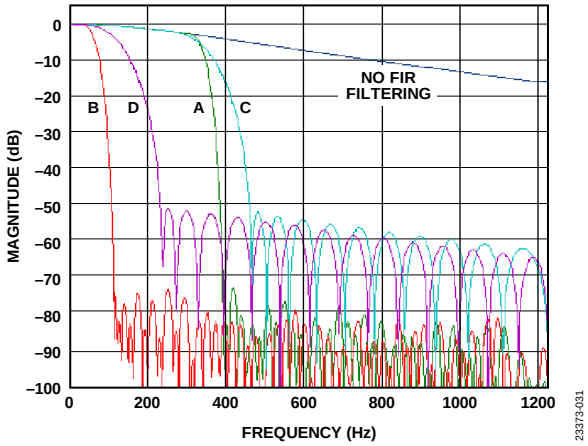


Figure 30. FIR Filter Frequency Response Curves

APPLICATIONS INFORMATION

MOUNTING BEST PRACTICES

For the best performance, follow these rules when installing the ADIS16486 into a system:

- Eliminate the opportunity for translational force (x-axis and y-axis direction, per Figure 18) application on the electrical connector.
- Isolate the mounting force to the four corners on the portion of the package surface that surrounds the mounting holes.
- Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch ounces (0.285 Nm).

These three rules help prevent irregular force profiles that can warp the package and introduce bias errors in the sensors. Figure 33 provides an example that leverages washers to set the package off the mounting surface and uses 2.85 mm passthrough holes and backside washers and nuts for attachment. Figure 31 and Figure 32 provide details for mounting hole and connector alignment pin drill locations.

For more information on mounting the ADIS16486, see the AN-1295 Application Note.

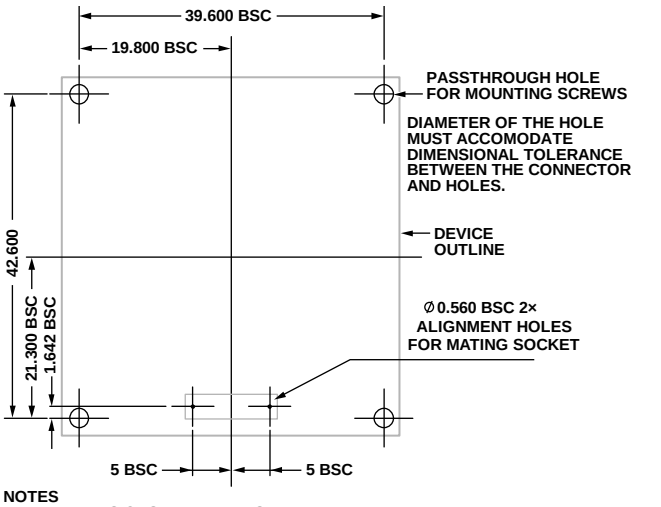


Figure 31. Suggested PCB Layout Pattern, Connector Down

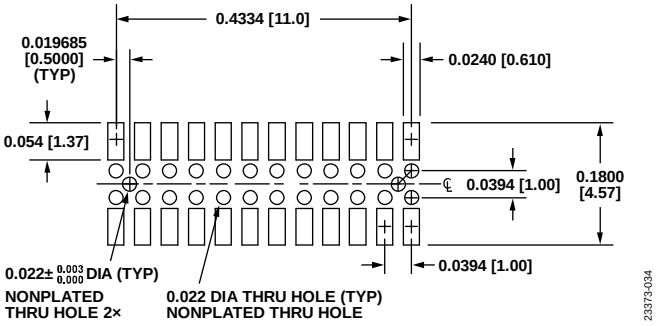


Figure 32. Suggested Layout and Mechanical Design When Using Samtec CLM-112-02-G-D-A for the Mating Connector

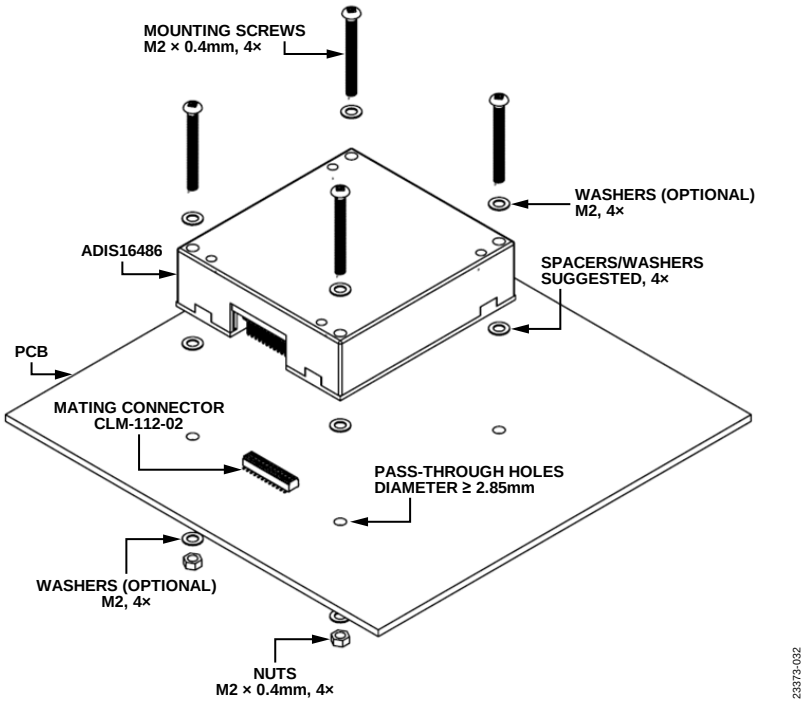


Figure 33. Mounting Example

EVALUATION TOOLS

Breakout Board, ADIS16IMU1/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16486, providing access to the ADIS16486 through larger connectors that support standard 1 mm ribbon cabling. This breakout board also provides four mounting holes for attaching the ADIS16486 to the breakout board. See the Ordering Guide for ordering details.

PC-Based Evaluation, EVAL-ADIS2

The EVAL-ADIS2 provides the system support PC-based evaluation of the ADIS16486.

POWER SUPPLY CONSIDERATIONS

The VDD power supply must charge 24 µF of capacitance (inside of the ADIS16486, across the VDD pins and GND pins) during the initial ramp and settling process of the power supply. When VDD reaches 2.85 V, the ADIS16486 begins its internal start-up process, which generates additional transient current demand. See Figure 34 for a typical current profile during the start-up process. The first peak in Figure 34 relates to charging the 24 µF capacitor bank, whereas the second peak (~360 ms after the first peak) relates to the initialization process of the ADIS16486. See Figure 35 for a close view of the current profile associated with the second peak in Figure 34.

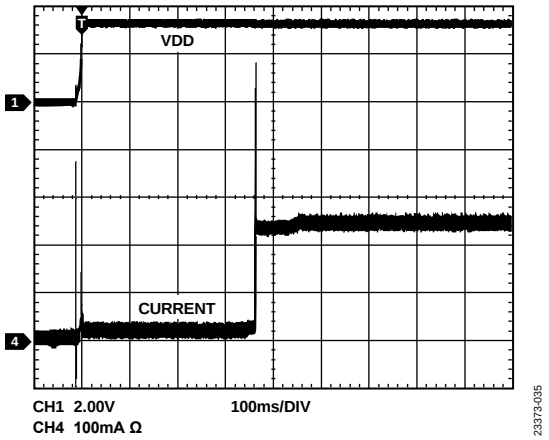


Figure 34. Transient Current Demand, Startup

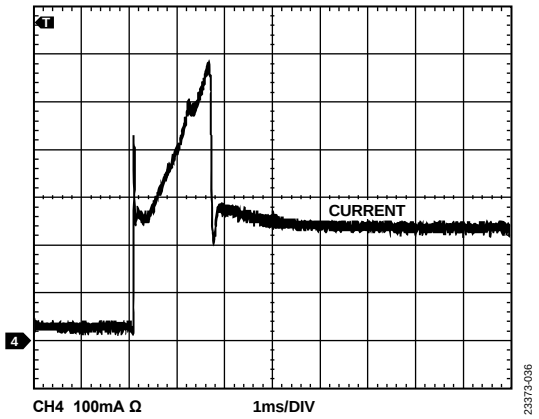


Figure 35. Transient Current Demand, Peak Demand

X-RAY SENSITIVITY

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, can affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16486 to this type of inspection.

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

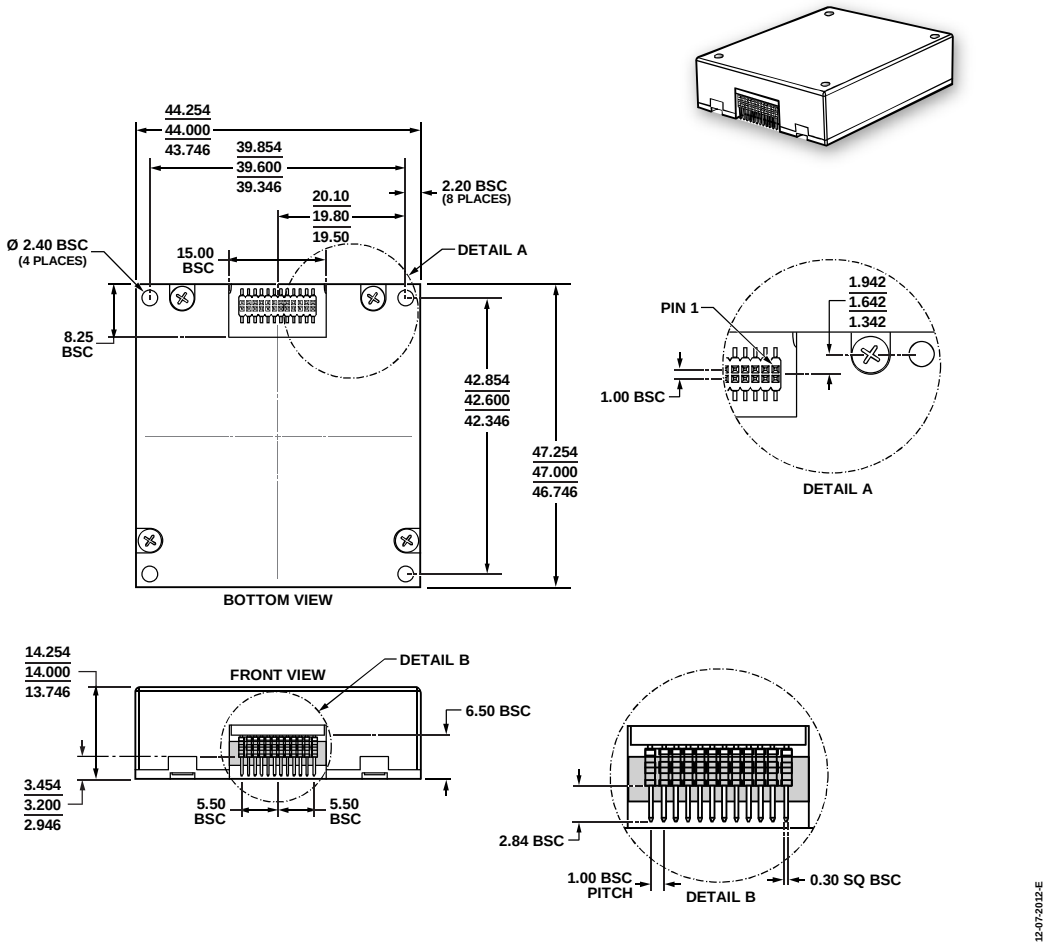


Figure 36. 24-Lead Module with Connector Interface [MODULE]
(ML-24-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16486BMLZ-P	−40°C to +105°C	24-Lead Module with Connector Interface [MODULE]	ML-24-6
ADIS16IMU1/PCBZ		Breakout Board	
EVAL-ADIS2Z		EVAL-ADIS2 Evaluation System	

[1] Z = RoHS Compliant Part.