ANALOG DEVICES

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APPLICATION NOTE

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Methodology for Narrow-Band Interface Design Between High Performance Differential Driver Amplifiers and ADCs

INTRODUCTION

The Analog Devices, Inc., broad portfolio of high performance differential amplifiers, including the ADL5561, ADL5562, AD8375, AD8376, and AD8352, are the amplifiers of choice for general-purpose IF and broadband applications where low distortion, noise, and power are critical. In addition to their wideband, low distortion performance, they offer gain adjust capability, making them ideally suited for driving analog-to-digital converters (ADCs).

By adopting a narrow band-pass antialiasing filter interface between the driver amplifier and the target ADC, the output noise of the amplifier outside the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves several dB when including a reasonable order antialiasing filter.

This application note provides a methodology to allow users to design a more effective interface between high performance driver amplifiers to ADCs, including those with switched-capacitor inputs. The narrow-band interface approach shown in this application note is optimized for driving some of Analog Devices popular unbuffered input ADCs, such as the AD9246, AD9640, and AD6655.

UNDERSTANDING THE INTERFACE COMPONENTS

The aim of the narrow-band interface is to offer band-pass filtering while providing adequate impedance transformation. Figure 1, Figure 2, and Figure 3 are block diagrams of the narrow-band approach to ADC interfacing for the various amplifiers. The four major components blocks—driver amplifier, low-pass filter, resonant match, and ADC—play critical roles in defining the interface, and each requires careful consideration. The requirements of each of the four are discussed in the following sections.

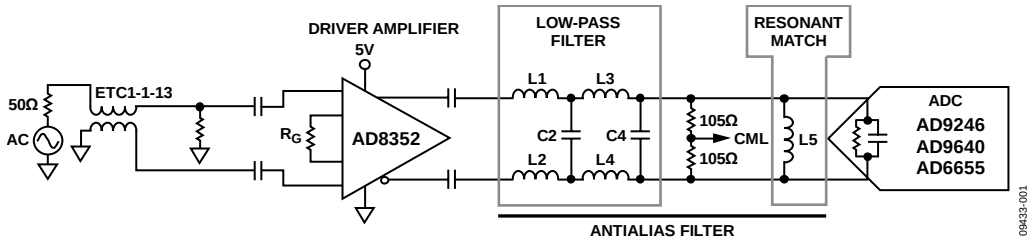

Figure 1. AD8352 Narrow-Band Solution for the ADC Interface

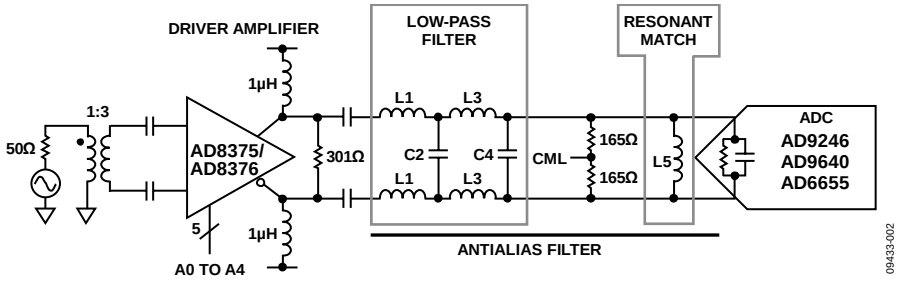

Figure 2. ADL8375 and ADL8376 Narrow-Band Solution for the ADC Interface

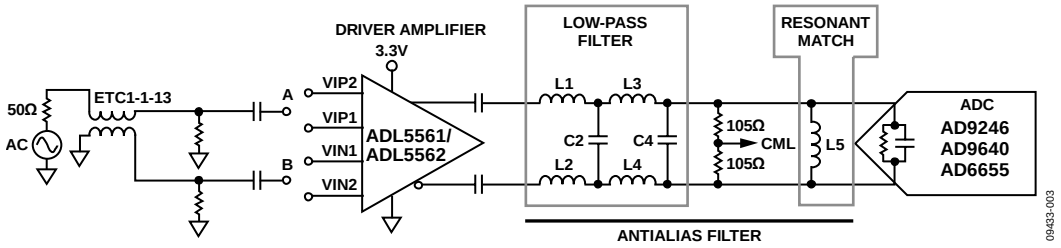

Figure 3. ADL5561 and ADL5562 Narrow-Band Solution for the ADC Interface

Table 1. Differential Amplifiers and Impedance Summary

Device	Gain Set Type	Input Impedance	Output Impedance	Optimal Load Impedance	RL/RS for Filter Design
AD8352	Resistive	3 kΩ	100 Ω || 3 pF	200 Ω	200/100 or 2:1
ADL5561	Pin-strappable	400 Ω, 200 Ω, or 133 Ω	12 Ω || 0.3 pF	200 Ω	200/50 or 4:1
ADL5562	Pin-strappable	400 Ω, 200 Ω, or 133 Ω	12 Ω || 0.3 pF	200 Ω	200/50 or 4:1
AD8375	Digital	150 Ω	16 kΩ || 0.8 pF	150 Ω	300/300 or 1:1
AD8376	Digital	150 Ω	16 kΩ || 0.8 pF	150 Ω	300/300 or 1:1

DIFFERENTIAL DRIVER AMPLIFIER

The broad portfolio of differential amplifiers, comprising the AD8352, AD8375, AD8376, ADL5561, and ADL5562, provides three basic types of gain control: resistor set gain, parallel digital control, and pin-strappable gain. Each of these gain control types has its own set of output impedance and desired impedance load for optimized performance, summarized in Table 1.

AD8352

The gain of the AD8352 is set using a gain setting resistor, R_G, which has buffers that isolate it from the signal inputs. As a result, the AD8352 maintains a constant 3 kΩ input resistance for gains of 3 dB to 25 dB, easing matching and input drive requirements. More details on adjusting the gain can be found in the AD8352 data sheet.

It is recommended that the input and output have ac coupling capacitors to isolate the VCC/2 bias from the source and balanced load.

The AD8352 has a nominal 100 Ω differential output resistance and achieves optimal ac performance with a load impedance equal to 200 Ω. This calls for an R_L/R_S filter ratio of 2:1, where R_S is the filter source impedance and R_L is the load impedance.

AD8375 and AD8376

The AD8375 is a single-channel, digitally controlled, variable gain amplifier, and the AD8376 is a dual channel version. Each channel is programmed by independent 5-bit binary codes that change each attenuator setting in 1 dB steps such that the gain of each amplifier channel changes from +20 dB (Code 0) to −4 dB (Code 24 and higher).

The AD8375 and AD8376 provide a 150 Ω input impedance and are tuned to drive a 150 Ω load impedance for optimal performance. The open-collector output structure requires dc bias through an external bias network. A set of 1 μH choke inductors is used on each channel output to provide bias to the open-collector output pins, which have a differential output impedance of 16 kΩ. Because the differential outputs are biased to the positive supply, they require ac-coupling capacitors, preferably 0.1 μF. Similarly, the input pins are at bias voltages of about 2 V above ground and should be ac-coupled as well.

Without any output matching, a tiny R_L/R_S filter ratio is likely to demand unrealistically large inductor values and extremely small capacitor values to make up the filter. The more drastic the impedance ratio, the more attention must be paid to component Q and layout parasitics. It is recommended that an antialiasing filter be terminated with shunt input and output resistances of about 300 Ω. In the example shown in Figure 2, the shunt resistances at either end of the filter, 301 Ω at the input and 330 Ω (through two 165 Ω bias setting resistors) at the output, combine to present the AD8375 or AD8376 with a nominal 150 Ω load impedance and produce a more benign R_L/R_S filter ratio of 1:1.

ADL5561 and ADL5562

The gain of the ADL5561 and ADL5562 is determined by the pin-strappable input configuration. When Input A is applied to VIP1 and Input B is applied to VIN1, the gain is 6 dB (minimum gain). When Input A is applied to VIP2 and Input B is applied to VIN2, the gain is 12 dB (middle gain). When Input A is applied to VIP1 and VIP2 and Input B is applied to VIN1 and VIN2, the gain is 15.5 dB (maximum gain). Note that the differential input impedance changes with the gain strapping selection: 400 Ω, 200 Ω, and 133 Ω for minimum, middle, and maximum gain settings, respectively. See the ADL5561 or ADL5562 data sheet for details on input matching.

It is recommended that the input and output have ac-coupling capacitors to isolate the VCC/2 bias from the source and balanced load.

The load should equal 200 Ω to provide the optimal ac performance. The differential output resistance of the ADL5561 and ADL5562 is 12 Ω. The greater the impedance ratio, the more attention must be paid to the component Q and layout parasitics. For ease of filter design, additional series padding of around 15 Ω can be added to each differential output to adopt a more benign R_L/R_S filter ratio of 4:1. Note that the added series elements attenuates the driver amplifier output.

ADC CHARACTERISTICS

High sampling rate analog-to-digital converters (ADCs) are commonly used to sample complex modulated signals at intermediate frequencies in modern wireless receiver designs. Often CMOS switched-capacitor based ADCs are selected for such designs due to their attractive low cost and power dissipation. These ADCs use an unbuffered front end directly coupled to the sampling network, which presents time varying input track-and-hold impedances to the amplifier driving the ADC. To effectively drive the ADC with minimal noise and distortion degradation of the wanted signal, it is necessary to design a passive network interface, which helps to reject wideband noise and transforms the track-and-hold impedance to present a more benign load impedance to the driving amplifier. A resonant approach for transforming the track-and-hold impedance to a more predictable load allowing precise design of antialiasing filters is recommended.

ANTIALIASING FILTER

The antialiasing filter comprises a fourth order Butterworth low-pass filter and a resonant tank circuit. The resonant tank helps ensure that the ADC input looks like a real resistance at the target center frequency by resonating out the capacitive portion of the ADC load (see the AN-742 and AN-827 Application Notes). The overall frequency response takes on a band-pass characteristic, helping to reject noise outside the intended Nyquist zone. In general, the SNR improves several dB by including a reasonable order antialiasing filter.

Low-Pass filter

Low pass filters used as antialiasing filters are often designed using LC networks and must have well-defined source and load impedances to achieve the desired stop band. To derive the filter network, a variety of cookbook filter synthesis approaches can be used. Often, Chebyshev or Butterworth polynomials are used to define the filter transfer function. Several software-based filter design programs are available to help simplify the problem, such as Filter Free 4.0 from Nuhertz Technologies or Agilent Technologies Advanced Design System (ADS).

Careful attention must be paid to the R_L/R_S filter ratio, where R_S is the filter sources impedance and R_L is the load impedance, and the filter order. A differential fourth-order Butterworth filter is recommended in this application note because increasing the order number results in unnecessary complexity with diminishing returns.

Resonant Match

The resonant match or tank circuit helps to ensure that the ADC input looks like a real resistance at the target center frequency (see the AN-742 and AN-827 Application Notes for more details). A shunt inductor, L5, works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by the last stage of the low-pass filter, C4, to form a resonant tank circuit.

The narrow frequency band of resonance of the tank circuit helps provide an overall band-pass frequency response to the antialiasing filter, helping to reject noise outside the intended Nyquist zone.

STEPS TO THE ANTIALIASING FILTER

Step One—Determine Interface Characteristics

The first step in this recommended methodology is to gather information about the requirements on all of the components that are involved in the ADC interface. The basic list of requirements to gather includes

- Filter specifications—requirements such as center frequency and bandwidth
- Antialiasing source and load impedances—defined as the differential driver output and the desired load for optimal performance (see Table 1)
- ADC (track mode) input impedance—S-parameters that are available in Excel format from the evaluation board section of the device website.

Step 2—Look Up Normalized Prototype Values

Filter design handbooks can be used to find unit normalized prototype filter values, which can then be scaled for the desired cutoff frequency and load impedance. Table 2 has some approximations for relevant prototype values.

Table 2. Fourth Order Butterworth Prototype Element Values

R_L/R_S	L1	C2	L3	C4
1	0.466	1.592	1.744	1.469
2	0.218	2.452	0.883	3.187
4	0.124	3.883	0.507	5.338

To compensate for the additional attenuation of the resonant tank match, the cutoff frequency should be 125% of the high end of the desired pass band. For example, if a filter with a 20 MHz bandwidth centered at 140 MHz is required, the cutoff frequency should be set to (140 MHz + 20 MHz ÷ 2.) × 125% = 188 MHz.

An example of a single-ended fourth-order unit normalized prototype filter is presented in Figure 4(a). The Butterworth filter shown provides flat response, with no ripple, for a 2:1 load-to-source impedance ratio.

Step 3—Scale Normalized Prototype Values by Frequency and Load

The single-ended unit normalized prototype filter values, C_n or L_n, can now be scaled to the desired cutoff frequency, f_{cut}, and load impedance, R. The transformation uses the following equations:

$$C = \frac{C_n}{2\pi \times f_{CUT} \times R}$$

$$L = \frac{RL_n}{2\pi \times f_{CUT}}$$

For a 188 MHz cutoff frequency and a 200 Ω load impedance, the single-ended equivalent network is presented in Figure 4(b).

Step 4—Convert Single-Ended Equivalent to Differential by Splitting Series Reactances

Most high speed ADCs capable of high dynamic range IF sampling use a differential input interface. Therefore, it is necessary to convert the single-ended network to a differential network, as shown in Figure 4(c). The series impedances are halved when transforming to the final differential network.

Step 5— Eliminate Raw Switched Capacitance at ADC Input

The shunt inductor in a resonant match or tank circuit helps to cancel out the on-chip ADC input capacitance (and any extra capacitance added beyond the last stage of the low-pass filter). An inductor value must be chosen to resonate away the imaginary admittance of the ADC, leaving only the conductive portion of the complex impedance. ω

$$\frac{1}{\omega(C_{ADC} + C_{EXTRA})} = \omega L$$

For example, the AD9640 differential input impedance is approximately 4.7 kΩ in parallel with 3.9 pF at 140 MHz.

$$\frac{1}{\omega(3.9\ pF)} = \omega L$$

Therefore, the required inductance, L, is 331 nH.

Note that the L/C ratio is one of the factors that determine the Q and the selectivity. For a parallel resonant circuit, the higher the inductance and the lower the capacitance, the broader the pass-band filter bandwidth. To achieve a more narrow-band response, a higher Q can be achieved by adding extra capacitance in parallel (in addition to the last capacitance stage of the low pass Butterworth filter). In the following equation, an additional 10 pF is added, reducing the required inductance, L, to 93 nH:

$$\frac{1}{\omega(3.9\ pF + 10\ pF)} = \omega L$$

Consequently, the Q is reduced, and the response bandwidth is also decreased.

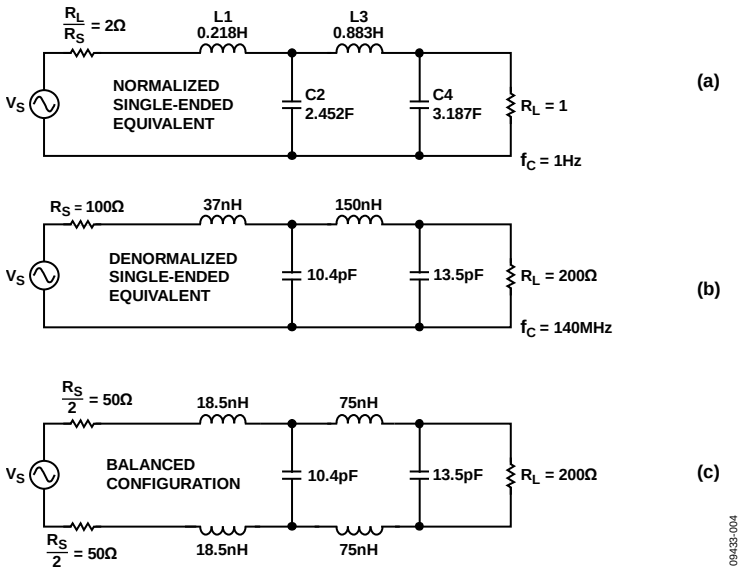

Figure 4. Prototype Filter Design Steps

Step 6—Putting It All Together

After the individual interface components have been calculated, the circuit can be brought together for simulation. Often, some simulation trial and error is needed to optimize the network interface for the best combination of filter requirements. It is advantageous to simulate the network response using realistic component models (s-parameters) that accurately capture the parasitic effects of real-world Ls and Cs.

The implementation using ideal L values and C values is shown in Figure 7. Note that the final implementation is likely to use slightly lower inductor values to accommodate for the series inductance of the circuit traces. Note also that the load in Figure 4(c) is replaced with the ADC interface in Figure 7, including a shunt inductor extra capacitance, and common-mode biasing resistors. The biasing resistors supply the needed DC offset into the individual differential inputs and work in combination with the raw track impedance and resonant shunt inductor to present a well-defined load for the filter.

Step 7—Board Level Empirical Tuning

The final implementation using realistic L values and C values is shown in Figure 8. After the board is populated with the final simulated values, some board level empirical optimization may be needed to help compensate for actual PCB parasitics.

It is for this reason that detailed simulation earlier in the process using good software and s-parameters is advised. In this way, the more time consuming board level tuning effort is lessened. In some instances, it may be necessary to model the printed circuit board parasitics to select optimum Ls and Cs.

Figure 5 and Figure 6 show the performance of the interface between the AD8352 and the AD9640.

LAYOUT CONSIDERATIONS

Minimizing of stray board parasitics is critical, in particular, where filter component values are small and additional parasitics result in substantial proportional changes. Excellent layout, grounding, and decoupling techniques must be used to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers. See each device driver amplifier and ADC data sheet for specific board recommendations.

REFERENCES

- *RF Circuit Design,* Chris Bowick, Page 66 to Page 97.
- AN-742 Application Note, *Frequency Response of Switched-Capacitor ADCs.*
- AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs.*

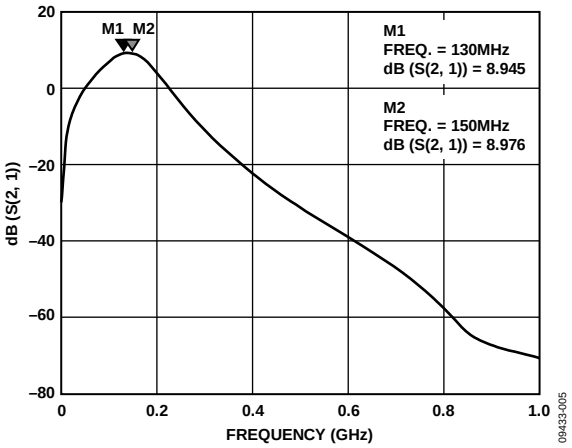

Figure 5. Filter Response of the Interfacing Example Featuring the AD8352 and the AD9640

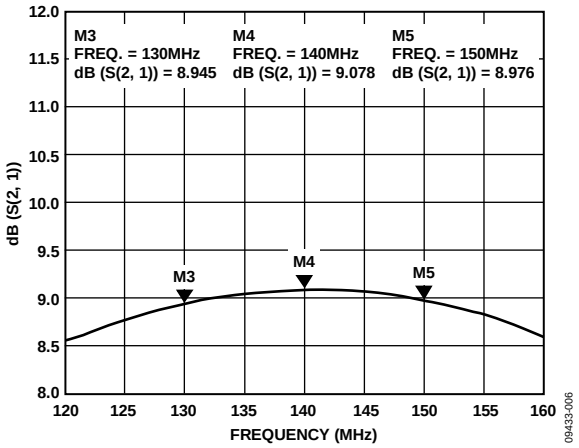

Figure 6. Pass-Band Flatness of the Interfacing Example Featuring the AD8352 and the AD9640

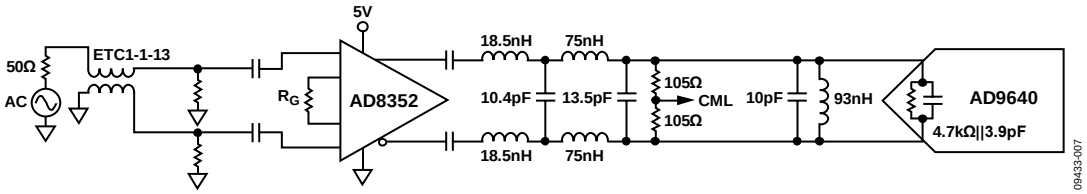

Figure 7. ADC Interfacing Example Featuring the AD8352 and the AD9640, Ideal Components

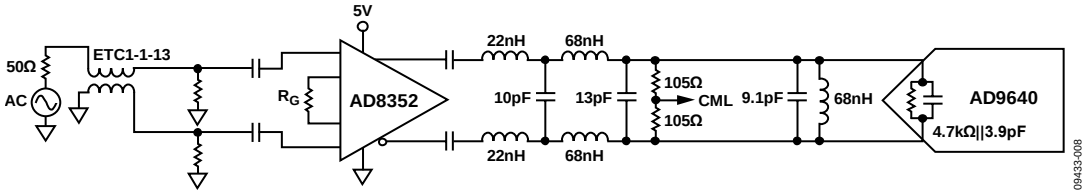

Figure 8. ADC Interfacing Example Featuring the AD8352 and the AD9640, Real Components

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