Hot Swap and Blocking FET Controller 2 × ADM1073 Hot Swap Controllers
by Alan Moloney

INTRODUCTION

In many −48 V hot swap systems, there is a blocking diode in series with the hot swapping FET. This component ensures that current can only flow into the load in one direction, preventing damage to the board in the case of reverse currents flowing. Figure 1 shows this implementation in an ADM1073 controlled system.

This solution can have serious power dissipation implications during normal operation due to the voltage drop across the blocking diode

$$P_{LOSS} = P_{FET} + P_{DIODE} + P_{QUIESCENT}$$

where:

$P_{DIODE} = (Load\ Current) \times (Diode\ Voltage\ Drop)$

Note that P_{DIODE} is responsible for a substantial portion of the total power loss (see Figure 1).

This is especially evident in applications where the average load current level is high and the total power losses are calculated across an entire system, which may consist of multiple racks of boards.
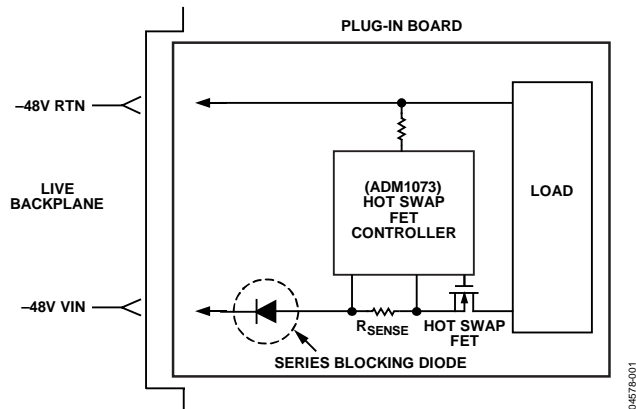

Figure 1. Blocking Diode in Series with Hot Swap FET

ALTERNATIVE SOLUTION

This application note focuses on another solution for systems where this power loss is unacceptable. The alternative solution is to replace the blocking diode with a blocking FET that has a low on resistance. A second ADM1073 can control this blocking FET. Figure 2 shows this solution on a plug-in board.

This solution reduces the power dissipation during operation to

$$P_{LOSS} = P_{HSWAP-FET} + P_{BLK-FET} + P_{QUIESCENT}$$

where:

$P_{BLK-FET} = (Load\ Current)^2 \times (FET\ On\ Resistance)$

Note that $P_{BLK-FET}$ is much smaller than P_{DIODE} and therefore reduces the total power loss significantly.

The ADM1073 data sheet should be consulted in conjunction with this application note.
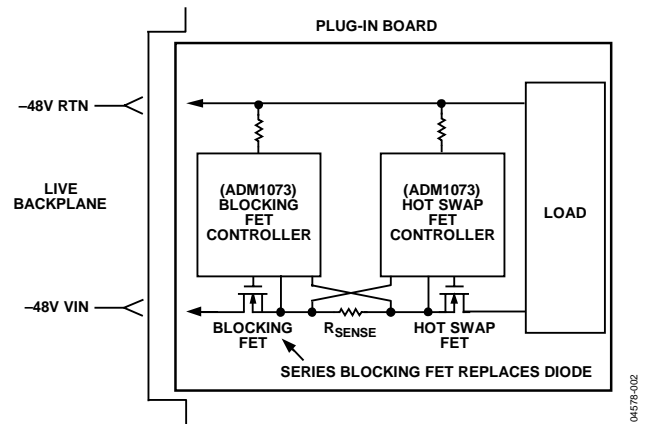

Figure 2. Alternative Solution—Blocking FET Replaces Diode

TABLE OF CONTENTS

REVISION HISTORY

5/13—Rev. 0 to Rev. A

Changes to Figure 3 and Example Configuration for
ADM1073 (A) Section 3
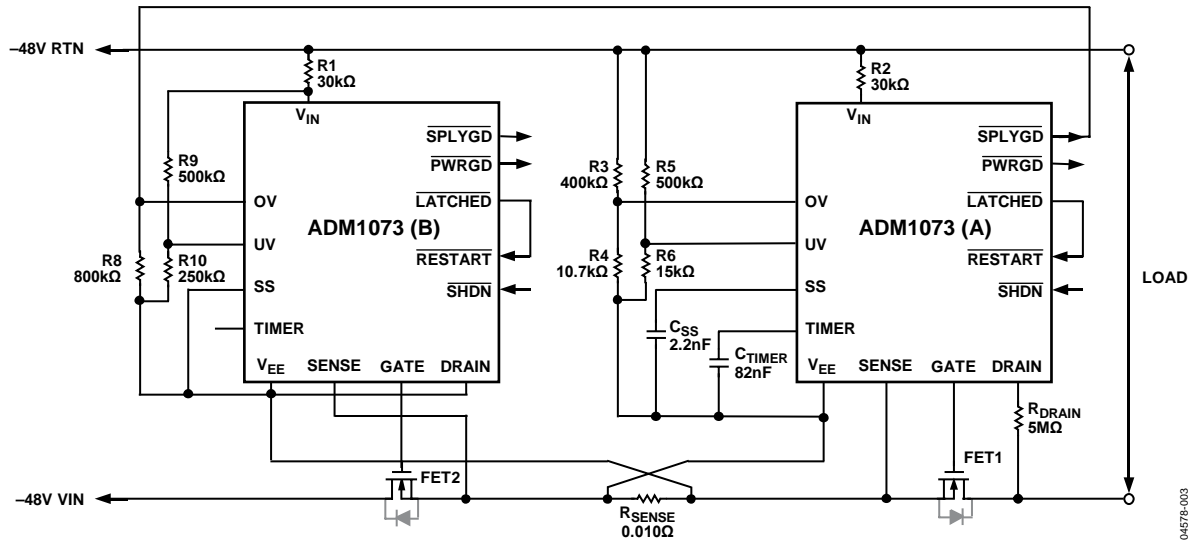
11/03—Revision 0: Initial Version

Figure 3. Full Implementation of Dual ADM1073 Solution for Blocking FET and Hot Swap FET Control

DETAILED DESCRIPTION

Figure 3 shows a full implementation of a dual ADM1073 solution for a blocking FET and hot swap FET control.

FET1 is the hot swap FET. This device must also have a low on resistance and a high reverse voltage capability. This device is required to dissipate high power during startup, so a D2PAK device may be required. ADM1073 (A) is the hot swap FET controller that controls FET1.

FET2 is the blocking FET. This device must have low on resistance to minimize power dissipation and a high reverse voltage capability. This device does not have to dissipate as much power so a smaller package may be suitable (for example, SOIC). ADM1073 (B) is the blocking FET controller that controls FET2.

A single sense element, R_{SENSE}, can be used for both ADM1073 devices. With this method, the ADM1073 (A) limits forward load current to 100 mV/R_{SENSE}; the ADM1073 (B) limits reverse load current to 18 mV/100 mV.

Example Configuration for ADM1073 (A)

The undervoltage level is set by R5 and R6. R5 is 500 kΩ; R6 is 15 kΩ. R6 normally gives a UV rising threshold of 32.3 V and a UV falling threshold of 29.8 V. In this case, the UV rising level is actually 32.9 V + FET1 body diode voltage drop (~1 V) and UV falling level will be 29.8 V + I²R of FET2.

The overvoltage level is set by R3 and R4. R3 is 400 kΩ; R4 is 10.7 kΩ. R4 normally gives an OV rising threshold of 74.08 V and an OV falling threshold of 72.08 V. In this case, the OV falling level is actually 72.08 V + FET2 body diode voltage drop (~1 V) and the OV rising level is 74.08 V + I²R of FET1.

The soft start time is set by C_{SS}. C_{SS} = 2.2 nF ≥ t_{SS} = 0.9 ms.

TIMER is selected by the C_{TIMER} capacitor, for example, C_{TIMER} = 82 nF gives a maximum TIMER of 5.8 ms at −48 V.

The drain fold back (for FET SOA protection) is set with R_{DRAIN}. A 5 MΩ resistor is sufficient to charge a 470 µF load.

The R2 dropper resistor is set to 30 kΩ for normal operation.

The $\overline{LATCHED}$ output is tied back to the $\overline{RESTART}$ input to give a continuous retry with a 5 second cooling off period under short-circuit condition.

The $\overline{SHDN}$ input is used as the start-up control if it is required.

The $\overline{PWRGD}$ output is used as a hot swap completion flag, which is required.

The $\overline{SPLYGD}$ output is connected to the OV pin of the ADM1073 (B) to provide a start-up signal to the ADM1073 (B) based on the voltage detection in the ADM1073 (A).

Example Configuration for ADM1073 (B)

The SENSE and V_{EE} pins connect across the ADM1073 (A) sense resistor with connections reversed, that is, the ADM1073 (B) SENSE pin is connected to the ADM1073 (A) V_{EE} pin and the ADM1073 (B) V_{EE} pin is connected to the ADM1073 (A) SENSE pin. This configures the ADM1073 (B) to regulate current in FET2 only if it sees a reverse current flowing in the sense resistor.

The undervoltage (UV) pin is tied to a resistor divider from the V_{IN} pin. Choose the resistor values so that the voltage on the UV pin is always above the UV threshold, for example, R9 = 500 kΩ; R10 = 250 kΩ ≥ V_{UV} = 4 V.

The overvoltage (OV) pin is connected to the $\overline{SPLYGD}$ output of the ADM1073 (A) so that startup of the ADM1073 (B) is controlled by the ADM1073 (A). A resistor to V_{EE} on this pin ensures that the voltage on the OV pin does not exceed 5 V when the supply of the chip on the ADM1073 (A) is high (for example, R8 = 800 kΩ ≥ OV = 4 V when high plus pull-up from OV hysteresis, which brings it up to V_{CC} of ADM1073 (B) but not above this).

The soft start (SS) pin is tied to V_{EE}. This fixes the reverse current control level at 18 mV, as opposed to up to 97.5 mV default. This limits the maximum reverse current to approximately $1/6^{th}$ of the forward inrush current limit.

The TIMER pin is left open. If reverse current is detected, it will current limit at 18 mV/R_{SENSE} for only a few microseconds plus the time taken to charge the gate up to V_{GSTH} of the FET (the retry duty cycle should be less than 10%). This then retries seven times and then shuts off, which should take no more than ~0.5 ms.

The DRAIN pin is unused and should be tied to V_{EE}.

The R1 dropper resistor is set to 30 kΩ for normal operation.

The $\overline{\text{LATCHED}}$ output is tied back to the $\overline{\text{RESTART}}$ input. If reverse current saturation persists for more than 0.5 ms, the blocking FET shuts off completely and then retries after 5 seconds (for example, if the input voltage is shorted for 100 ms, a small average reverse current would flow for 0.5 ms. The FET would switch off 5 seconds after the supply was good again, and the FET would turn back on and shunt the diode current).

The $\overline{\text{SHDN}}$ function is unused; leave the $\overline{\text{SHDN}}$ pin disconnected.

The $\overline{\text{PWRGD}}$ function is unused; leave the $\overline{\text{PWRGD}}$ pin disconnected.

The $\overline{\text{SPLYGD}}$ function is unused; leave the $\overline{\text{SPLYGD}}$ pin disconnected.

Example Comparison for Power Dissipation Using Both Methods

Assumptions:

I_{LOAD} = 5 A

R_{ONFET} = 10 mΩ

V_{DIODE} = 1 V

Standard Diode Solution

Standard configuration using hot swap FET and blocking diode:

Input lower = 96 W

Hot swap power loss = $P_{FET} + P_{DIODE} + P_{QUIESCENT}$

= $(5 \times 5 \times 0.01) + (5 \times 1) + (48 \times 0.0026)$

= 5.37 W

(= 5.6% power loss)

Dual ADM1073 Solution

New configuration using hot swap FET and blocking FET:

Input power = 96 W

Hot swap power loss = $P_{HSWAP-FET} + P_{BLK-FET} + P_{QUIESCENT}$

= $(5 \times 5 \times 0.01) + (5 \times 5 \times 0.01) + (48 \times 0.0026)$

= 0.62 W

(= 0.65% total power loss)

Table 1. Results Based on Example Configurations

Solution	Power Loss	Percentage Loss
Standard Diode Solution	5.37 W	5.6%
Dual ADM1073 Solution	0.62 W	0.65%

ANALOG DEVICES

www.analog.com