ADM1278 Hotswap Controller Design Guide

1. System Specifications

The following conditions are assumed for this example:

- Controller = ADM1278
- V_{IN} = 12 V Nominal
- V_{MAX} = 12.6 V
- I_{TRIP} = ~70 A
- C_{LOAD} = 3000 µF
- T_{AMAX} = 60°C
- $R_{POWERUP}$ = 1kΩ (static load resistance during system power up)
- MOSFET = PH0925CL

To simplify this example, the calculations exclude the effects of component tolerances. These tolerances should of course be considered when designing for worst-case conditions. Note also there may be slight differences in the numbers quoted here compared to the design tool. In this case the tool takes precedence.

2. UV Pin Threshold

The UV falling threshold is detected by an internal comparator with a 1V reference.

$$UV_{FALLING} = \frac{RUV1 + RUV2}{RUV2} \times 1V$$

Therefore for a 9.3V UV falling threshold, if RUV1 = 49.9kΩ, then RUV2 = 6.04kΩ

The UV pin has 50mV of hysteresis, therefore for the same resistor string, the UV rising threshold will be 9.72V

A decoupling cap can also be added to the UV resistor divider if required. This will extend the UV glitch filtering.

Summary of the key component selection for this section:
$R_{UV(TOP)}$ = 49.9 KΩ
$R_{UV(BOT)}$ = 6.04 KΩ
C_{UV} = 10 nF

3. OV Pin Threshold

The OV rising threshold is detected by an internal comparator with a 1V reference.

$$OV_{RISING} = \frac{ROV1 + ROV2}{ROV2} \times 1V$$

Therefore for a 16.0V OV rising threshold, if ROV1 = 49.9kΩ then ROV2 = 3.32kΩ

The OV pin has 60mV of hysteresis, therefore for the same resistor string, the OV falling threshold will be 15.1V

A decoupling cap can also be added to the OV resistor divider if required. This will extend the OV glitch filtering.

Summary of the key component selection for this section:
$R_{OV(TOP)}$ = 49.9 KΩ
$R_{OV(BOT)}$ = 3.32 KΩ
C_{OV} = 10 nF

4. Sense Resistor Selection

The sense resistor selection is primarily based on the required circuit breaker trip current. However, the ADM1278 has an adjustable current limit threshold which allows for fine tuning of the current limit beyond that provided by the limited availability of standard sense resistor values. The sense voltage can be programmed within a 5 to 25mV range. Such a low sense voltage, along with the flexibility of programmability, offers reduced power loss and size in sense resistor selection.

Using the default 20mV threshold we determine what order of magnitude the sense resistor needs to be. The programmed sense voltage (using ISET pin) refers to the current regulation point. However, the circuit breaker timer (current fault glitch filter) begins typically 0.8mV below this. This means that to set a trip point of 69A (19.2mV) we need to set the regulation point to ~73A (20mV).

$$R_{SENSE} = \frac{V_{SENSE}}{I_{TRIP}} = \frac{0.020\,\text{V}}{73\,\text{A}} \approx 0.273m\Omega$$

This is not a common available value so the closest to consider is 0.25mΩ with either **2x 0.5mΩ** or **4x 1mΩ**. To reduce space we will opt

for only two resistors. Let's reverse the equation above to determine the required sense voltage.

$$V_{SENSE} = R_{SENSE} \times I_{TRIP}$$
$$= 0.25m\Omega \times 73 \approx 18.25mV$$

If you were to require the default 20mV limit then ISET pin can be connected to the VCAP pin. Alternatively the ISET pin can be programmed to a desired voltage using a divider from the VCAP reference. This will set a desired Vsense trip voltage above or below 20mV to match commonly available sense resistors.

Note: ISET voltage = Vsense x 50. The range of 15mV to 25mV is recommended for optimum accuracy.

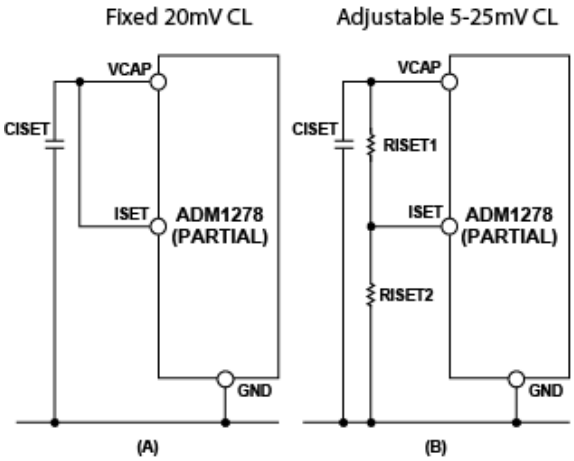

Figure 1. ISET Current Limit

As the VCAP node has a limited load current spec we will keep the top resistor relatively large, e.g. 41.2KΩ. To provide a sense voltage limit of 18.25mV we use the following equation:

$$V_{ISET} = V_{SENSE} \times 50 = 18.25mV \times 50 = 0.912V$$

Using the 2.7V VCAP reference, and assuming RISET1= 41.2KΩ, this will result in a bottom resistor of 21.2KΩ. A decoupling capacitor can also be added to the ISET resistor divider string.

Now let's check where the current limits are:

As mentioned before, there are two important sense voltage levels to be familiar with around the programmed Vsense voltage:

- **Vsensereg = 18.25mV**

  (value programmed by ISET)

- **Vsensecb = 17.4mV**

  (Vsensereg - V_{CBOS}, = 18.25mV – 0.88mV)

Vsensereg, represents at what sense voltage the controller will regulate the load current. When including tolerances, the maximum of this voltage determines the maximum current allowed by controller when in current limit. This is used in MOSFET SOA verification.

Vsensecb, represents the circuit breaker trip voltage. If you were to include tolerances, the minimum of this determines the DC current that could be allowed before the circuit breaker trips. Systems should never require more than this current for DC. While the maximum determines the maximum DC current that could be allowed before the circuit breaker trips. This is used to verify thermal design limits.

So based on these three parameters the following current limits can be assumed:

- I_{REG} = 73A
- I_{CB} = 70 A

Including all component tolerances, and assuming +/- 1% sense resistor, the ADM1278 can offer tight tolerances on the current limit ranging from +/-5% at 20mV.

Power Rating:

To determine the power rating of the sense resistors first we must determine the maximum DC current in each resistor. If we were to calculate the total worst case DC was 71A, then each resistor will run ~39A each (including imbalance margin of ~10%). Therefore power can be calculated as:

$$P_{RSENSE} = I_{TRIP}^{2} \times R_{SENSE}$$
$$= (39\ A)^2 \times 0.0005\ \Omega$$
$$=\sim 0.76\ W$$

So each sense resistor should be capable of dissipating >1 W (including temperature derating factors). A 2W or 3W resistor is recommended.

When using multiple sense resistors a Kelvin footprint (4-pad layout) should be used to achieve best accuracy. This can be done even with standard 2-pad sense resistors. Series 10Ω resistors should be used to average all these nodes together to the controller.

Summary of the key component selection for this section:
$R_{ISET(TOP)}$ = 41.2 KΩ
$R_{ISET(BOT)}$ = 21.2 KΩ
C_{ISET} = 10 nF

R_{SENSEx} = 0.5mΩ x2 (2 / 3W)
R_{AVGx} = 10Ω x4

5. MOSFET Selection

The first consideration as criteria for selection of a suitable MOSFET is the R_{DSON} specification, to ensure that minimum power is lost in the MOSFET when it is fully enhanced in normal operation.

The ADM1278 features a high voltage gate drive to ensure a minimum of 10V V_{GS} is achieved to maintain the lowest specified R_{DSON}. The gate drive circuit is designed to achieve this while still ensuring the 20V maximum V_{GS} spec is not violated.

As the temperature of the MOSFET increases, its power rating is reduced, or *derated*. The R_{DSON} spec determines the maximum junction temperature of the MOSFET and therefore the required derating can be applied to SOA parameters. In addition, running MOSFETs at high temperatures may decrease their reliability.

Let's begin by estimating the required R_{DSON}. Recall the maximum DC current was 75A, worst case. Then using the maximum ambient temperature specified in section 1 we can estimate the power loss in the MOSFET(s). First we make a few assumptions…

- R_{thJA} = 40 C/W (must not exceed)
- T_{jMAX} = 120 °C

  (This is the maximum preferred junction temp, keeping well away from any silicon limits)

Calculate the junction temperature rise:

$$T_{RISE} = T_{jMAX} - T_{AMAX} = 120 - 60 = 60^{\circ}C$$

Then the power for a single FET:

$$P_{MOSFET} = \frac{T_{RISE}}{R_{thJA}} = \frac{60}{40} = 1.5W$$

Now total R_{DSON}:

$$R_{DSON} = \frac{P_{MOSFET}}{I_{MAXDC}^{\ 2}} = \frac{1.5}{75^2} = 0.266m\Omega$$

This number is far too small for a single FET so let's try 3 FETs in parallel:

$$R_{DSON} = \frac{P_{MOSFET}}{(I_{MAXDC}/3)^2} = \frac{1.5}{25^2} = 2.4m\Omega$$

Now we reduce this by 10% to give us some margin for imbalance due to layout asymmetry and a further 1.4 factor to allow some derate:

$$R_{DSON} = \frac{2.4 \times 0.9}{1.4} = 1.5m\Omega$$

Taking this as our target R_{SDON} we can now search for suitable candidates. The search can be narrowed to FETs that fit the following profile:

- V_{DS} = 25/30V (20V may be possible but not preferred)
- V_{GS} = 20V
- $R_{DSON} \leq 1.4m\Omega$

After selecting a suitable MOSFET, the derating of the R_{DSON} should be quantified using the MOSFET datasheet graph of R_{DSON} against T_J.

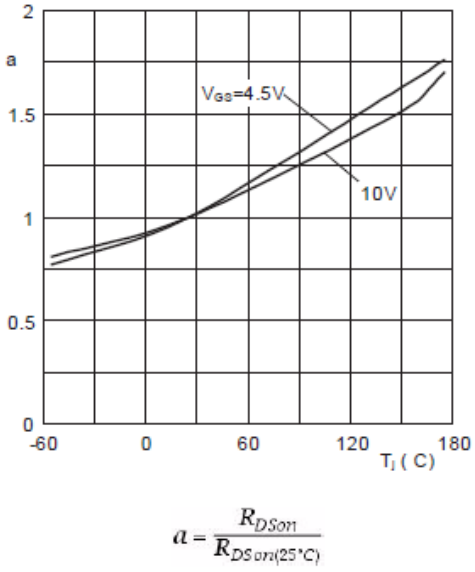

Figure 2. Normalised R_{DSON} vs T_J

Using T_{jMAX} of 120 °C, we can see the R_{DSON} increases by a factor of 1.4 to about 1.4mΩ(assuming 1mΩ at 25°C) at 120°C. As a rule it is best to keep junction temp ≤120C.

Assuming that the MOSFET's max R_{DSON} is 1.4mΩ, the power of each FET can be determined by:

$$P_{MOSFET} = \left(\frac{I_{MAXDC}}{n} + 10\% \right)^2 \times R_{DSON}$$
$$= (27.5\,\text{A})^2 \times 0.0014\,\Omega$$
$$\approx 1.06\text{W}$$

The MOSFET's thermal resistance at ambient temperature should be specified in the datasheet. The footprint size, airflow, nearby heat sources and additional copper will also have an effect on this value so care must be taken to ensure the specified conditions are met. Assume, for this design a target of:

$$R_{thJA} = 40^{\circ}\text{C/W}$$

(Note: Care should be taken with layout/airflow to ensure this figure is not exceeded)

As the MOSFET is expected to dissipate ~1.06W, a worst-case temperature rise of 42.4 °C above ambient can be expected as follows:

$$T_{RISE} = R_{thJA} \times P_{MOSFET} = 42.4^{\circ}\text{C}$$

The resulting junction temp of the FET can be determined as follows:

$$T_J = T_A + T_{RISE} = 60 + 42.4 = 102.4^{\circ}\text{C}$$

As this is below the maximum selected value of 120°C, the risk of thermal runway is avoided. When using multiple MOSFETs in parallel, a 10Ω resistor should be use in series with the gate of each MOSFET to prevent oscillations.

Summary of the key spec / component selection for this section:

Q_X	= Selected 1.0mΩ MOSFET (e.g. PH0925CL).
R_{thJA}	= 40 K/W (or 40 C/W)
R_{GATE}	= 10Ω (x3)

6. Power Derating Factor

Now that the maximum junction temperature is verified we can determine the maximum derate factor. This number will be used to derate all the SOA parameters to verify a robust solution across temperature.

Remember we determined the max expected T_j =102.4°C. From the datasheet we can see the max allowed T_j =175°C. If we look at the SOA curve we see that a condition of the data on this curve is that T_C =25°C (case temperature). In order to do a proper derating we need to determine the case temp when the T_j =102.4°C. From the datasheet let's assume the Thermal resistance from J-C is 1 K/W. Therefore, the max expected case temp is:

$$T_C = T_j - (R_{thJC} \times P_{MOSFET})$$
$$T_C = 102.4 - (1.0 \times 1.06) = 101.3^{\circ}C$$

Now the derating factor can be calculated as follows:

$$DF = \frac{T_{J\,\max} - T_{CSOA}}{T_{J\,\max} - T_{C\,\max}} = \frac{175°\text{C} - 25°\text{C}}{175°\text{C} - 101.3°\text{C}} = 2.0$$

Summary of the key spec / component selection for this section:

DF = 2.0

7. Foldback

The ADM1278 utilizes a foldback technique to protect the MOSFETs in the event of overcurrent faults or short circuits. The MOSFET V_{DS} voltage is monitored and the current limit is adjusted based on the V_{DS} of the MOSFET to maintain a constant power limit in the MOSFET. An example of this relationship can be seen in Figure 3.

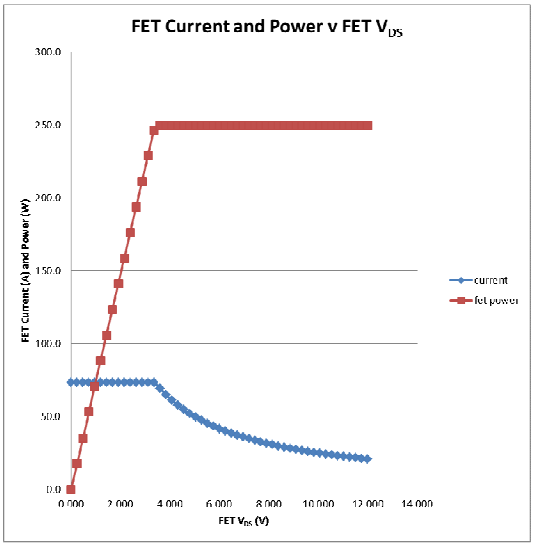

Figure 3. Constant Power

When the output voltage is at zero, there is a lower limit clamp to prevent the current limit approaching zero. This clamp is fixed at ~2mV Vsense, which equates to ~8A on this particular

design. The lower clamp level is not reached in this design. As the output voltage increases (and therefore the MOSFET V_{DS} voltage reduces), the current limit ramps as a function of the MOSFET V_{DS} voltage. The constant power level set by the PSET pin is always maintained as a maximum. Then we see a plateau in FET current as the MOSFET V_{DS} voltage reduces below 4V. This is where we hit the current limit set by the ISET pin. The current cannot increase any further so the MOSFET power drops off until the load capacitance is fully charged.

In this design, the chosen FET is able to handle >500W for 1ms. With a derate factor of 2, the constant power level needs to be set at 250W or lower. Using the formula below, the PSET resistor values can be selected.

$$FETPowerLimit = \frac{(V_{PSET} \times 8)}{(50 \times R_{SENSE})}$$

$$\Rightarrow V_{PSET} = \frac{250W \times 50 \times 0.25m\Omega}{8} = 0.39V$$

Targeting 0.39V, a suitable resistor divider would be 100KΩ top and 16.9KΩ bottom.

The ADM1278 is capable of powering up in constant power mode. However, due to the large load capacitance in server designs and the slow ramp required on VOUT, it is preferential to power up in dv/dt mode (see "Powerup analysis" section). In this case the constant power feature will not be used during a normal power up event as dv/dt effectively trickle charges the load capacitance, keeping below the active current limit. The constant power foldback will always be active and will help protect the MOSFET in the case of a fault or short circuit event.

Summary of the key spec / component selection for this section:

V_{PSET}	= 0.39V
R_{PSET1}	= 100 KΩ
R_{PSET2}	= 16.9 KΩ
C_{PSET}	= 10 nF

8. PWRGD threshold

The PWRGD pin is an open drain output pin and will be pulled low if:

a) there is a fault condition that hasn't been cleared, or
b) the controller hasn't signaled that the hotswap can be enabled, or
c) the power-good input threshold hasn't been exceeded.

The power-good input threshold is set by a resistor divider on the PWGIN pin.

$$PWGIN_{FALLING} = \frac{RPWGIN1 + RPWGIN2}{RPWGIN2} \times 1V$$

Therefore for a 10.3V PWGIN falling threshold, if RPWGIN1 = 49.9kΩ then RPWGIN2 = 5.36kΩ

The PWGIN pin has 50mV of hysteresis, therefore for the same resistor string, the PWGIN rising threshold will be 10.8V

9. MOSFET SOA Analysis – Short Circuit

The next step is to review the SOA curve on the MOSFET datasheet to determine how much time it can tolerate the worst case power in the FET. This will determine a suitable timer capacitor value.
In a multiple FET solution, it must be assumed that a single FET could be dissipating 100% of the power during a powerup or event such as this. This is due to possible differing Vth levels on each FET, only one could be conducting when in regulation.

The ADM1278 has a very fast overcurrent detect circuit which detects a severe overcurrent event and responds in <300ns. There is also a very large gate pulldown device to ensure large MOSFETs are shutdown fast. These combined should ensure sub 1µs shutdown (excluding any system specific components which may slow down di/dt). The controller will re-establish control and begin controlled current fault timing.

If a short was applied the V_{DS} of the FET can be assumed to be ~12.6V (assuming source at GND). In reality the number would likely to be lower than this due to line impedance.

Picking the 1ms SOA line on the chosen MOSFET, we can see that the worst case maximum power in the voltage range of interest at 1ms = 500W. Using the derate factor of 2 calculated earlier, this is derated to 250W constant power. The TIMER fault time should never exceed 1ms to avoid damaging the FET at

this power level We will add some extra margin to this TIMER fault time in the "TIMER capacitor" section if possible.

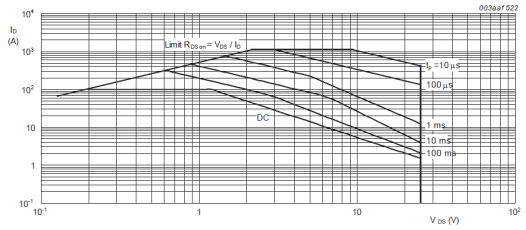

Figure 4. MOSFET SOA

Summary of the key spec / component selection for this section:

T_{SOA_MAX} = 1000µs

10. Power-up Analysis

Now that the timer had been selected, we must check to verify that there is sufficient time available to allow the loads caps to complete powerup. This is determined by how long the startup current profile intersects with the current limit, i.e. how long the timer is active during powerup.

During the *power-up* phase, the controller will usually hit the current limit due to the inrush current demanded by the load capacitance. If the time set by the TIMER pin is insufficient to allow the load capacitors to charge, then the MOSFET will be disabled and system will not power up.

We can use the following equation to estimate the ideal value in the case when foldback is not used:

$$t_{CHARGE} = \frac{C_{LOAD} \times V_{MAX}}{I_{MAXPK} - \frac{V_{MAX}}{R_{POWERUP}}}$$

$$= \frac{3000 \times 10^{-6}\ \text{F} \times 12.6\ \text{V}}{81\ \text{A} - \frac{12.6}{1000}}$$

$$\approx 466 \mu s$$

This equation assumes an ideal condition of load current ramping from 0 to Imax instantaneously.

When you add the foldback into the equation the current starts at the foldback clamp (8A) and ramps up to full load as Vout increases. As an estimate we can assume it will take more than 2x this time… resulting in approx 930µs. Adding tolerances this could result in the timer expiring before the startup has completed and the FETs being shut down.

However, in reality, the gate charge, Q_G, of the MOSFETs serves to limit the slew-rate of the gate voltage—and hence the power up current profile—so that a quantity of charge is delivered to the load capacitor without triggering the TIMER function.

The key parameter here is the C_{GD} of the MOSFET. This is because during this stage of the powerup the FETs are behaving like source-followers where the source dv/dt is following the profile of the gate dv/dt. So the V_{GS} during this stage remains largely constant and the V_{GD} is what is moving. Therefore most of the gate current is flowing into the C_{GD} of the MOSFETs.

In Figure 5, the MOSFET with the higher C_{GD} results in the TIMER being active for a shorter period, T1–T3, as compared to the MOSFET with the lower $C_{GD,}$ which causes the timer to be active during T0–T2.

This is because the charge delivered between T0 and T1 accumulates at less than the current limit. Thus, the calculated time required can be reduced accordingly. This can be used in a well characterised system to align start-up time with SOA limits.

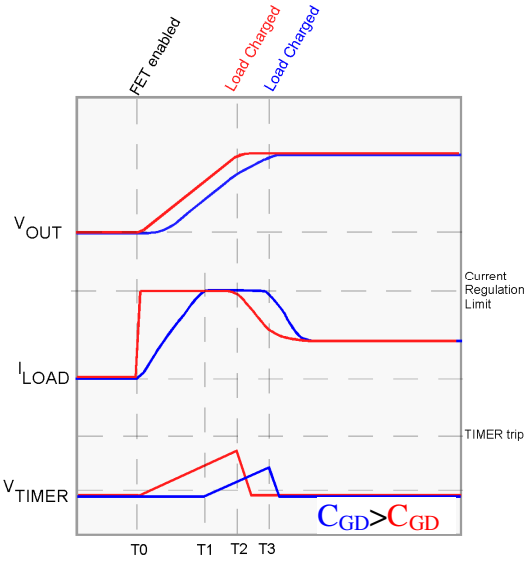

Figure 5. Effect of C_{GD} on start-up profiles.

This is difficult to quantify as the C_{GD} of the MOSFET is variable and dependant on the V_{DS} of the FET.

So based on typical performance data on the MOSFET, along with the gate pullup current, we can estimate the time it takes to charge these parasitic capacitors enough to bring V_{OUT} from 0 to Vmax (remember V_{OUT} follows V_{GATE}). This is done using the design tool.

As this specification is difficult to quantify we can add gate capacitance to dominate a minimum time to allow the system to powerup with the selected timer. By using a fixed capacitor and a fixed current source (by avoiding reaching limit) on the gate pin the inrush ramp can be assumed to be near square wave (derivative of the near linear slope of V_{OUT}, although in reality the curve may have sloped rise and fall edges due to the change in directions of gate currents around the FET parasitic capacitances at the start and the end of the output voltage ramp). The additional gate cap can be determined using the following equation:

$$C_{GATE} = \frac{C_{LOAD} \times I_{GATE}}{I_{FLBMIN} - \left(\frac{V_{CBOS}}{R_{SENSE}}\right)}$$

$$= \frac{3000 \times 10^{-6}\ \text{F} \times 25\mu A}{8A - (\frac{0.88mV}{0.25m\Omega})}$$

$$\approx 16.7nF$$

So a 16.7nF gate capacitor can be used to ensure the inrush current remains below the current limit. Looking at the design tool we can see that at all worst case conditions this shouldn't result in any intersection with the current limit. Choosing a capacitor value of 22nF will ensure the current limit will not be exceeded at power-up.

Note also that the actual value of gate capacitance could vary due to the C_{GD} that is not quantified or represented in this equation. If the effective C_{GD} can be quantified, through whatever means, this can be subtracted from the value above. So in reality a smaller cap may be sufficient to provide adequate clearance as remember there is sufficient timer available to allow some intersection. However, this would need to be tested and verified to be the case. The size of the gate capacitor also controls the VOUT ramp time so can be made larger if a longer ramp time is required. Power-up time can now be calculated as follows:

$$t_{POWERUP} = \frac{C_{GATE} \times V_{MAX}}{I_{GATE}}$$

$$= \frac{22\text{nF} \times 12.6\ \text{V}}{25\mu A}$$

$$\approx 11.1ms$$

If the worst case C_{GD} is added to this a figure of closer to 15ms could be achieved.

Summary of the key spec / component selection for this section:

C_{GATE} = 22 nF
$T_{POWERUP}$ = ~11.1ms to 15ms

11. Timer Capacitor

Now that the MOSFETs SOA requirements have been determined and power-up time is satisfied, a TIMER capacitor value can be calculated. This can be calculated as follows:

$$C_{TIMER} = \frac{t_{TIMER} \times I_{TIMER}}{V_{TIMER}}$$

Where I_{TIMER} = 60 µA and V_{TIMER} = 1.0 V,

$$C_{TIMER} = \frac{\left(1000 \times 10^{-6}\ \text{s}\right) \times \left(60 \times 10^{-6}\ \text{A}\right)}{1.0\ \text{V}}$$

$$\approx 60\ \text{nF}$$

Therefore, a capacitor value smaller than 60nF is required. Using the design tool to consider all the tolerances it can be determined that a 10nF capacitor will result in a timer fault time of between 147µs and 188µs, worst case. This will be an acceptable value for SOA protection and provides maximum FET protection. If a longer fault filter time is desired then a 22nF or 33nF TIMER capacitor will also provide sufficient protection.

Summary of the key spec / component selection for this section:

C_{TIMER} = 10 nF

12. Start-up Current Limit

The Start-up current limit is a fixed current limit that is only active when PWRGD is bad. This current limit can therefore be used to detect any unexpectedly large inrush current during dv/dt power-up where the inrush is normally well below the foldback or ISET current limits.

The ISTART pin is used to select the start-up current limit. It can be tied low for a default 2mV Vsense limit or can be configured with a resistor divider to VCAP to configure a different current limit.

$$V_{ISTART} = \frac{RISTART2}{RISTART1 + RISTART2} \times VCAP$$

$$StartupCL = \frac{V_{ISTART}}{AV_{CSAMP} \times R_{SENSE}}$$

where AV_{CSAMP} = 50 V/V (gain of current sense amplifier)

Inrush current during dv/dt power-up is not expected to exceed 3 or 4 Amps according to the design tool. Therefore a realistic limit for the start-up current limit could be 8 to 10A. This is above the expected inrush current and below the maximum power level allowed in the MOSFET.

The ISTART pin can be tied to GND for an 8A start-up current limit (V_{ISTART_CLAMP} = 0.1V) or a resistor divider to VCAP of RISTART1 = 100kΩ and RISTART2 = 4.85kΩ for a 10A start-up current limit. A decoupling capacitor can be added to the ISTART resistor divider string if required.

The circuit breaker offset of 0.88 mV will have a greater effect at these low Vsense levels so should be taken into account. The circuit breaker limit is the level above which the TIMER will start to ramp. So for the 8 A current limit calculated above, the circuit breaker limit will be 2 mV – 0.88 mV = 1.12 mV. This corresponds to a circuit breaker current of 1.12 mV / 0.25 mΩ = 4.48A. A 10 A current limit will give a circuit breaker limit of 6.47 A.

It is also possible to program the startup current limit via PMBus. See datasheet for more details.

Summary of the key spec / component selection for this section:

Start-up CL	= 10 A (6.5 A circuit breaker)
$R_{ISTART1}$	= 100 KΩ
$R_{ISTART2}$	= 4.85 KΩ
C_{ISTART}	= 10 nF

13. Power in MOSFET at start-up – SOA

Now, as a final step we need to check that the power being dissipated in the FETs at startup is within the SOA limits of the MOSFET. We can calculate the Energy required to charge the load cap as follows:

$$E_{CL} = \frac{CV^2}{2}$$
$$= \frac{3000 \times 10^{-6} \times (12.6)^2}{2}$$
$$\approx 0.238\, joules$$

The power can be determined using:

$$P_{FET} = \frac{E}{t}$$
$$= \frac{0.238}{11.1 \times 10^{-3}}$$
$$\approx 21.4W$$

Derate this to 64W (21.4W x 3). Now calculate the current at max V_{DS}

$$I = \frac{P}{V} = \frac{64}{12.6} = 5.1A$$

Now if we examine the SOA again, we can see that 12.6V and 5.1A corresponds to ~50ms. As the maximum expected power-up is ~15ms, there is adequate room for tolerance and margin within this spec.