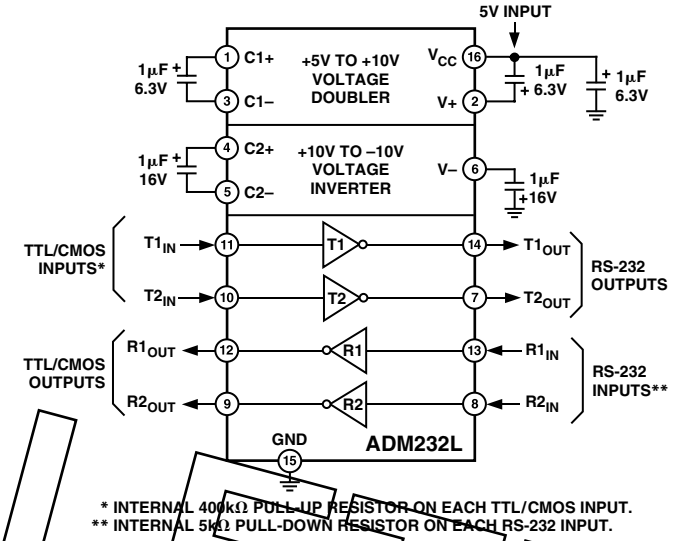
5 V Powered CMOS RS-232 Drivers/Receivers

ADM223/ADM230L–ADM241L

FEATURES
Single 5 V Power Supply
Meets All EIA-232-E and V.28 Specifications
120 kB/s Data Rate
On-Board DC-DC Converters
±9 V Output Swing with 5 V Supply
Small 1 μF Capacitors
Low Power Shutdown ≤1 μA
Receivers Active in Shutdown (ADM223)
±30 V Receiver Input Levels
Latch-Up FREE
Plug-In Upgrade for MAX223/230-241
Plug-In Upgrade for AD230–AD241

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

ADM232L TYPICAL OPERATING CIRCUIT



* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

GENERAL DESCRIPTION

The ADM2xx family of line drivers/receivers is intended for all EIA-232-E and V.28 communications interfaces, especially in applications where ±12 V is not available. The ADM223, ADM230L, ADM235L, ADM236L and ADM241L feature a low power shutdown mode that reduces power dissipation to less than 5 μW, making them ideally suited for battery powered equipment. Two receivers remain enabled during shutdown on the ADM223. The ADM233L and ADM235L do not require any external components and are particularly useful in applications where printed circuit board space is critical.

All members of the ADM230L family, except the ADM231L and the ADM239L, include two internal charge pump voltage converters that allow operation from a single 5 V supply. These converters convert the 5 V input power to the ±10 V required for RS-232 output levels. The ADM231L and ADM239L are designed to operate from 5 V and 12 V supplies. An internal +12 V to –12 V charge pump voltage converter generates the –12 V supply.

The ADM2xxL is an enhanced upgrade for the AD2xx family featuring lower power consumption, faster slew rate and operation with smaller (1 μF) capacitors.

Table I. Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Pins
ADM223	5 V	4	5	4	Yes ($\overline{SD}$)	Yes (EN)	28
ADM230L	5 V	5	0	4	Yes	No	20
ADM231L	5 V and 7.5 V to 13.2 V	2	2	2	No	No	14
ADM232L	5 V	2	2	4	No	No	16
ADM233L	5 V	2	2	None	No	No	20
ADM234L	5 V	4	0	4	No	No	16
ADM235L	5 V	5	5	None	Yes	Yes	24
ADM236L	5 V	4	3	4	Yes	Yes	24
ADM237L	5 V	5	3	4	No	No	24
ADM238L	5 V	4	4	4	No	No	24
ADM239L	5 V and 7.5 V to 13.2 V	3	5	2	No	Yes	24
ADM241L	5 V	4	5	4	Yes	Yes	28

REV. B

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ADM223/ADM230L–ADM241L–SPECIFICATIONS (V_{CC} = 5 V ± 10% (ADM223, ADM231L, ADM232L, ADM234L, ADM236L, ADM238L, ADM239L, ADM241L); V_{CC} = 5 V ± 5% (ADM230L, ADM233L, ADM235L, ADM237L); V+ = 7.5 V to 13.2 V (ADM231L and ADM239L); C1–C4 = 1.0 µF Ceramic. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Swing	±5	±9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		2.5	6.0	mA	No Load, (ADM232L only)
		3.5	13	mA	No Load
V+ Power Supply Current		1.5	4	mA	No Load, V+ = 12 V ADM231L and ADM239L Only
Shutdown Supply Current		1	10	µA	
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Input Logic Threshold High, V_{INH}	2.4			V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Logic Pull-Up Current		12	25	µA	T_{IN} = 0 V
RS-232 Input Voltage Range[1]	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.6	2.4	V	
RS-232 Input Hysteresis		0.25		V	
RS-232 Input Resistance	3	5	7	kΩ	T_A = 0°C to 85°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
TTL/CMOS Output Leakage Current		0.05	±10	µA	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		250		ns	ADM223, ADM235L, ADM236L, ADM239L, ADM241L (Figure 25. C_L = 150 pF)
Output Disable Time (T_{DIS})		50		ns	ADM223, ADM235L, ADM236L, ADM239L, ADM241L (Figure 25. R_L = 1 kΩ)
Propagation Delay		0.3		µs	RS-232 to TTL
Transition Region Slew Rate		8		V/µs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to –3 V or –3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10		mA	

NOTES
[1]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{CC} ..... –0.3 V to +6 V
V+ ..... (V_{CC} – 0.3 V) to +14 V
V– ..... +0.3 V to –14 V
Input Voltages
  T_{IN} ..... –0.3 V to (V_{CC} + 0.3 V)
  R_{IN} ..... ±30 V
Output Voltages
  T_{OUT} ..... (V+, + 0.3 V) to (V–, – 0.3 V)
  R_{OUT} ..... –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} ..... Continuous
Power Dissipation
  N-14 DIP (Derate 10 mW/°C above 70°C) ..... 800 mW
  N-16 DIP (Derate 10.5 mW/°C above 70°C) ..... 840 mW
  N-20 DIP (Derate 11 mW/°C above 70°C) ..... 890 mW
  N-24 DIP (Derate 13.5 mW/°C above 70°C) .... 1000 mW
  N-24A DIP (Derate 13.5 mW/°C above 70°C) ... 500 mW
  R-16 SOIC (Derate 9 mW/°C above 70°C) ..... 760 mW
  R-20 SOIC (Derate 9.5 mW/°C above 70°C) .... 800 mW
  R-24 SOIC (Derate 12 mW/°C above 70°C) ..... 850 mW
  R-28 SOIC (Derate 12.5 mW/°C above 70°C) ... 900 mW
  RS-28 SSOP (Derate 10 mW/°C above 70°C) .... 900 mW
  Q-14 Cerdip (Derate 10 mW/°C above 70°C) .... 720 mW
  Q-16 Cerdip (Derate 10 mW/°C above 70°C) .... 800 mW
  Q-20 Cerdip (Derate 11.2 mW/°C above 70°C) .... 890 mW
  Q-24 Cerdip (Derate 12.5 mW/°C above 70°C) ... 1000 mW
  D-24 Ceramic (Derate 20 mW/°C above 70°C) .. 1000 mW
Thermal Impedance, θ_{JA}
  N-14 DIP ..... 140°C/W
  N-16 DIP ..... 135°C/W
  N-20 DIP ..... 125°C/W
  N-24 DIP ..... 120°C/W
  N-24A DIP ..... 110°C/W
  R-16 SOIC ..... 105°C/W
  R-20 SOIC ..... 105°C/W
  R-24 SOIC ..... 85°C/W
  R-28 SOIC ..... 80°C/W
  RS-28 SSOP ..... 100°C/W
  Q-14 Cerdip ..... 105°C/W
  Q-16 Cerdip ..... 100°C/W
  Q-20 Cerdip ..... 100°C/W
  Q-24 Cerdip ..... 55°C/W
  D-24 Ceramic ..... 50°C/W
Operating Temperature Range
  Commercial (J Version) ..... 0 to 70°C
  Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature, Soldering ..... 300°C
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C

*This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*
ADM223			**ADM230L**			**ADM231L**		
ADM223AR	–40°C to +85°C	R-28	ADM230LJN	0°C to 70°C	N-20	ADM231LJN	0°C to 70°C	N-14
ADM223ARS	–40°C to +85°C	RS-28	ADM230LJR	0°C to 70°C	R-20	ADM231LJR	0°C to 70°C	R-16
			ADM230LAN	–40°C to +85°C	N-20	ADM231LAN	–40°C to +85°C	N-14
			ADM230LAR	–40°C to +85°C	R-20	ADM231LAR	–40°C to +85°C	R-16
			ADM230LAQ	–40°C to +85°C	Q-20	ADM231LAQ	–40°C to +85°C	Q-14
ADM232L			**ADM233L**			**ADM234L**		
ADM232LJN	0°C to 70°C	N-16	ADM233LJN	0°C to 70°C	N-20	ADM234LJN	0°C to 70°C	N-16
ADM232LJR	0°C to 70°C	R-16	ADM233LAN	–40°C to +85°C	N-20	ADM234LJR	0°C to 70°C	R-16
ADM232LAN	–40°C to +85°C	N-16				ADM234LAN	–40°C to +85°C	N-16
ADM232LAR	–40°C to +85°C	R-16				ADM234LAR	–40°C to +85°C	R-16
ADM232LAQ	–40°C to +85°C	Q-16				ADM234LAQ	–40°C to +85°C	Q-16
ADM235L			**ADM236L**			**ADM237L**		
ADM235LJN	0°C to 70°C	N-24A	ADM236LJN	0°C to 70°C	N-24	ADM237LJN	0°C to 70°C	N-24
ADM235LAN	–40°C to +85°C	N-24A	ADM236LJR	0°C to 70°C	R-24	ADM237LJR	0°C to 70°C	R-24
ADM235LAQ	–40°C to +85°C	D-24	ADM236LAN	–40°C to +85°C	N-24	ADM237LAN	–40°C to +85°C	N-24
			ADM236LAR	–40°C to +85°C	R-24	ADM237LAR	–40°C to +85°C	R-24
			ADM236LAQ	–40°C to +85°C	Q-24	ADM237LAQ	–40°C to +85°C	Q-24
ADM238L			**ADM239L**			**ADM241L**		
ADM238LJN	0°C to 70°C	N-24	ADM239LJN	0°C to 70°C	N-24	ADM241LJR	0°C to 70°C	R-28
ADM238LJR	0°C to 70°C	R-24	ADM239LJR	0°C to 70°C	R-24	ADM241LAR	–40°C to +85°C	R-28
ADM238LAN	–40°C to +85°C	N-24	ADM239LAN	–40°C to +85°C	N-24	ADM241LJRS	0°C to 70°C	RS-28
ADM238LAR	–40°C to +85°C	R-24	ADM239LAR	–40°C to +85°C	R-24	ADM241LARS	–40°C to +85°C	RS-28
ADM238LAQ	–40°C to +85°C	Q-24	ADM239LAQ	–40°C to +85°C	Q-24			

*D = Ceramic DIP; N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC); RS = Small Shrink Outline Package (SSOP).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM223/ADM230L–ADM241L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

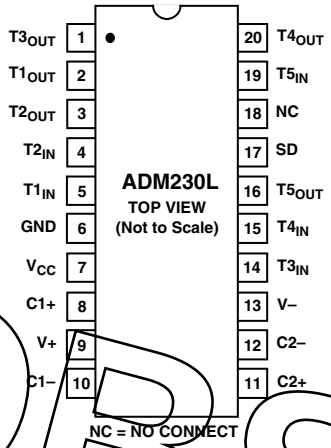


Figure 1. ADM230L DIP/SOIC Pin Configuration

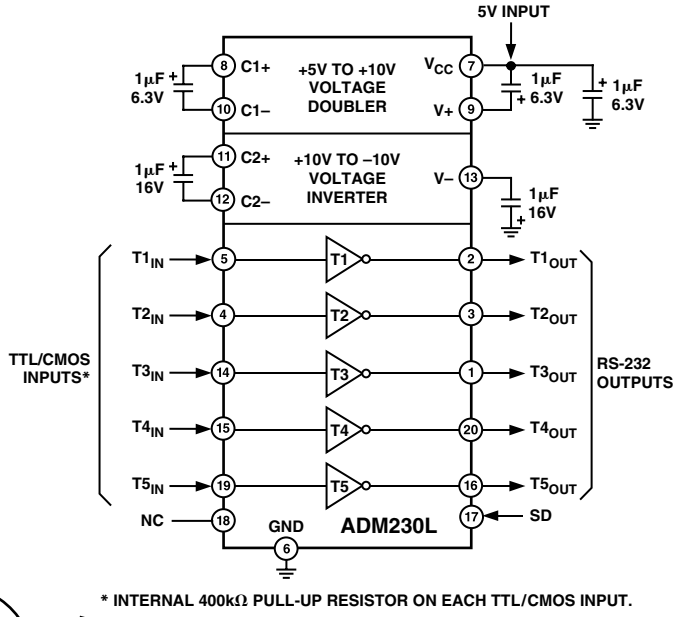
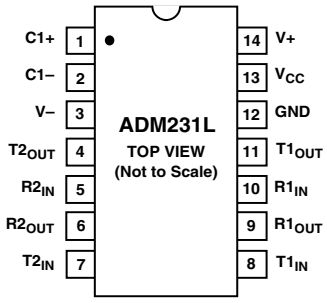


Figure 2. ADM230L Typical Operating Circuit

DIP



SOIC

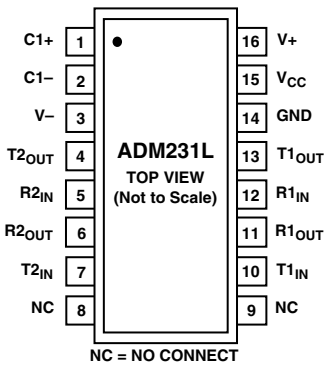


Figure 3. ADM231L DIP and SOIC Pin Configurations

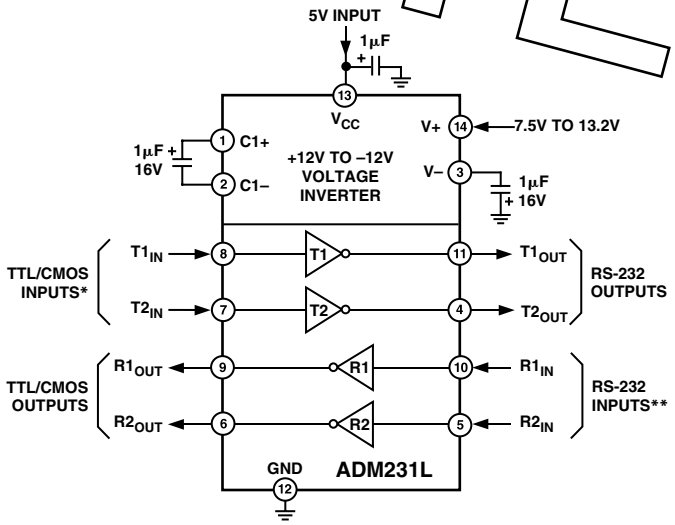


Figure 4. ADM231L Typical Operating Circuit (DIP Pinout)

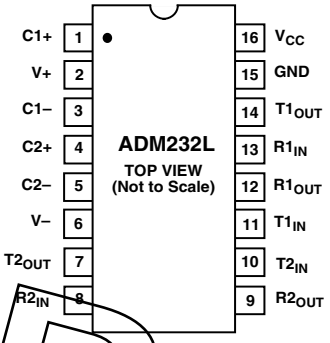
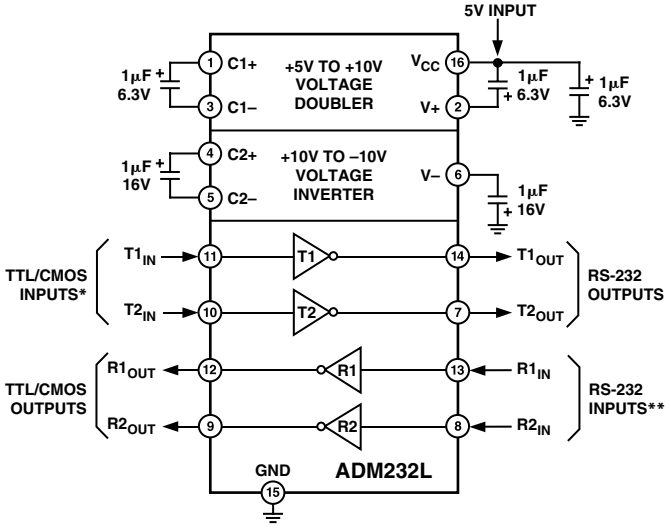


Figure 5. ADM232L DIP/SOIC Pin Configuration



* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

Figure 6. ADM232L Typical Operating Circuit

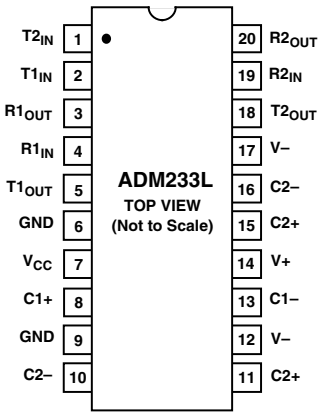
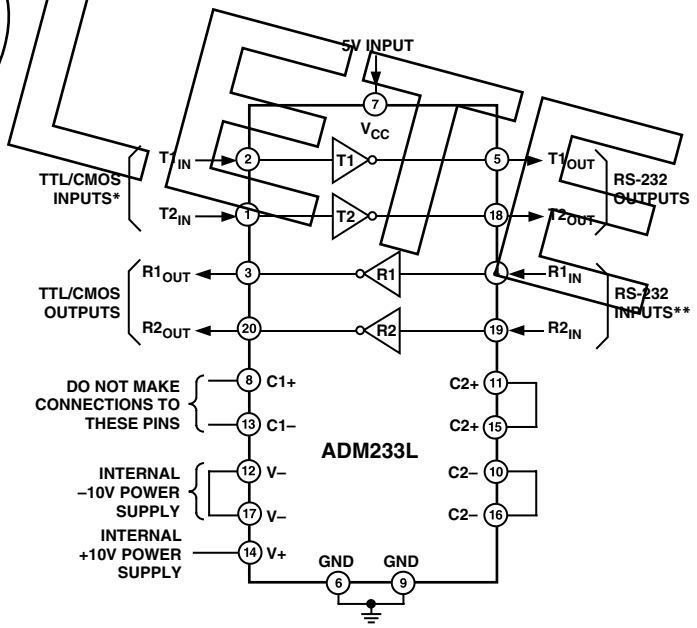


Figure 7. ADM233L DIP Pin Configuration



* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

Figure 8. ADM233L Typical Operating Circuit

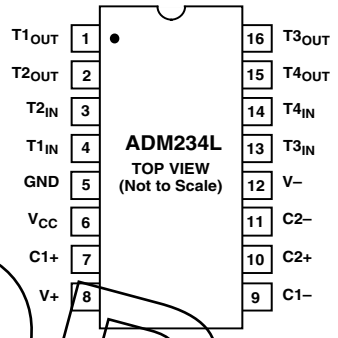


Figure 9. ADM234L DIP/SOIC Pin Configuration

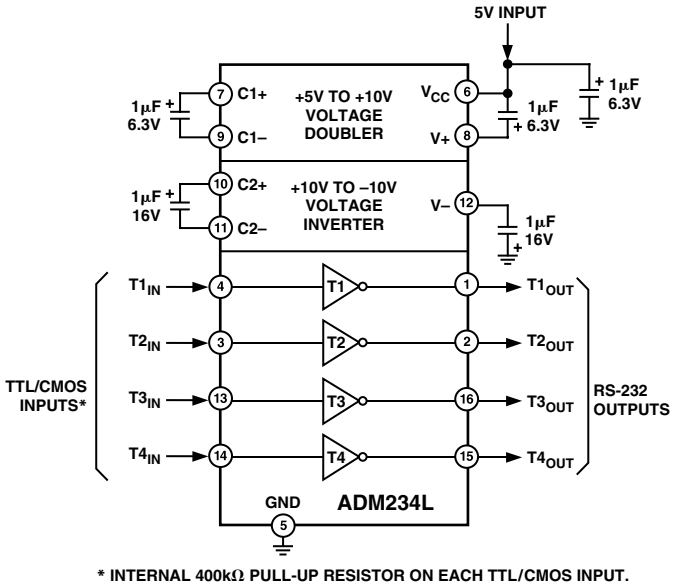


Figure 10. ADM234L Typical Operating Circuit

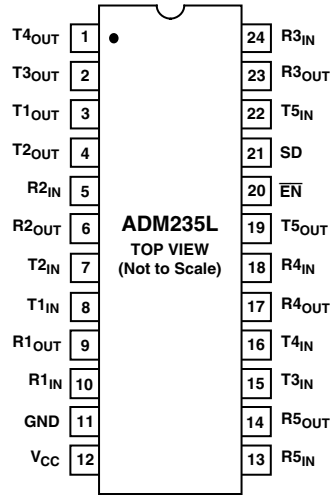


Figure 11. ADM235L DIP Pin Configuration

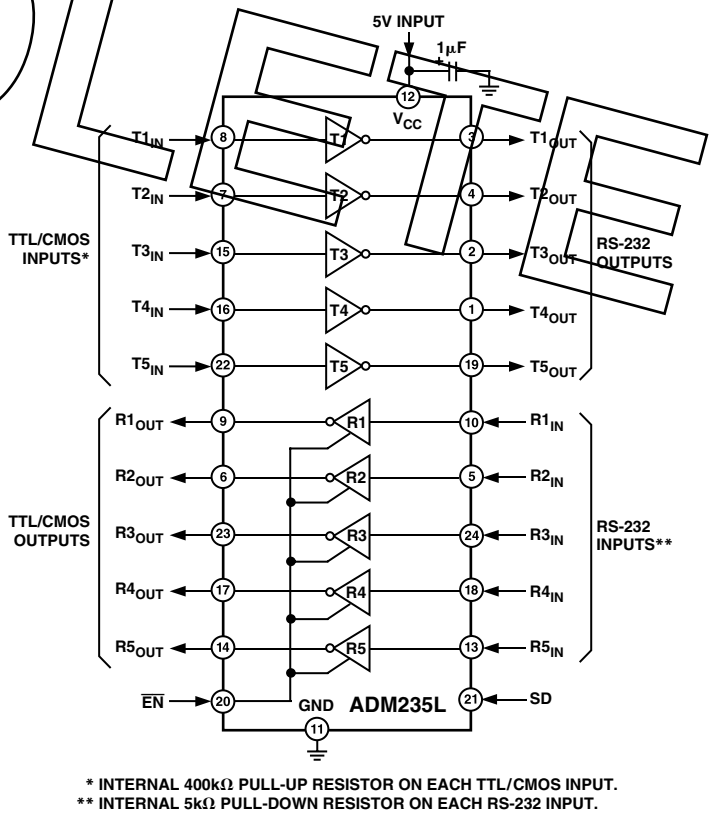


Figure 12. ADM235L Typical Operating Circuit

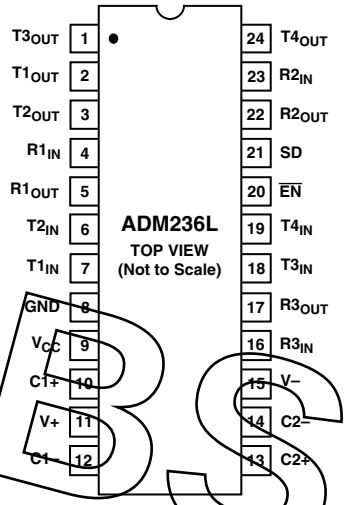


Figure 13. ADM236L DIP/SOIC Pin Configuration

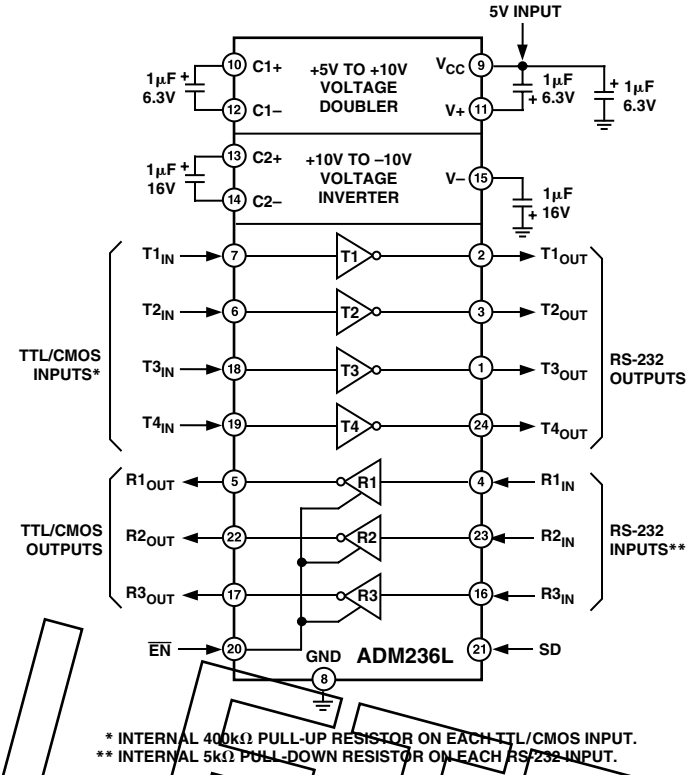


Figure 14. ADM236L Typical Operating Circuit

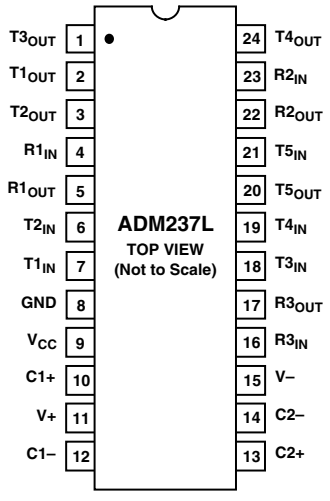


Figure 15. ADM237L DIP/SOIC Pin Configuration

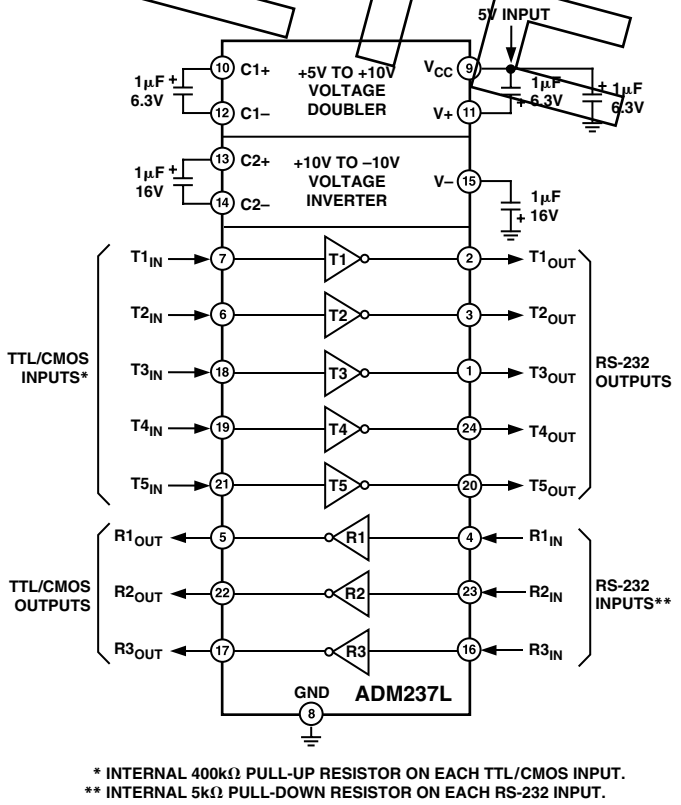


Figure 16. ADM237L Typical Operating Circuit

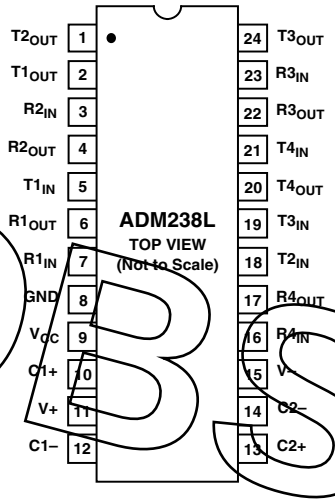


Figure 17. ADM238L DIP/SOIC Pin Configuration

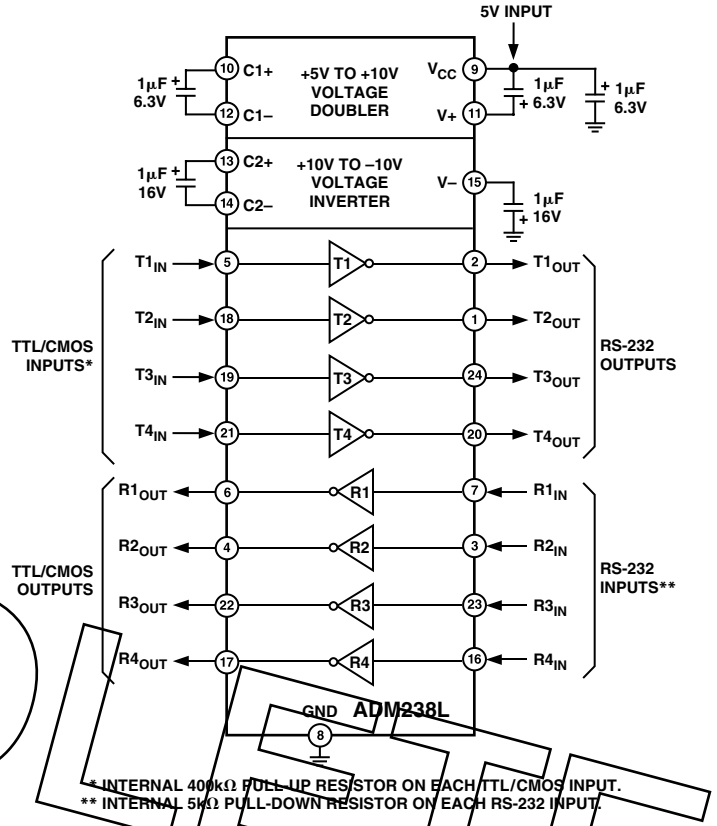


Figure 18. ADM238L Typical Operating Circuit

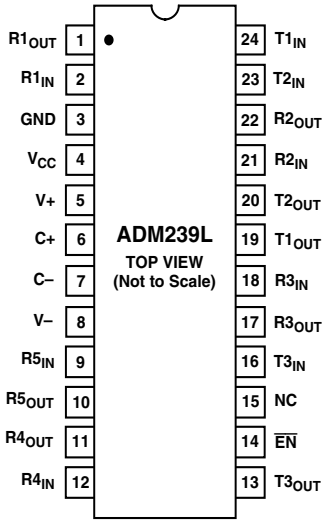


Figure 19. ADM239L DIP/SOIC Pin Configuration

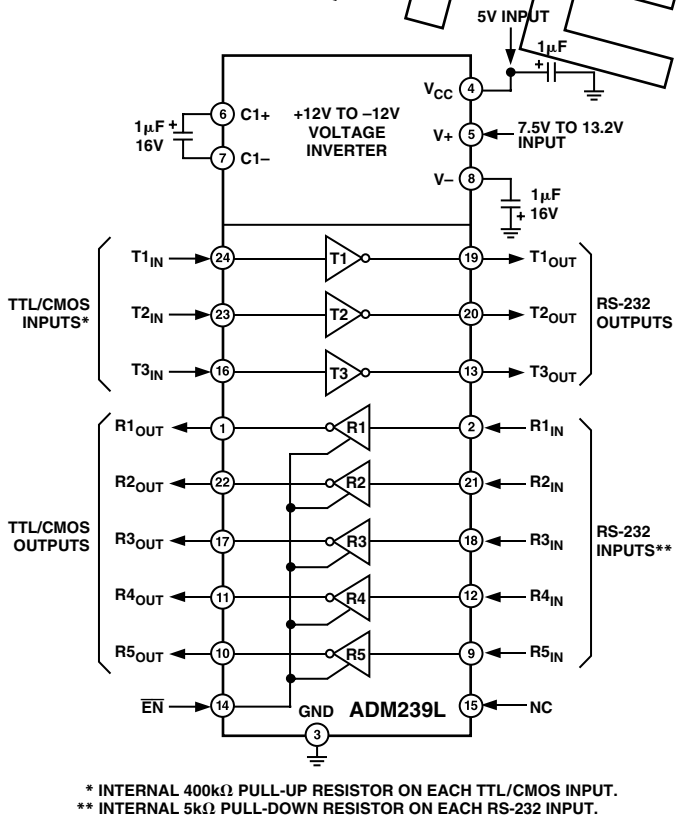


Figure 20. ADM239L Typical Operating Circuit

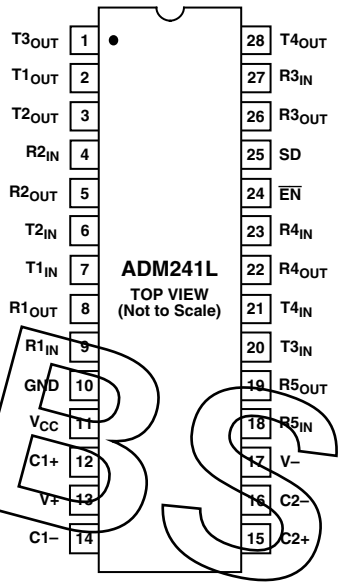


Figure 21. ADM241L SOIC/SSOP Pin Configuration

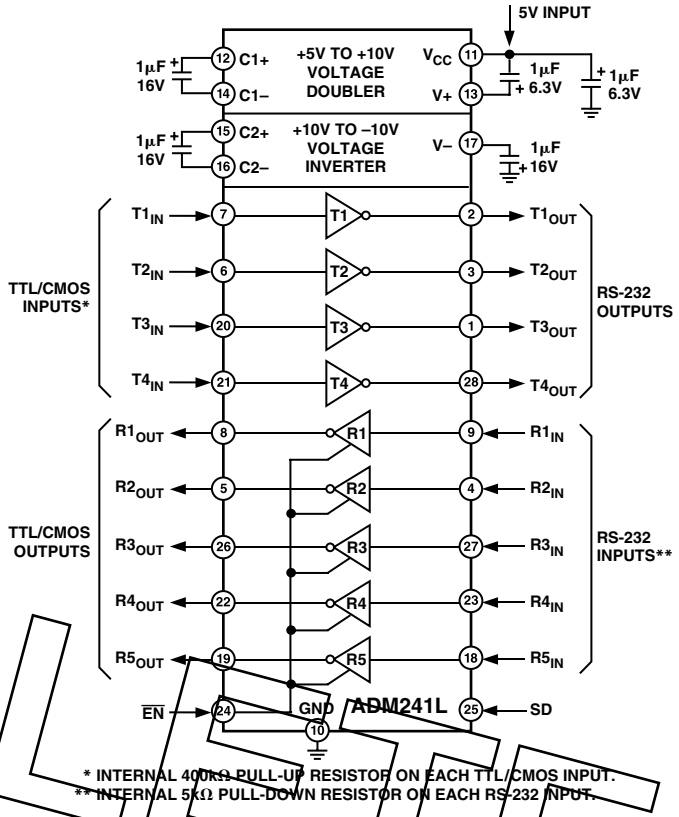


Figure 22. ADM241L Typical Operating Circuit

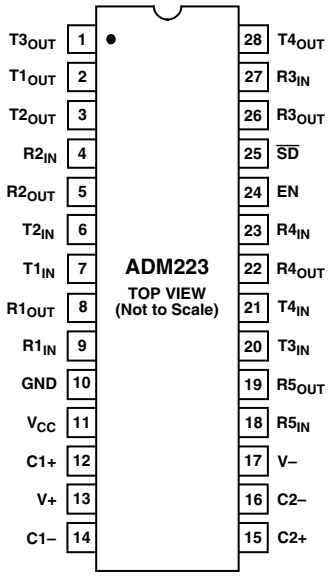


Figure 23. ADM223 SOIC/SSOP Pin Configuration

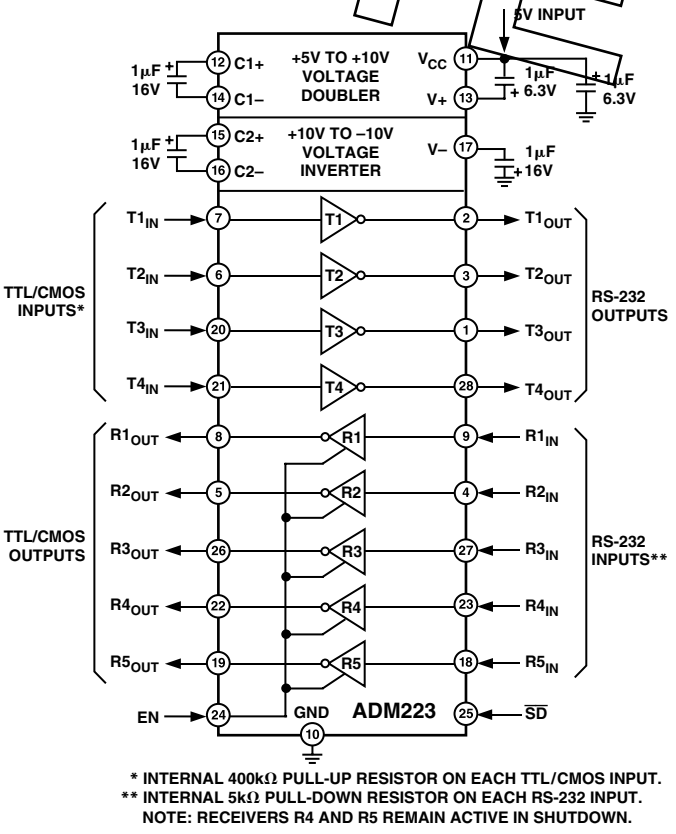


Figure 24. ADM223 Typical Operating Circuit

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input 5 V ± 10% (5 V ± 5% ADM233L, ADM235L).
V+	Internally generated positive supply (+10 V nominal) on all parts except ADM231L and ADM239L. ADM231L, ADM239L requires external 7.5 V to 13.2 V supply.
V–	Internally generated negative supply (–10 V nominal).
GND	Ground pin. Must be connected to 0 V.
C+	(ADM231L and ADM239L only). External capacitor (+ terminal) is connected to this pin.
C–	(ADM231L and ADM239L only). External capacitor (– terminal) is connected to this pin.
C1+	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (+ terminal) is connected to this pin. (ADM233L) The capacitor is connected internally and no external connection to this pin is required.
C1–	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (– terminal) is connected to this pin. (ADM233L) The capacitor is connected internally and no external connection to this pin is required.
C2+	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (+ terminal) is connected to this pin. (ADM233L) Internal capacitor connections, Pins 11 and 15 must be connected together.
C2–	(ADM230L, ADM232L, ADM234L, ADM236L, ADM237L, ADM238L, ADM241L) External capacitor (– terminal) is connected to this pin. (ADM233L) Internal capacitor connections, Pins 10 and 16 must be connected together.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ± 10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$/EN	Enable Input. Active low on ADM235L, ADM236L, ADM239L, ADM241L. Active high ADM223. This input is used to enable/disable the receiver outputs. With $\overline{EN}$ = low (EN = high ADM223), the receiver outputs are enabled. With $\overline{EN}$ = high (EN = low ADM223), the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD/$\overline{SD}$	Shutdown Input. Active high on ADM235L, ADM236L, ADM241L. Active low on ADM223. With SD = high on the ADM235L, ADM236L, ADM241L, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off. With $\overline{SD}$ low on the ADM223, the charge pump is disabled, the driver outputs are turned off and all receivers except R4 and R5 are placed in a high impedance state. In shutdown, the power consumption reduces to 5 µW.
NC	No Connect. No connections are required to this pin.

Table I. ADM235L, ADM236L, ADM241L Truth Table

SD	$\overline{EN}$	Status	Transmitters T1–T5	Receivers R1–R5
0	0	Normal Operation	Enabled	Enabled
0	1	Normal Operation	Enabled	Disabled
1	0	Shutdown	Disabled	Disabled

Table II. ADM223 Truth Table

$\overline{SD}$	EN	Status	Transmitters T1–T4	Receivers R1–R3	Receivers R4, R5
0	0	Shutdown	Disabled	Disabled	Disabled
0	1	Shutdown	Disabled	Disabled	Enabled
1	0	Normal Operation	Enabled	Disabled	Disabled
1	1	Normal Operation	Enabled	Enabled	Enabled

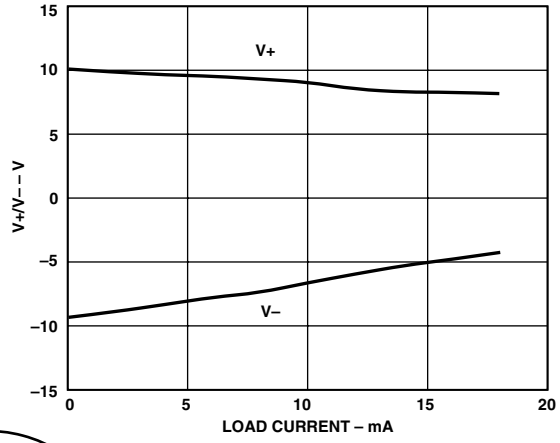


Figure 25. Charge Pump V+, V– vs. Current

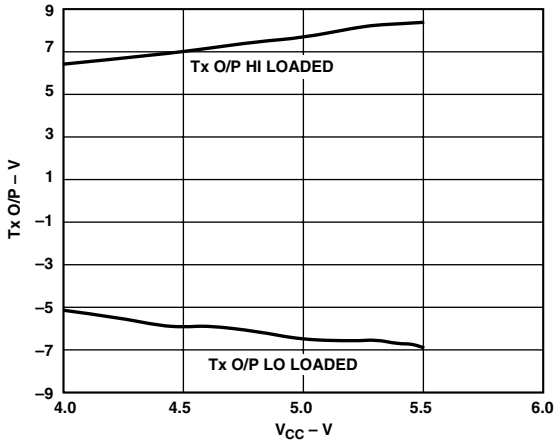


Figure 27. Transmitter Output Voltage vs. V_{CC}

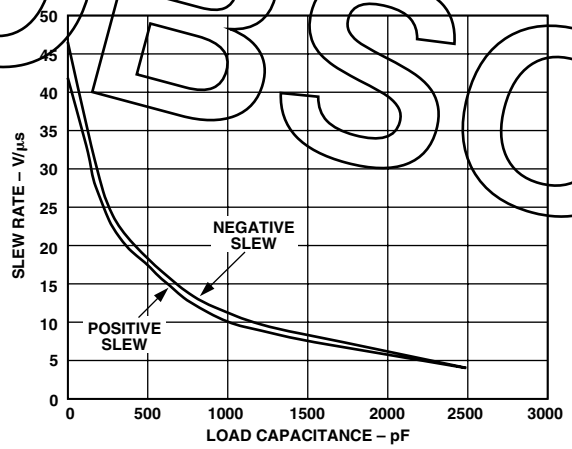


Figure 26. Transmitter Slew Rate vs. Load Capacitance

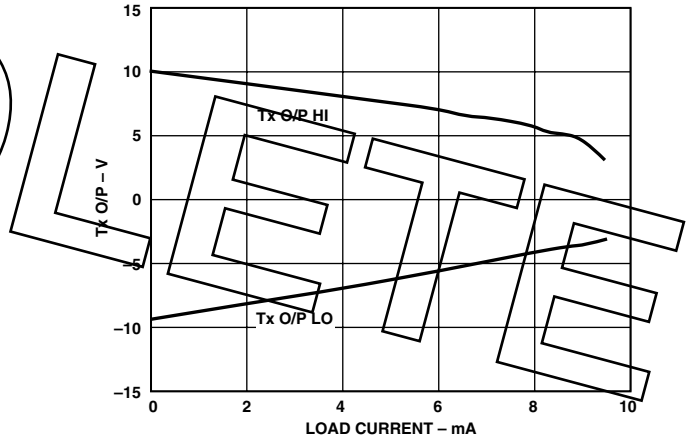


Figure 28. Transmitter Output Voltage vs. Current

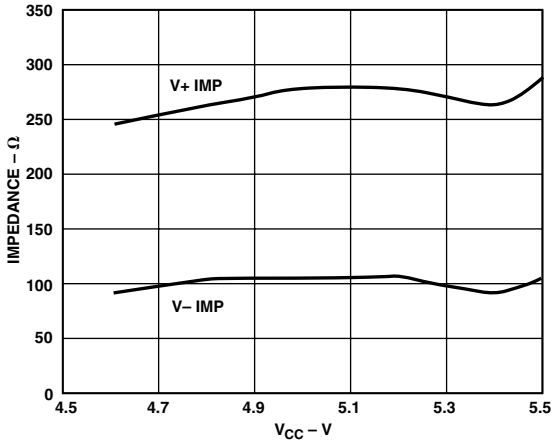


Figure 29. Charge Pump Impedance vs. V_{CC}

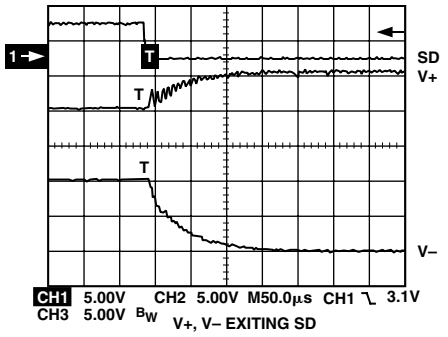


Figure 30. Charge Pump, V+, V– Exiting Shutdown

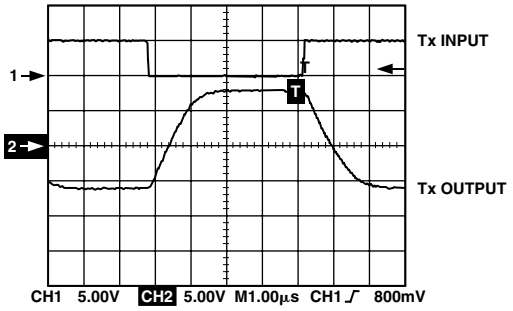


Figure 31. Transmitter Output Loaded Slew Rate

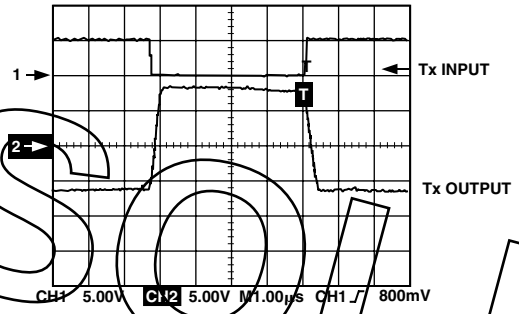


Figure 32. Transmitter Output Unloaded Slew Rate

GENERAL INFORMATION

The ADM223/ADM230L–ADM241L family of RS-232 drivers/receivers are designed to solve interface problems by meeting the EIA-232-E specifications while using a single digital 5 V supply. The EIA-232-E standard requires transmitters which will deliver ±5 V minimum on the transmission channel and receivers which can accept signal levels down to ±3 V. The ADM223/ADM230L–ADM241L meet these requirements by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/receiver combinations is available to cover most communications needs.

The ADM223, ADM230L, ADM235L, ADM236L and ADM241L are particularly useful in battery powered systems as they feature a low power shutdown mode which reduces power dissipation to less than 5 µW.

The ADM233L and ADM235L are designed for applications where space saving is important as the charge pump capacitors are molded into the package.

The ADM231L and ADM239L include only a negative charge pump converter and are intended for applications where a positive 12 V is available.

To facilitate sharing a common line or for connection to a microprocessor data bus the ADM235L, ADM236L, ADM239L and ADM241L feature an enable (EN, $\overline{EN}$) function. When disabled, the receiver outputs are placed in a high impedance state.

CIRCUIT DESCRIPTION

The internal circuitry in the ADM230L–ADM241L consists of three main sections. These are:

(a) A charge pump voltage converter
(b) RS-232 to TTL/CMOS receivers
(c) TTL/CMOS to RS-232 transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated in Figures 33 and 34. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate –10 V using C2 as the storage element.

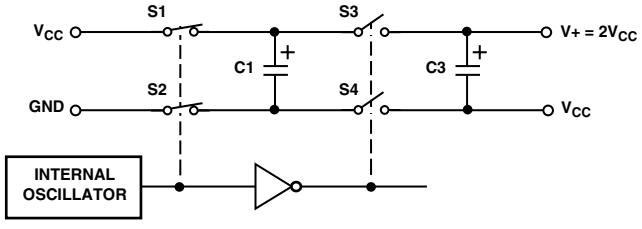


Figure 33. Charge-Pump Voltage Doubler

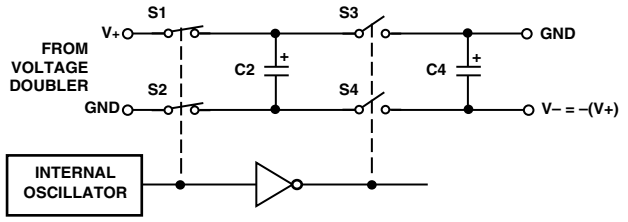


Figure 34. Charge-Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V– supplies.

The V+ and V– supplies may also be used to power external circuitry if the current requirements are small.

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With V_{CC} = +5 V and driving a typical EIA-232-E load, the output voltage swing is ±9 V. Even under worst-case conditions the drivers are guaranteed to meet the ±5 V EIA-232-E minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the EIA-232-E standard, the slew rate is limited to less than 30 V/µs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept EIA-232-E input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V EIA-232-E requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.5 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

Shutdown (SD)

The ADM223, ADM230L, ADM235L, ADM236L and ADM241L feature a control input that may be used to disable the part and reduce the power consumption to less than 5 µW. This is very useful in battery operated systems. During shutdown the charge pump is turned off, the transmitters are disabled and all receivers except R4 and R5 on the ADM223 are put into a high-impedance disabled state. Receivers R4 and R5 on the ADM223 remain enabled during shutdown. This feature allows monitoring external activity such as ring indicator monitoring while the device is in a low power shutdown mode.

The shutdown control input is active high on all parts except the ADM223 where it is active low. Refer to Tables I and II.

Enable Input

The ADM235, ADM239, ADM241L and ADM223 feature an enable input used to enable or disable the receiver outputs. The enable input is active low on the ADM235L, ADM239L, ADM241L and active high on the ADM223. Refer to Tables I and II. When disabled, all receiver outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 35.

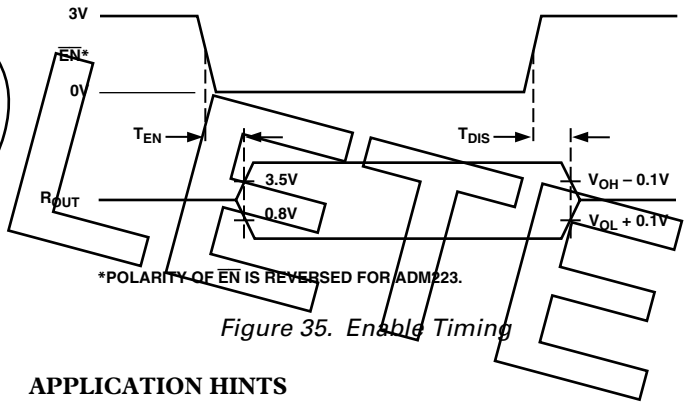


Figure 35. Enable Timing

APPLICATION HINTS

Driving Long Cables

In accordance with the EIA-232-E standard, long cables are permissible provided that the total load capacitance does not exceed 2500 pF. For longer cables which do exceed this, then it is possible to trade off baud rate vs. cable length. Large load capacitances cause a reduction in slew rate, and hence the maximum transmission baud rate is decreased. The ADM230L-ADM241L are designed so that the slew rate reduction with increasing load capacitance is minimized.

For the receivers, it is important that a high level of noise immunity be inbuilt so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The ADM230L-ADM241L have 0.5 V of hysteresis to guard against this. This ensures that, even in noisy environments, error-free reception can be achieved.

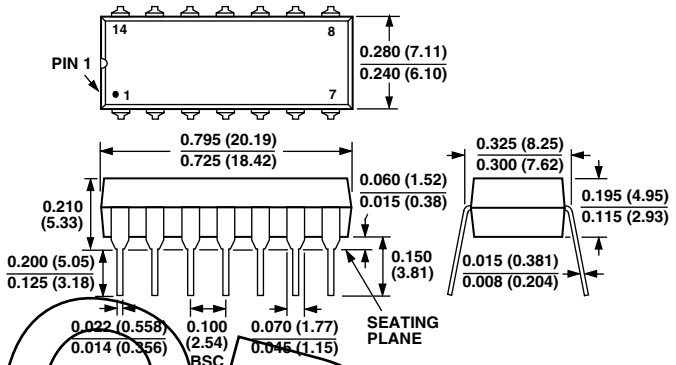
High Baud Rate Operation

The ADM230L-ADM241L feature high slew rates permitting data transmission at rates well in excess of the EIA-232-E specification. The drivers maintain ±5 V signal levels at data rates up to 100-kB/s under worst-case loading conditions.

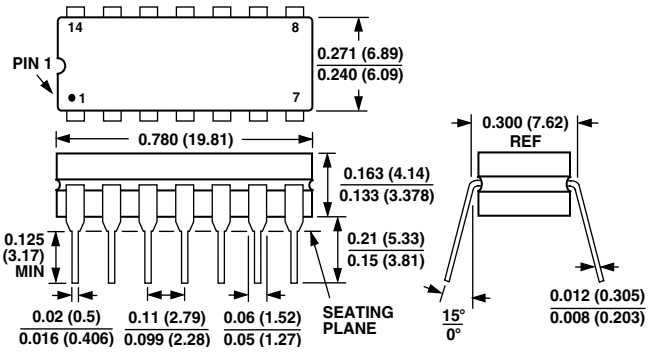
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

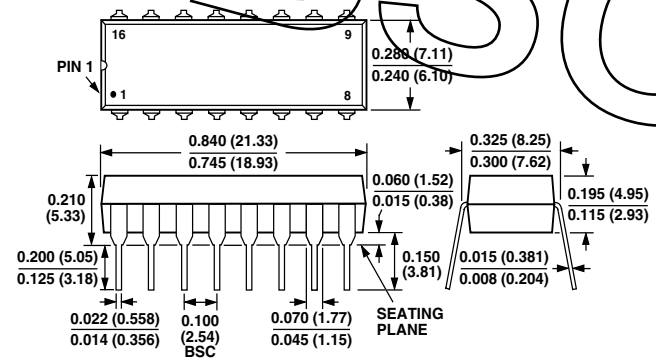
14-Lead Plastic DIP (N-14)



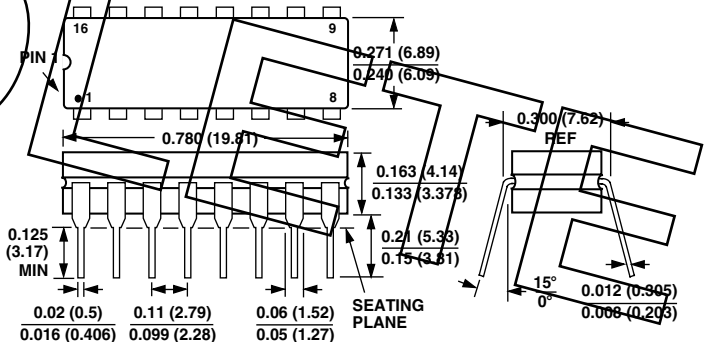
14-Lead Cerdip (Q-14)



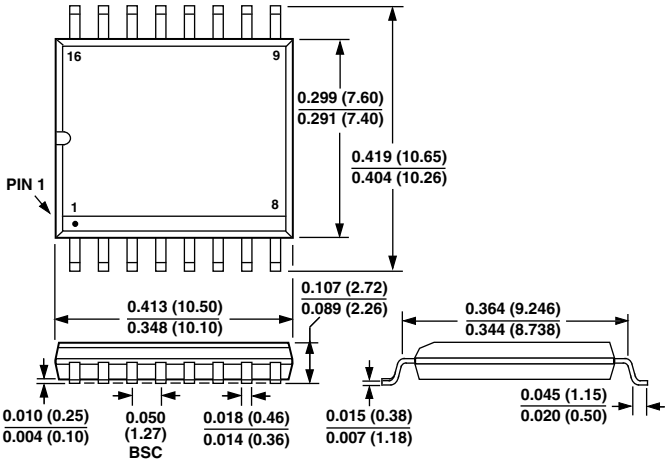
16-Lead Plastic DIP (N-16)



16-Lead Cerdip (Q-16)



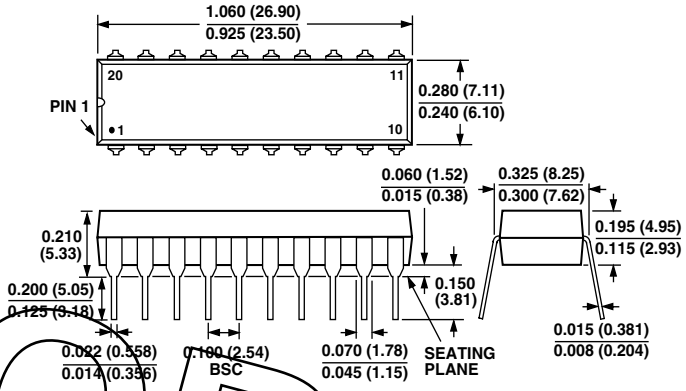
16-Lead SOIC (R-16)



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Plastic DIP (N-20)



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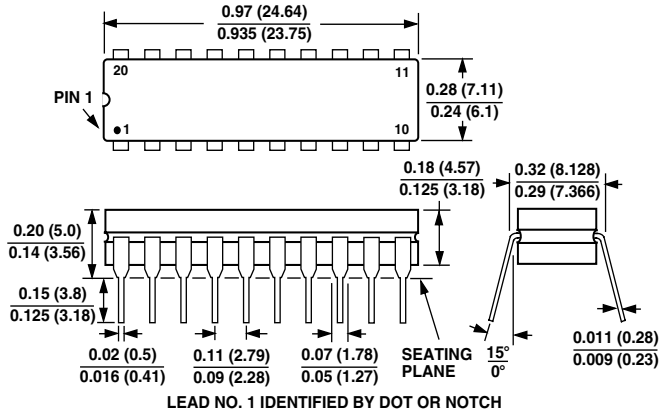

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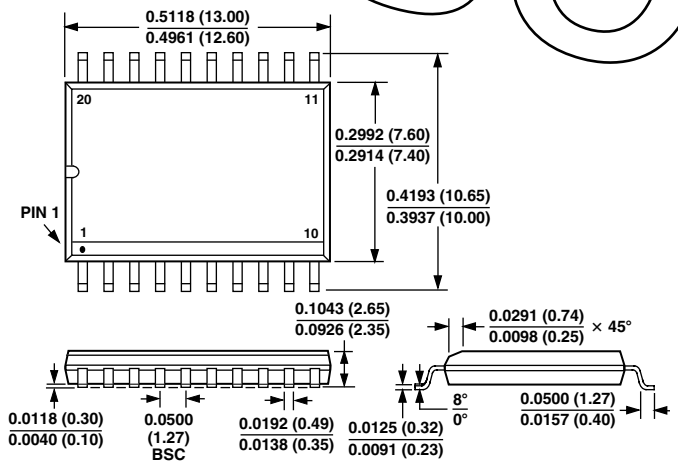
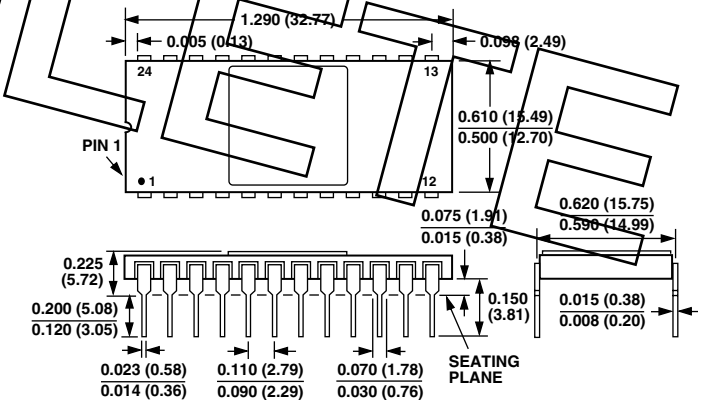
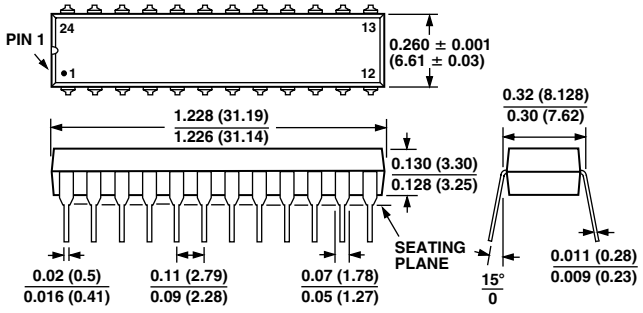


24-Lead Ceramic DIP (D-24)

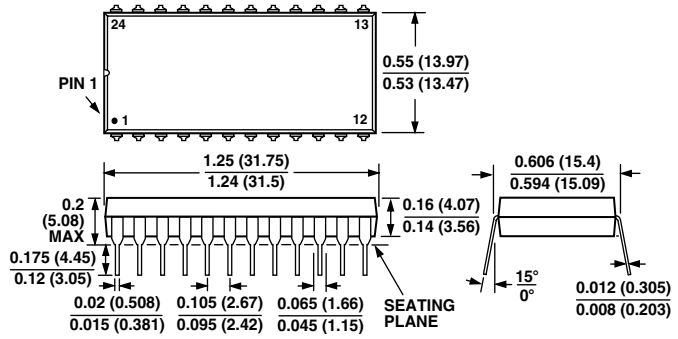


24-Lead Plastic DIP (N-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

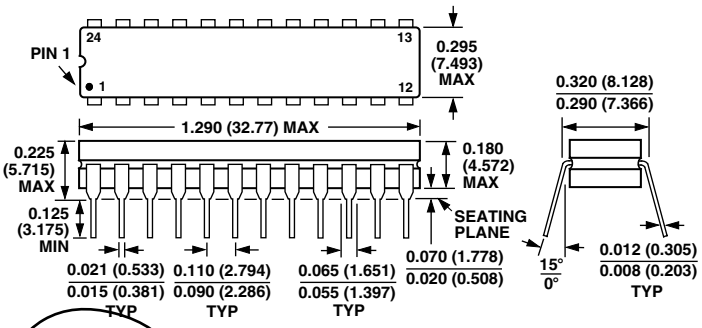
24-Lead Plastic DIP (N-24A)



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Cerdip (Q-24)



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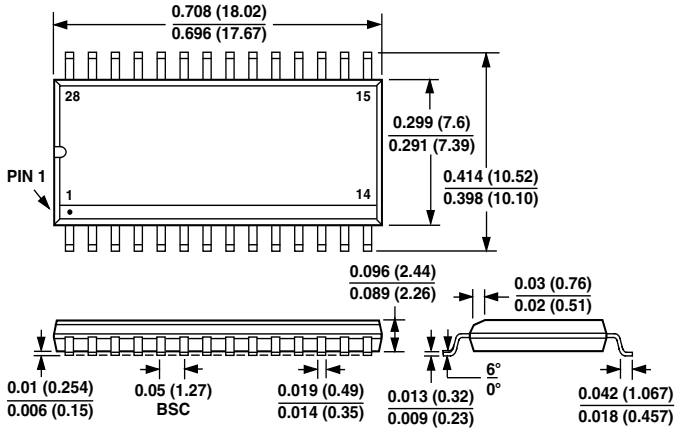
28-Lead SOIC (R-28)



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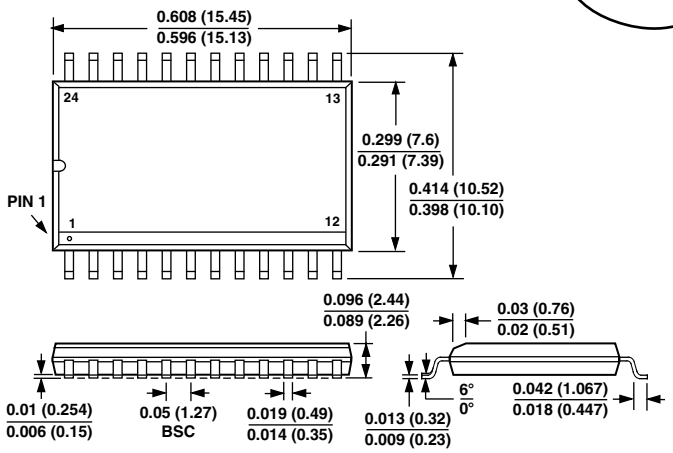
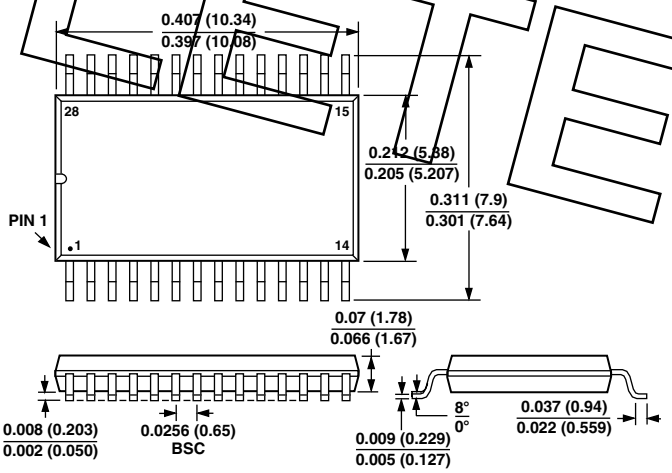
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead SOIC (R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

28-Lead SSOP (RS-28)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

ADM223/ADM230L–ADM241L–Revision History

Location **Page**

05/01

Data Sheet changed from REV. A to REV. B.

Edits to Test Conditions/Comments of Specifications 2

Location **Page**

01/01

Data Sheet changed from REV. 0 to REV. A.

Removed ESD information from FEATURES 1

SPECIFICATIONS changes 2

Removed ESD information from ABSOLUTE MAXIMUM RATINGS 2

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