Data Sheet

ADMV4821

24 GHz to 29.5 GHz Transmitter/Receiver, Dual Polarization Beamformer

FEATURES

- RF frequency range: 24 GHz to 29.5 GHz
- 16 configurable transmit channels
- 16 configurable receive channels
- Dual polarization: 8 horizontal and 8 vertical channels
- Fast TDD switching time using external pins
- Matched, 50 Ω, single-ended RF inputs and outputs
- Integrated transmitter power detectors and temperature sensor
- High resolution, 6-bit vector modulators for phase control
- High resolution, 6-bit and 5-bit DVGAs for amplitude control
- Gain compensation over temperature
- Memory for 256 beam positions
- Single power supply required: 3.3 V with on-chip LDO regulator for 1.8 V
- Adjustable power modes for power consumption reduction
- 3-wire or 4-wire SPI supporting up to a 61.44 MHz SPI clock speed
- 72-terminal, 10 mm × 10 mm, LGA package

APPLICATIONS

- 5G applications
- Broadband communication
- Test and measurement
- Aerospace and defense

GENERAL DESCRIPTION

The ADMV4821 is a silicon germanium (SiGe), 24 GHz millimeter-wave (mmW) to 29.5 GHz mmW 5G beamformer. The RF IC is highly integrated and contains 16 independent channels with both transmit and receive functionality. The ADMV4821 supports eight horizontal and eight vertical polarized antennas via the independent RFV and RFH inputs/outputs common pins.

In transmit mode, both the RFV and RFH input signals are split via two independent 1:8 power splitters and pass through the eight, independent, corresponding transmit channels. In this mode, each channel includes a vector modulator (VM) to control the phase and two digital variable gain amplifiers (DVGAs) to control the amplitude.

In receive mode, input signals pass through two sets of eight receive channels (either vertical or horizontal) and are combined via one independent 8:1 combiner connected to the RFV pin and one independent 8:1 combiner connected to the RFH pin. In this mode, each channel includes a VM to control the phase and a DVGA to control the amplitude.

The VM provides a full 360° phase adjustment range in either transmit or receive mode. The VM provides six bits of resolution for 5.625° phase steps.

In transmit mode, the total DVGA dynamic range adjustment range is 32.4 dB. The DVGAs provide five bits or six bits of resolution, resulting in 1.0 dB or 0.5 dB amplitude steps, respectively.

In receive mode, the DVGA allows for 17.1 dB of dynamic range adjustment. The DVGA also provides six bits of resolution, resulting in 0.5 dB amplitude steps. The DVGAs provide a flat phase response across the full gain range.

The transmitter channels contain individual power detectors to detect and calibrate the gain for each channel as well as the channel to channel gain mismatch. Directly connect the ADMV4821 RF ports to a patch antenna to create a dual polarization mmW 5G subarray.

Users can program the ADMV4821 by using a 3-wire or 4-wire serial port interface (SPI). The integrated on-chip low dropout (LDO) regulator generates the 1.8 V supply for the SPI circuitry to reduce the number of supply domains required. There are various SPI modes to enable fast startup and control during normal operation.

Users can either set the amplitude and phase for each channel individually or program multiple channels simultaneously by using the on-chip memory for beamforming. The on-chip memory can store up to 256 beam positions, which can be allocated for either transmitter or receiver mode in any combination. In addition, four address pins allow SPI control of up to 16 devices on the same serial lines. Dedicated horizontal and vertical polarization load pins also synchronize all devices in the same array. There is a horizontal and vertical polarization transmit and receive mode control pins (TRXV and TRXH) for fast switching between transmit and receive mode.

The ADMV4821 comes in a compact, thermally enhanced 10 mm × 10 mm, RoHs compliant land grid array (LGA) package. The ADMV4821 operates over the −40°C to +95°C case temperature range. This LGA package allows users to heat-sink the ADMV4821 from the top side of the package for the most efficient thermal heatsinking and to allow flexible antenna placement on the opposite side of the printed circuit board (PCB).

Throughout the figures in this data sheet, Tx means transmit (or transmitter) and Rx means receive (or receiver).

Rev. B

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REVISION HISTORY

3/2022—Revision B: Initial Version

FUNCTIONAL BLOCK DIAGRAM

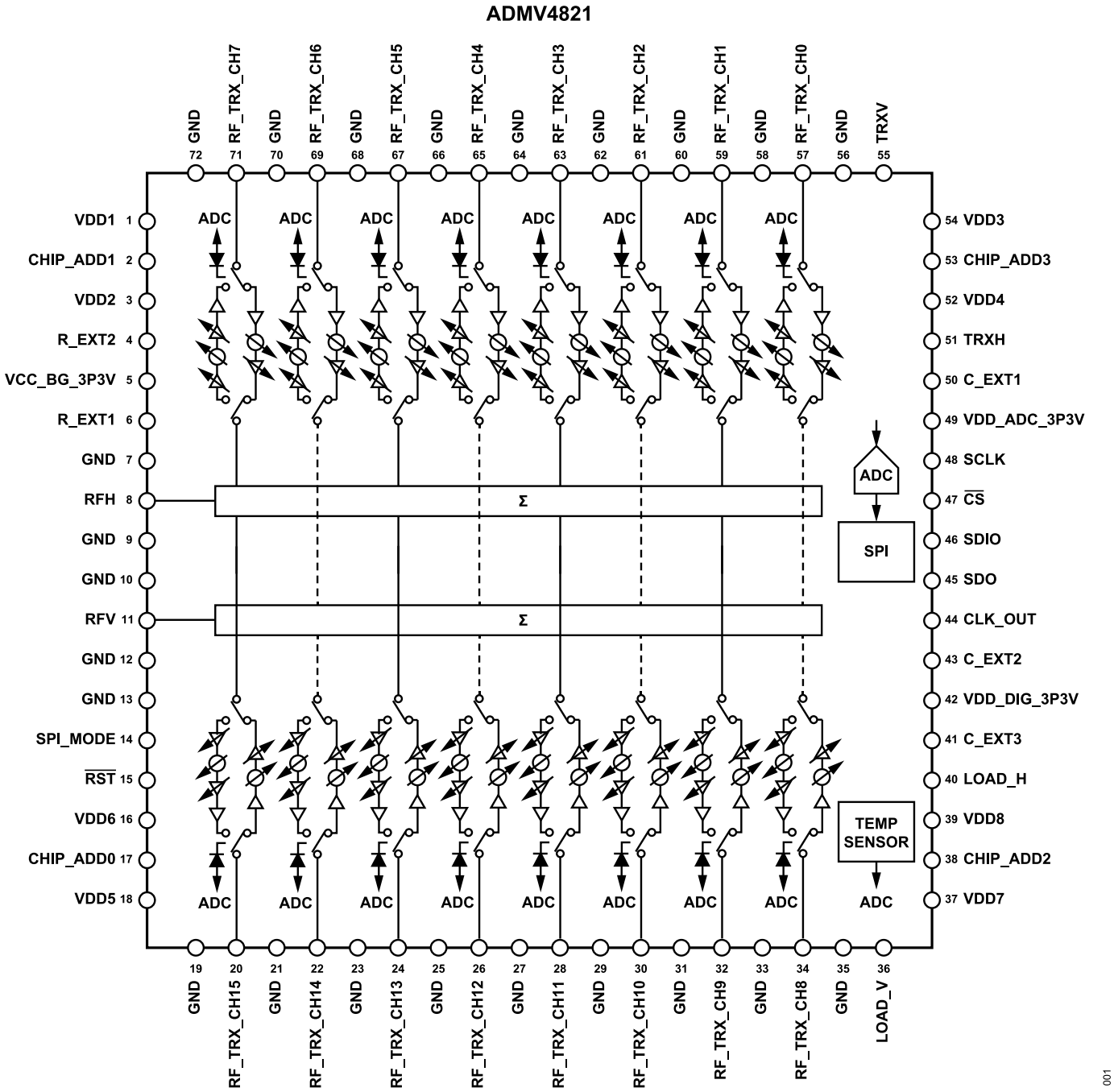

Figure 1.

SPECIFICATIONS

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* and the case temperature, which is referenced to the topside of package (T_C), = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
RF Range		24		29.5	GHz
Operating Temperature		−40		+95	°C
POWER SUPPLY					
Voltage Range		3.15	3.3	3.45	V
Transmit Mode	16 channels active				
VDDx[1] Current			1826		mA
VCC_BG_3P3V Current			45		mA
VDD_DIG_3P3V Current			9		mA
VDD_ADC_3P3V Current			16		mA
Receive Mode	16 channels active				
VDDx Current			998		mA
VCC_BG_3P3V Current			45		mA
VDD_DIG_3P3V Current			8		mA
VDD_ADC_3P3V Current			15		mA
TRANSMITTER AND RECEIVER SECTION					
Impedance			50		Ω
Number of Channels			16		
Phase Accuracy	Using 6 bits of control		5.625		Degrees
Gain Variation	Due to phase setting		0.6	1	dB
Phase RMS Error			1.5	3	Degrees
Phase Variation	Due to gain setting		±2.0		Degrees
Gain Flatness					
Across 100 MHz Bandwidth			±0.13		dB
Across 800 MHz Bandwidth			±0.35		dB
Across 3000 MHz Bandwidth			±0.7		dB
Gain/Phase Settling Time			30		ns
Time Division Duplex (TDD) Switching Time					
Transmitter Off to Receiver On			120		ns
Receiver Off to Transmitter On			60		ns
TEMPERATURE SENSOR					
Range		−40		+125	°C
Slope	LSB in decimal		0.93		LSB/°C
Resolution			8		Bits

[1] Where x = 1 to 8.

TRANSMITTER SPECIFICATIONS

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, and T_C = 25°C, unless otherwise noted.

Measurements performed in transmit mode, RF amplitude = −20 dBm, and the channel Digital Variable Gain Amplifier 1 (DVGA 1) and common Digital Variable Gain Amplifier 2 (DVGA 2) set to the maximum gain.

SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TRANSMITTER					
Output 1 dB Compression Point (P1dB)		14	17.5		dBm
Output Third-Order Intercept Point (IP3)	100 MHz tone spacing		26		dBm
Gain	Includes splitting losses	16	25		dB
Gain Dynamic Range		30	32.4		dB
Gain Step					
DVGA 1	Using 6 bits of control		0.5		dB
DVGA 2	Using 5 bits of control		1.0		dB
Gain Error			±0.1		dB
Input Return Loss			−10		dB
Output Return Loss			−8		dB
Noise Figure			27.3		dB
Power Consumption per Channel					
Nominal Power Mode					
At P1dB	Output power = 17.5 dBm		0.66		W
Backoff from P1dB	Output power = 0 dBm		0.40		W
Medium Power Mode					
At P1dB	Output power = 17.5dBm		0.57		W
Backoff from P1dB	Output power = 0 dBm		0.32		W
Low Power Mode					
At P1dB	Output power = 15.9 dBm		0.44		W
Backoff from P1dB	Output power = 0 dBm		0.24		W
POWER DETECTOR					
Output Power Range			±15		dBm
Power Detector Range[1]			30		dB
Resolution			6		Bits

[1] Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* (contact Analog Devices at mmwave5G@analog.com) for more details regarding specific ranges that can be programmed via the SPI.

RECEIVER SPECIFICATIONS

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, and T_C = 25°C, unless otherwise noted.

Measurements performed in receive mode, RF amplitude = −30 dBm, and receiver DVGA set to maximum gain, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RECEIVER					
Single-Channel Noise Figure					
8 Channels Active, Single Input			15.2		dB
1 Channel Active[1], Single Input			6.2		dB
Input P1dB		−23.5	−20.5		dBm
Input IP3	100 MHz tone spacing		−12.7		dBm
Electrical Gain (EG)[2]	8 channels active		20.6		dB
Single Channel Gain (SCG)	1 channel active	5	11.6		dB
Gain Dynamic Range			17.1		dB
Gain Step	Using 6 bits of control		0.5		dB

SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Gain Step Error			±0.1		dB
Input Return Loss			−11		dB
Output Return Loss			−10		dB
Power Consumption Per Channel					
Nominal Power Mode			0.22		W
Medium Power Mode			0.21		W
Low Power Mode			0.16		W

[1] The single-channel noise figure is calculated based on the following equations: SCNFM = SCNF1 + 10 × log(M), where SCNFM is the single-channel noise figure measured when M channels are active.

[2] Electrical gain (EG) is calculated based on EG = SCG + SPL where SCG is the single channel gain when one channel is active and SPL, the ideal splitter network losses, is represented by 10 × log(N) where N is the number of summations. In the case of the ADMV4821, SPL is 9 due to the 8:1 sum splitter. The EG value is typically used for cascade noise figure and gain calculations. Coherent gain (CG) is calculated based on CG = EG + 10 × log(M), where EG is the electrical gain and M is the number of channels active.

SERIAL PORT INTERFACE (SPI)

Refer to the SPI Information section for full details.

Table 4. Logic Input and Output Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS	CHIP_ADD0 to CHIP_ADD3, SPI_MODE, $\overline{RST}$, LOAD_x[1], SDIO, $\overline{CS}$, SCLK, and TRXx[1]				
Input Voltage					
High (V_{IH})		1.2	1.8		V
Low (V_{IL})			0	0.63	V
High and Low Input Current (I_{INH}, I_{INL})			7		µA
Input Capacitance (C_{IN})			0.4		pF
LOGIC OUTPUTS	CLK_OUT, SDO, and SDIO				
Output Voltage					
High (V_{OH})	Output high current (I_{OH}) = 8 mA	1.35			V
Low (V_{OL})	Output low current (I_{OL}) = 8 mA			0.45	V

[1] Where x is either V or H.

Table 5. Timing Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Maximum SCLK Rate (t_{SCLK})					
SRAM Write				61.44	MHz
SRAM Read				61.44	MHz
Register Write				61.44	MHz
Register Read				30.72	MHz
	With first data bit double clocked			61.44	MHz
Pulse Width					
SCLK Minimum Pulse Width					
High (t_{HIGH})			4		ns
Low (t_{LOW})			4		ns
$\overline{CS}$ Minimum Pulse Width High	Between two writes or reads		3		ns
$\overline{RST}$ Minimum Pulse Width Low			2.5		ns
LOAD_V Minimum Pulse Width					

SPECIFICATIONS

Table 5. Timing Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
High			5.5		ns
Low			3.1		ns
Minimum Setup Time					
$\overline{CS}$ to SCLK (t_S)			1.0		ns
SDIO to SCLK (t_{DS})			1.0		ns
Minimum Hold Time					
SCLK to $\overline{CS}$ (t_H)	Falling SCLK edge, see Figure 80		0.8		ns
SCLK to SDIO (t_{DH})			2.8		ns
SDO					
Data Valid, SDO to SCLK (t_{DV})	Falling SCLK edge, see Figure 81		6.0		ns
Rise Time	10% to 90%		2.0		ns
Fall Time	90% to 10%		2.6		ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage	
VDD1 to VDD8, VDD_DIG_3P3V, VCC_BG_3P3V, VDD_ADC_3P3V	3.6 V
Digital Input/Output Voltages	
Logic Input Low	0.63 V
Logic Input High	1.95 V
RF Input Power	0 dBm
Maximum Junction Temperature	125°C
Maximum Power Dissipation[1]	25 W
Lifetime at Maximum Junction Temperature (T_J)	1×10^6 hours
Operating Case Temperature Range	−40°C to +95°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering 60 sec)	260°C
Moisture Sensitivity Level (MSL) Rating[2]	MSL3
Topside Force Ratings	
One Time Maximum	5.44 kgf
Constant	1 kgf
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	3.5 kV
Field Induced Charged Device Model (FICDM)	750 V

[1] The maximum power dissipation is a theoretical number calculated by (T_J − 95°C)/θ_{JC_TOP}.

[2] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Only use θ_{JA} and θ_{JC} to compare the thermal performance of different packages when all test conditions listed are similar to the JEDEC specifications. Otherwise, use Ψ_{JT} and Ψ_{JB} to calculate the device junction temperature using the following equations:

$$T_J = \left(P \times \Psi_{JT}\right) + T_{TOP} \quad (1)$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JT} is the junction to top thermal characterization number.
T_{TOP} is the package top temperature (°C).
T_{TOP} is measured at the top center of the package.

$$T_J = \left(P \times \Psi_{JB}\right) + T_{BOARD} \quad (2)$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JB} is the junction to board thermal characterization number.
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package no more than 1 mm from the edge of the package body (°C).

As stated in JEDEC51-12, only use Equation 1 and Equation 2 when no heat sink or heat spreader is present. When a heat sink or heat spreader is added, use θ_{JC_TOP} to estimate or calculate the junction temperature. The preferred heat sink or heat spreader placement for this device is to contact the topside of the exposed pad of the device to the heatsink using an appropriate thermal grease to efficiently reduce the junction temperature of the device.

Table 7. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC_TOP}[3]	Ψ_{JT}[4]	Ψ_{JB}[5]	Unit
CC-72-3					
Transmit Mode	16.0	0.9	1.3	2.7	°C/W
Receive Mode	17.3	1.5	1.9	3.2	°C/W

[1] The thermal resistance values specified in Table 7 are simulated based on JEDEC specifications, unless specified otherwise, and must be used in compliance with JESD51-12.

[2] θ_{JA} is the junction to ambient thermal resistance in a natural convection, JEDEC environment.

[3] θ_{JC_TOP} is the junction to case (top) JEDEC thermal resistance.

[4] Ψ_{JT} is the junction to top JEDEC thermal characterization parameter.

[5] Ψ_{JB} is the junction to board JEDEC thermal characterization parameter.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

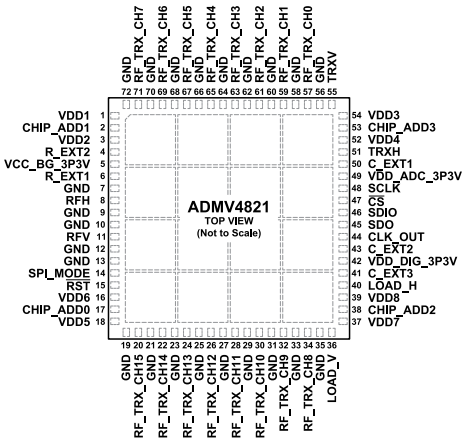

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD1	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
2	CHIP_ADD1	Chip Select Address Bit 1 Input (1.8 V CMOS Logic). Together with the CHIP_ADD0, CHIP_ADD2, and CHIP_ADD3 pins, this pin selects one of 16 devices to accept serial instructions and data. Under normal operating conditions, connect this pin to ground.
3	VDD2	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
4	R_EXT2	On-Chip LDO Regulator Circuit Connection. This pin requires a 1.1 kΩ series, <1%, high precision resistor connected to ground.
5	VCC_BG_3P3V	3.3 V Power Supply for Variable Gain Amplifier (VGA) Chip Band Gap Circuit. Place a 10 µF shunt capacitor to ground. Then, place a 0.01 µF shunt capacitor to ground, and then a shunt 100 pF capacitor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
6	R_EXT1	On-Chip LDO Regulator Circuit Connection. This pin requires a 1.1 kΩ series, <1%, high precision resistor connected to ground.
7, 9, 10, 12, 13, 19, 21, 23, 25, 27, 29, 31, 33, 35, 56, 58, 60, 62, 64, 66, 68, 70, 72	GND	Ground. Tie all ground pins and grounds together to a low impedance plane on the PCB.
8	RFH	Horizontal RF Input or Output. This pin is internally dc-coupled to ground and matches to 50 Ω, single-ended.
11	RFV	Vertical RF Input or Output. This pin is internally dc-coupled to ground and matches to 50 Ω, single-ended.
14	SPI_MODE	Standard SPI Mode Select Pin. Set this pin to logic low for standard SPI mode operation. For more information regarding the various SPI modes, refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*.
15	$\overline{\text{RST}}$	SPI Reset is an Active Low Interface. Connect this pin to logic high for normal operation. The SPI logic is 1.8 V.
16	VDD6	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
17	CHIP_ADD0	Chip Select Address Bit 0 Input (1.8 V CMOS Logic). Together with the CHIP_ADD1, CHIP_ADD2, and CHIP_ADD3 pins, this pin selects one of 16 devices to accept serial instructions and data. Under normal operating conditions, connect this pin to ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
18	VDD5	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
20	RF_TRX_CH15	Antenna Connection for Horizontal Channel 15 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
22	RF_TRX_CH14	Antenna Connection for Vertical Channel 14 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
24	RF_TRX_CH13	Antenna Connection for Horizontal Channel 13 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
26	RF_TRX_CH12	Antenna Connection for Vertical Channel 12 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
28	RF_TRX_CH11	Antenna Connection for Horizontal Channel 11 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
30	RF_TRX_CH10	Antenna Connection for Vertical Channel 10 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
32	RF_TRX_CH9	Antenna Connection for Horizontal Channel 9 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
34	RF_TRX_CH8	Antenna Connection for Vertical Channel 8 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
36	LOAD_V	Transmitter and Receiver Registers Load Input (1.8 V CMOS Logic) for Vertical Polarity Channels. Transitioning this pin from a logic low to a logic high three times causes values written to the corresponding registers, written since the last such load operation, to be fully loaded by the device.
37	VDD7	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
38	CHIP_ADD2	Chip Select Address Bit 2 Input (1.8 V CMOS Logic). Together with the CHIP_ADD0, CHIP_ADD1, and CHIP_ADD3 pins, this pin selects one of 16 devices to accept serial instructions and data. Under normal operating conditions, connect this pin to ground.
39	VDD8	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
40	LOAD_H	Transmitter and Receiver Registers Load Input (1.8 V CMOS Logic) for Horizontal Polarity Channels. Transitioning this pin from a logic low to a logic high three times causes values written to the corresponding registers, written since the last such load operation, to be fully loaded by the device.
41	C_EXT3	On-Chip 1.8 V Reference LDO Regulator Circuit Decoupling Pin Connection. This pin requires a series 3.3 µF capacitor in series with a 1.5 Ω resistor connected to ground. The voltage measured from this pin to ground is 1.8 V.
42	VDD_DIG_3P3V	3.3 V Power Supply for the LDO Regulator Circuit for Digital Circuitry. Place a 10 µF shunt capacitor to ground. Then, place a 0.01 µF shunt capacitor to ground, and then a 100 pF shunt capacitor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
43	C_EXT2	On-Chip 1.8 V Reference LDO Circuit Decoupling Pin Connection. This pin requires a series 3.3 µF capacitor in series with a 1.5 Ω resistor connected to ground. The voltage measured from this pin to ground is 1.8 V.
44	CLK_OUT	SPI Clock Output (1.8 V CMOS Logic). Under normal operating conditions, connect this pin to ground.
45	SDO	SPI Serial Data Output (1.8 V CMOS Logic). In 4-wire SPI mode, this pin is an SPI serial data output. In 3-wire SPI mode, this pin is unused and may be connected to ground.
46	SDIO	SPI Serial Data Input/Output (1.8 V CMOS Logic). In 4-wire SPI mode, this pin is an SPI serial data input. In 3-wire SPI mode, this pin is an SPI serial data input/output.
47	$\overline{CS}$	SPI Chip Select Input (1.8 V CMOS Logic). Serial communication is enabled when the $\overline{CS}$ pin is set to logic low. When the $\overline{CS}$ pin is set to logic high at the end of the serial data command, the data written to the register address is given in the command. For more information about using the $\overline{CS}$ pin in the various SPI modes, refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
48	SCLK	SPI Serial Clock Input (1.8 V CMOS Logic). In write mode, data is sampled on the rising edge of the SCLK pin. During a read cycle, output data changes at the falling edge of the SCLK pin.
49	VDD_ADC_3P3V	3.3 V Power Supply for the LDO Regulator Circuit for Digital Circuitry. Place a 10 µF shunt capacitor to ground. Then, place a 0.01 µF shunt capacitor to ground, and then a 100 pF shunt capacitor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
50	C_EXT1	On-Chip 1.8 V Reference LDO Regulator Circuit Decoupling Pin Connection. This pin requires a series 3.3 µF capacitor in series with a 1.5 Ω resistor connected to ground. The voltage measured from this pin to ground is 1.8 V.
51	TRXH	Transmit and Receive Mode Select Input for TDD Operation (1.8 V CMOS Logic). A rising edge of an input signal transitions the mode from receive to transmit. A falling edge of an input signal transitions the mode from transmit to receive. On startup, set this pin to logic low to ensure that the ADMV4821 starts up in receive mode.
52	VDD4	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
53	CHIP_ADD3	Chip Select Address Bit 3 Input (1.8 V CMOS Logic). Together with the CHIP_ADD0, CHIP_ADD1, and CHIP_ADD2 pins, this pin selects one of 16 devices to accept serial instructions and data. Under normal operating conditions, connect this pin to ground.
54	VDD3	3.3 V Power Supply for the RF Signal Paths. Place a 10 µF shunt capacitor in series with a 6.04 Ω resistor to ground. Then, place a 1 µF shunt capacitor in series with a 6.04 Ω resistor to ground, and then a shunt 0.15 µF capacitor in series with a 1.5 Ω resistor to ground, as close as possible to this pin. Refer to the ADMV4821-EVALZ user guide for component placement.
55	TRXV	Transmit and Receive Mode Select Input for TDD Operation of Vertical Polarity Channels (1.8 V CMOS Logic). A rising edge of an input signal transitions the mode from receive to transmit. A falling edge of an input signal transitions the mode from transmit to receive. On startup, set this pin to logic low to ensure the ADMV4821 starts in receive mode.
57	RF_TRX_CH0	Antenna Connection for Vertical Channel 0 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
59	RF_TRX_CH1	Antenna Connection for Horizontal Channel 1 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
61	RF_TRX_CH2	Antenna Connection for Vertical Channel 2 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
63	RF_TRX_CH3	Antenna Connection for Horizontal Channel 3 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
65	RF_TRX_CH4	Antenna Connection for Vertical Channel 4 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
67	RF_TRX_CH5	Antenna Connection for Horizontal Channel 5 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
69	RF_TRX_CH6	Antenna Connection for Vertical Channel 6 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
71	RF_TRX_CH7	Antenna Connection for Horizontal Channel 7 Input or Output in Either Receive or Transmit Mode. This pin is dc-coupled and matched to 50 Ω, single-ended.
	EPAD (backside)	Exposed Pad. Connect the exposed pad and all GND connections to a low impedance ground plane on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSMIT MODE

VDD1 to VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set SPI values based on the start-up sequence in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, T_C = 25°C, RF amplitude = −20 dBm, and set DVGA 1 and DVGA 2 to the maximum gain, unless otherwise noted.

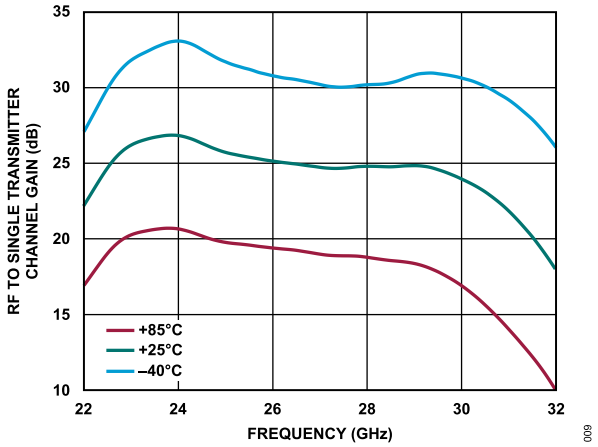

Figure 3. RF to Single Transmitter Channel Gain vs. Frequency at Various Temperatures at Maximum Gain

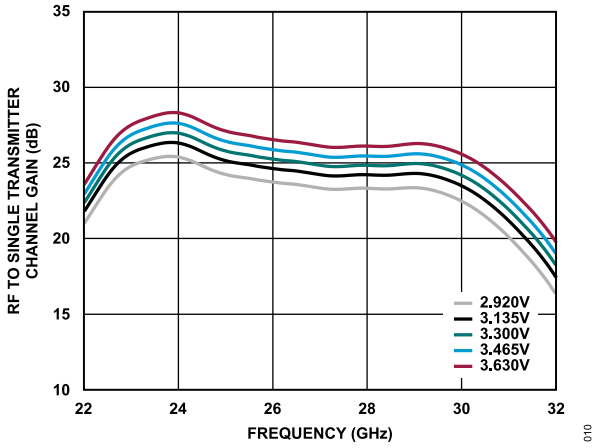

Figure 4. RF to Single Transmitter Channel Gain vs. Frequency at Various Supply Voltages at Maximum Gain

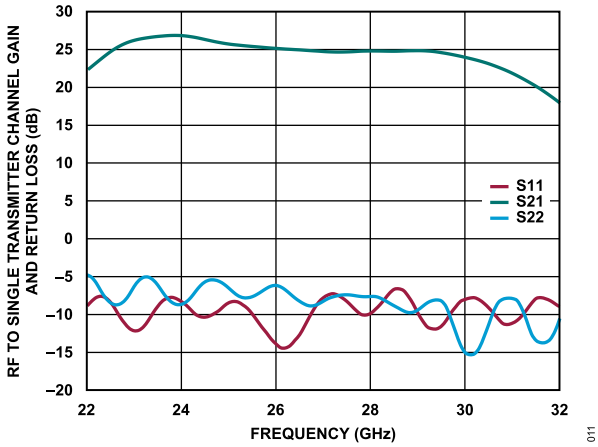

Figure 5. RF to Single Transmitter Channel Gain and Return Loss vs. Frequency at Maximum Gain

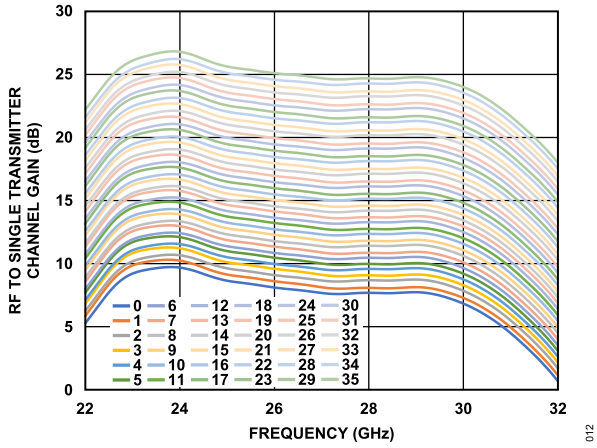

Figure 6. RF to Single Transmitter Channel Gain vs. Frequency at Various DVGA 1 Settings from 0 to 35

TYPICAL PERFORMANCE CHARACTERISTICS

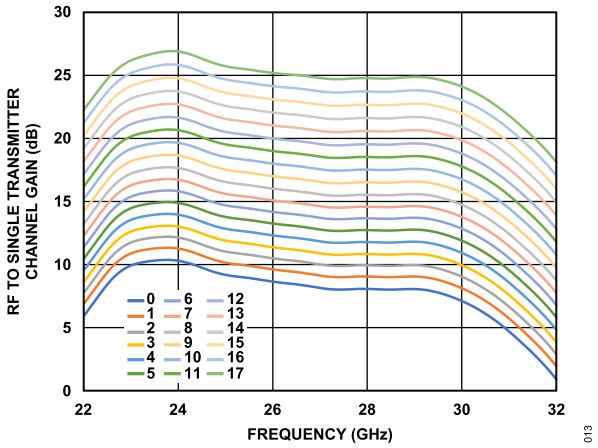

Figure 7. RF to Single Transmitter Channel Gain vs. Frequency at Various DVGA 2 Settings from 0 to 17

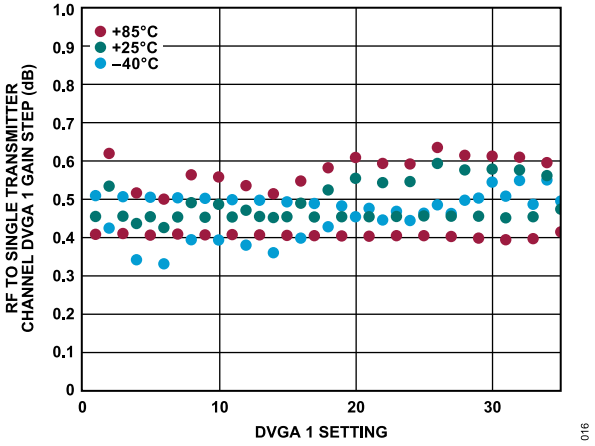

Figure 10. RF to Single Transmitter Channel DVGA 1 Gain Step vs. DVGA 1 Setting from 0 to 35 over Various Temperatures at 27 GHz

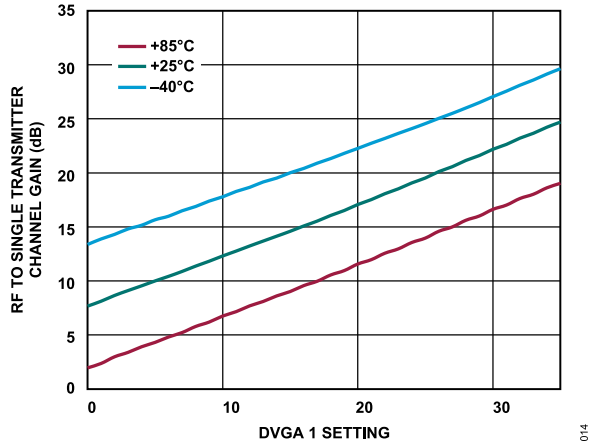

Figure 8. RF to Single Transmitter Channel Gain vs. DVGA 1 Setting from 0 to 35 over Various Temperatures at 27 GHz

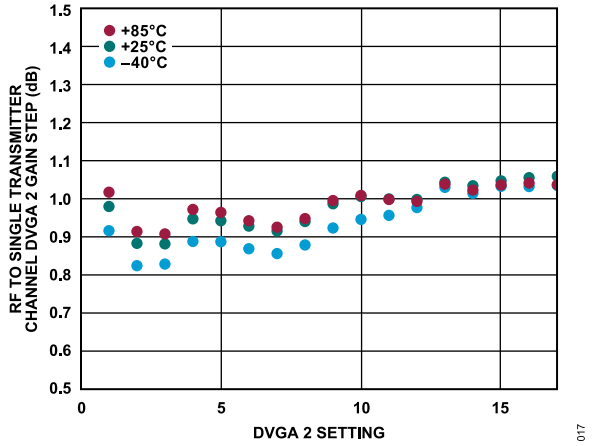

Figure 11. RF to Single Transmitter Channel DVGA 2 Gain Step vs. DVGA 2 Setting from 0 to 17 over Various Temperatures at 27 GHz

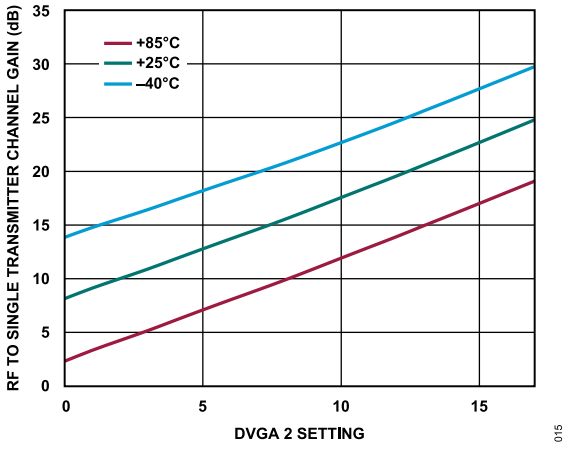

Figure 9. RF to Single Transmitter Channel Gain vs. DVGA 2 Setting from 0 to 17 over Various Temperatures at 27 GHz

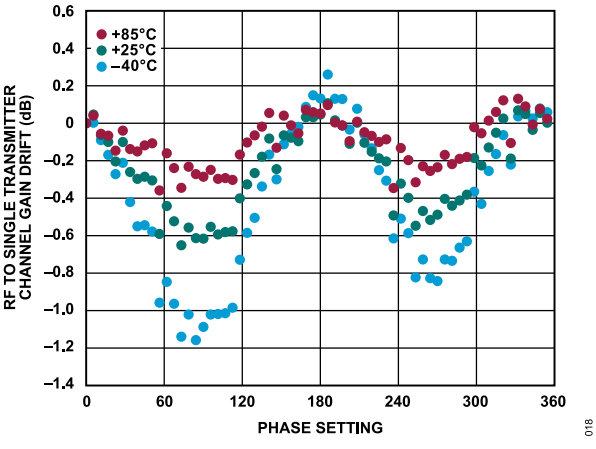

Figure 12. RF to Single Transmitter Channel Gain Drift vs. Phase Setting from 0° to 360° over Temperature at 27 GHz, Set to Maximum Gain

TYPICAL PERFORMANCE CHARACTERISTICS

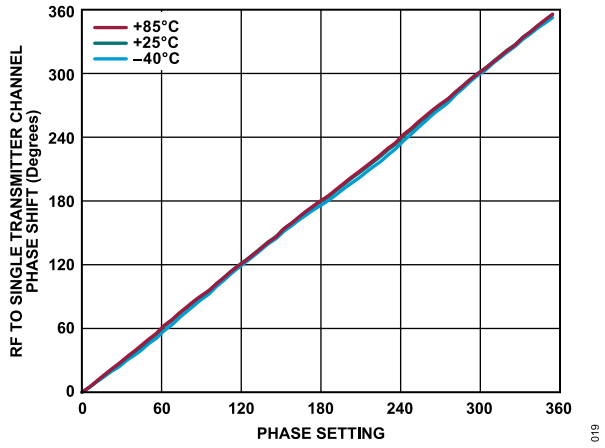

Figure 13. RF to Single Transmitter Channel Phase Shift vs. Phase Setting from 0° to 360° over Various Temperatures at 27 GHz, Set to Maximum Gain

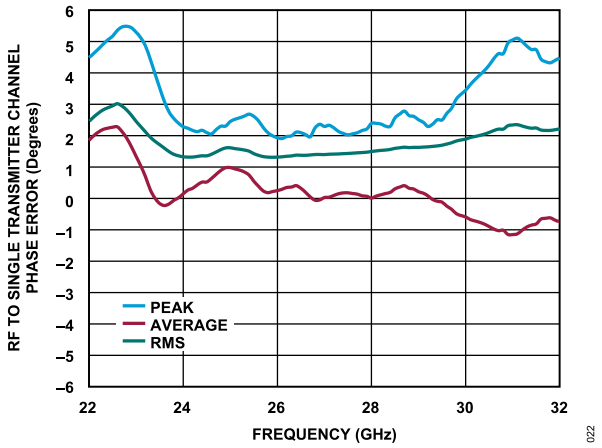

Figure 16. RF to Single Transmitter Channel Phase Error vs. Frequency for Peak, Average, and RMS Error

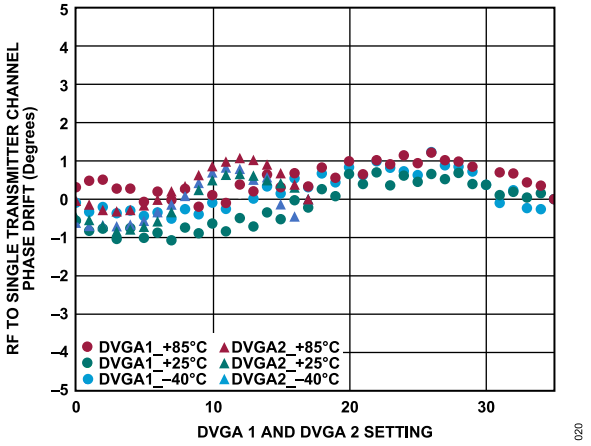

Figure 14. RF to Single Transmitter Channel Phase Drift vs. DVGA 1 Setting from 0 to 35 and DVGA 2 Setting from 0 to 17, over Various Temperatures at 27 GHz

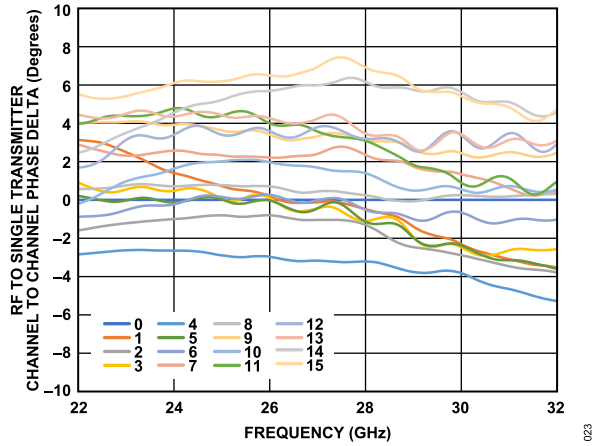

Figure 17. RF to Single Transmitter Channel to Channel Phase Delta vs. Frequency at Maximum Gain, Where Numbers in Legend Are Channel Numbers

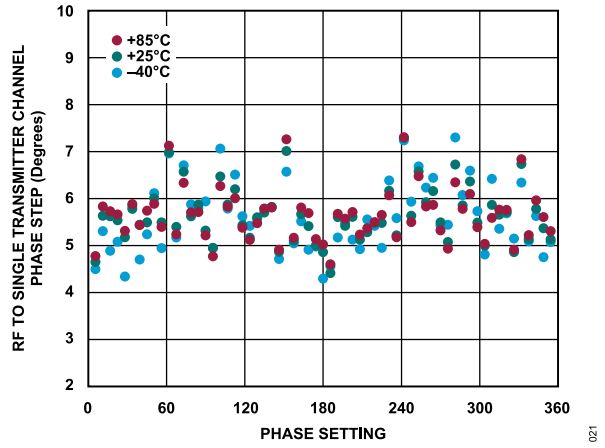

Figure 15. RF to Single Transmitter Channel Phase Step vs. Phase Setting from 0° to 360° over Various Temperatures at 27 GHz, Set to Maximum Gain, Nominal Step 5.625°

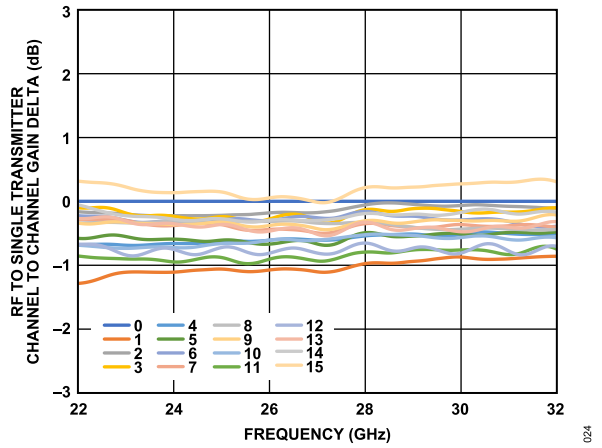

Figure 18. RF to Single Transmitter Channel to Channel Gain Delta vs. Frequency at Maximum Gain, Where Numbers in Legend Are Channel Numbers

TYPICAL PERFORMANCE CHARACTERISTICS

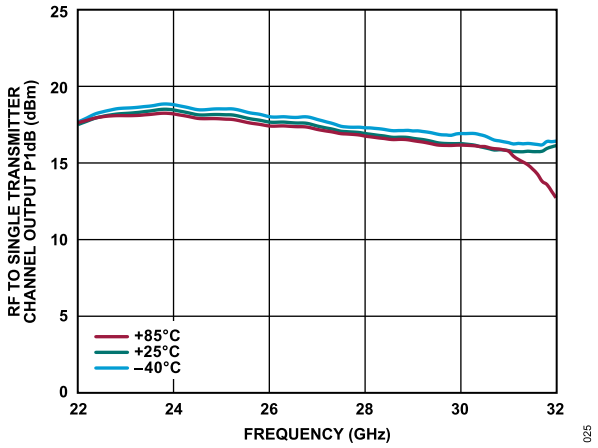

Figure 19. RF to Single Transmitter Channel Output P1dB vs. Frequency at Various Temperatures at Maximum Gain

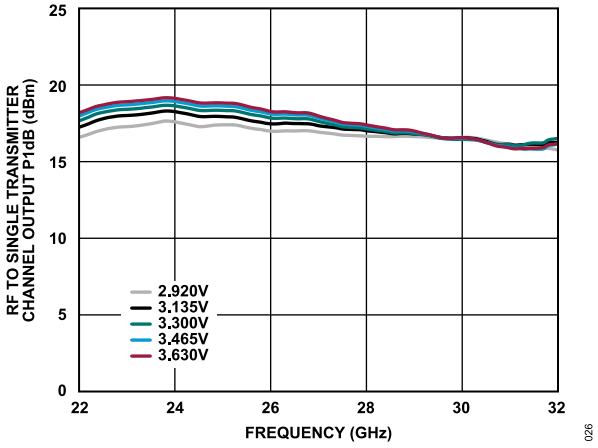

Figure 20. RF to Single Transmitter Channel Output P1dB vs. Frequency at Various Supply Voltages at Maximum Gain

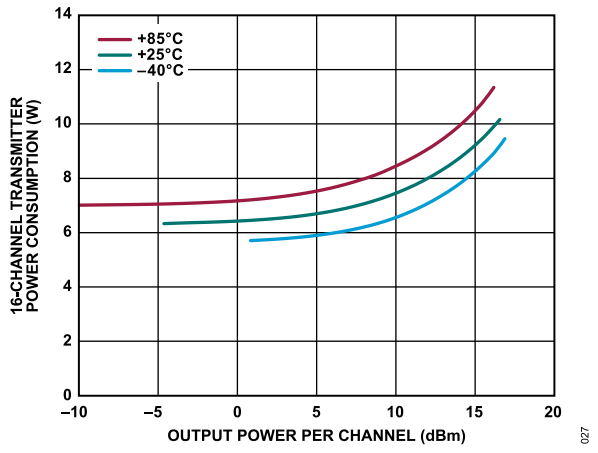

Figure 21. 16-Channel Transmitter Power Consumption vs. Output Power per Channel at Various Temperatures at Maximum Gain

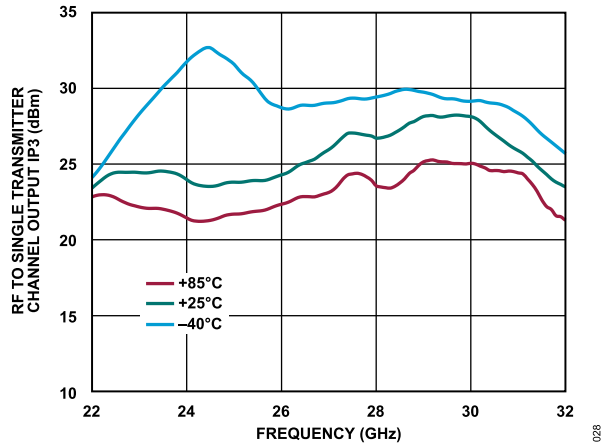

Figure 22. RF to Single Transmitter Channel Output IP3 vs. Frequency at Various Temperatures at Maximum Gain

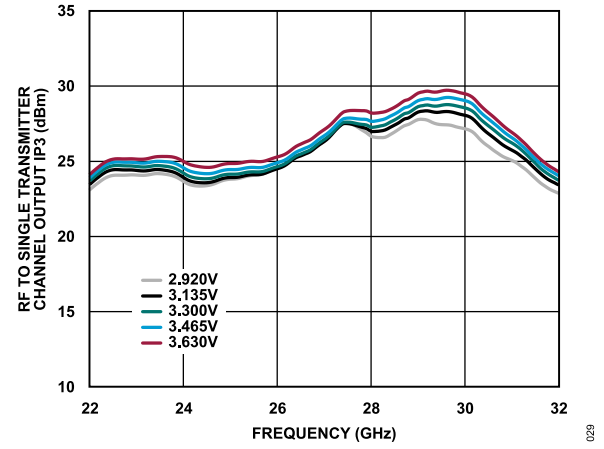

Figure 23. RF to Single Transmitter Channel Output IP3 vs. Frequency at Various Supply Voltages at Maximum Gain

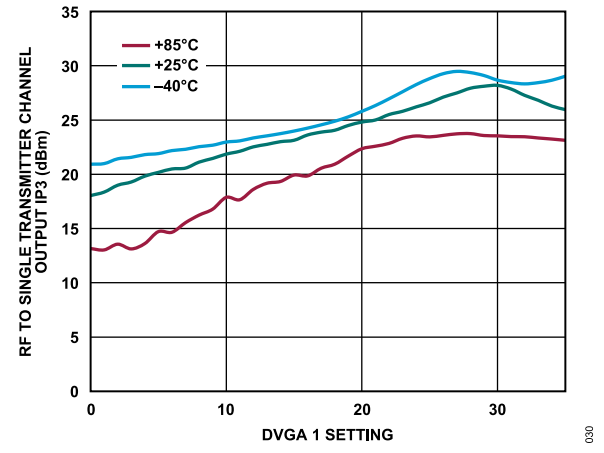

Figure 24. RF to Single Transmitter Channel Output IP3 vs. DVGA 1 Setting from 0 to 35 over Various Temperatures at 27 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

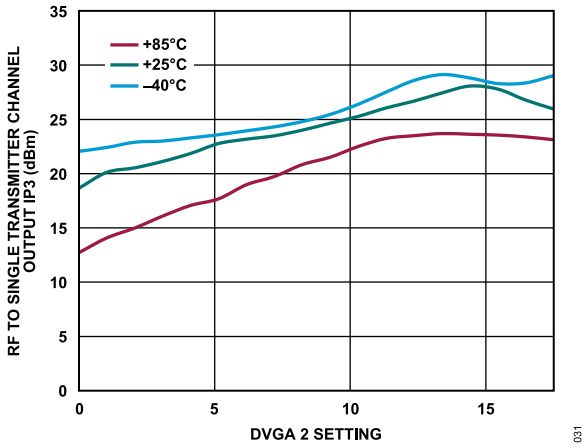

Figure 25. RF to Single Transmitter Channel Output IP3 vs. DVGA 2 Setting from 0 to 17 over Various Temperatures at 27 GHz

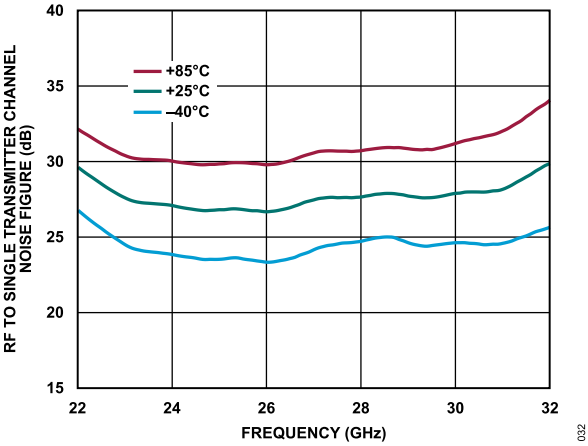

Figure 26. RF to Single Transmitter Channel Noise Figure vs. Frequency at Various Temperatures at Maximum Gain

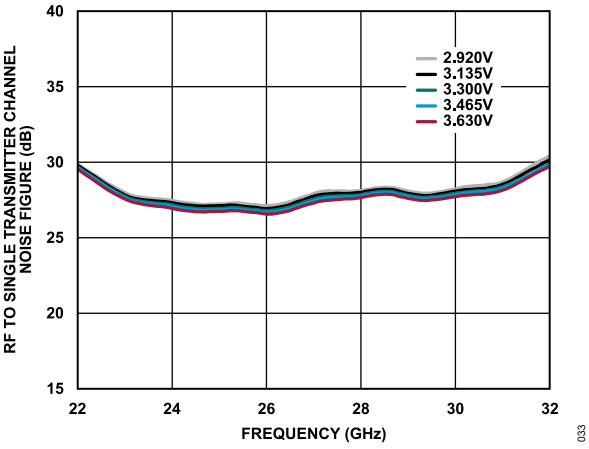

Figure 27. RF to Single Transmitter Channel Noise Figure vs. Frequency at Various Supply Voltages at Maximum Gain

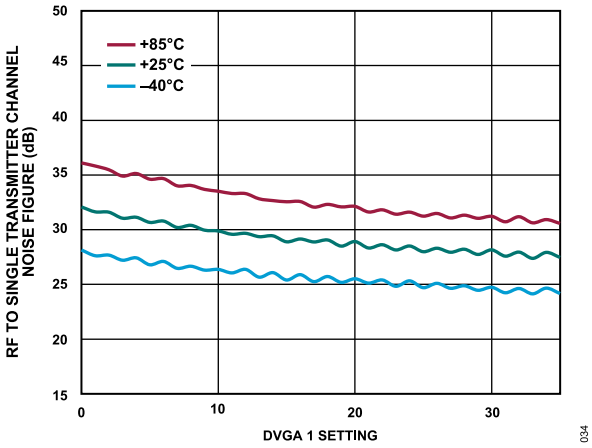

Figure 28. RF to Single Transmitter Channel Noise Figure vs. DVGA 1 Setting from 0 to 35 over Various Temperatures at 27 GHz

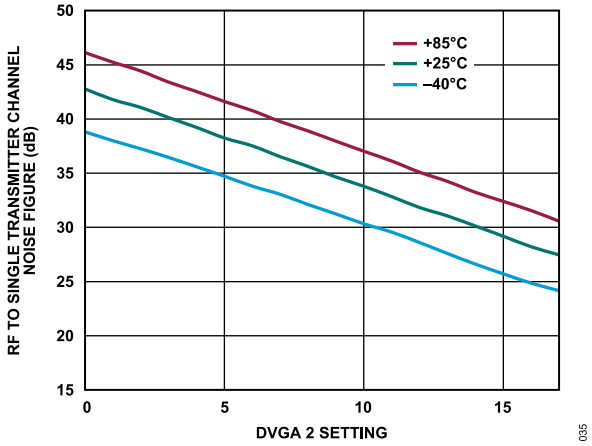

Figure 29. RF to Single Transmitter Channel Noise Figure vs. DVGA 2 Setting from 0 to 17 over Various Temperatures at 27 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

POWER DETECTOR PERFORMANCE

VDD1 to VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, T_C = 25°C, RF amplitude = −20 dBm, and set DVGA 1 and DVGA 2 to the maximum gain, unless otherwise noted. The detector range settings are written to Register 0x027, Bits[6:0].

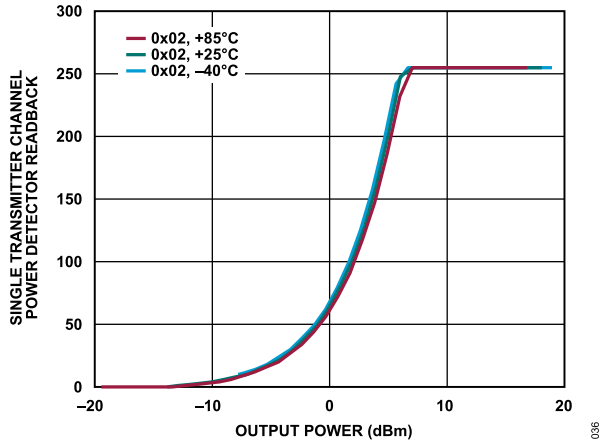

Figure 30. Single Transmitter Channel Power Detector Readback vs. Output Power at Various Temperatures at 27 GHz, Set to Maximum Gain, Detector Range Set to 0x02

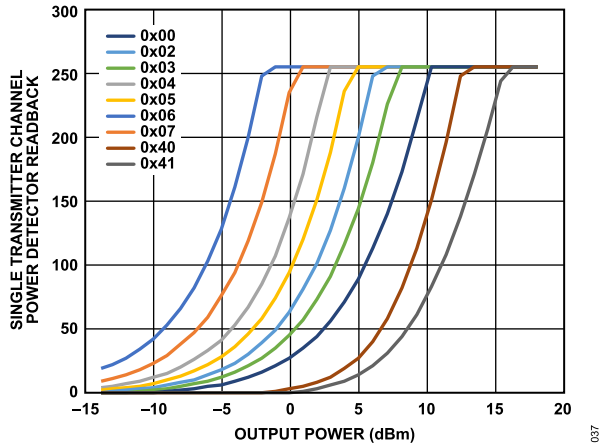

Figure 31. Single Transmitter Channel Power Detector Readback vs. Output Power at Various Detector Range Settings at 27 GHz, Set to Maximum Gain

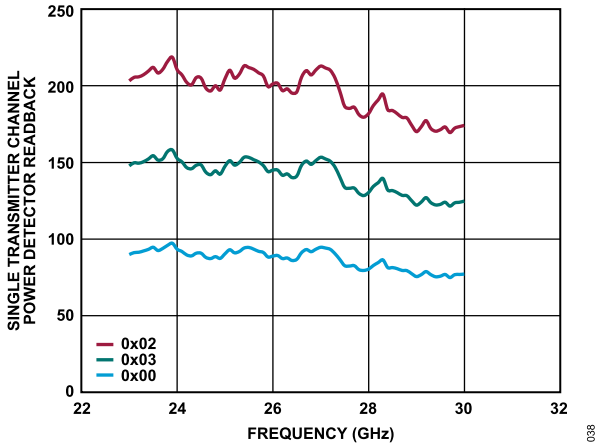

Figure 32. Single Transmitter Channel Power Detector Readback vs. Frequency at Various Detector Range Settings, Set to Maximum Gain, Input Power = 5 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVER TO TRANSMITTER SWITCHING SPEED AND AMPLITUDE/PHASE SETTLING TIME

VDD1 to VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, T_C = 25°C, RF amplitude = −20 dBm, and set DVGA 1 and DVGA 2 to the maximum gain, unless otherwise noted.

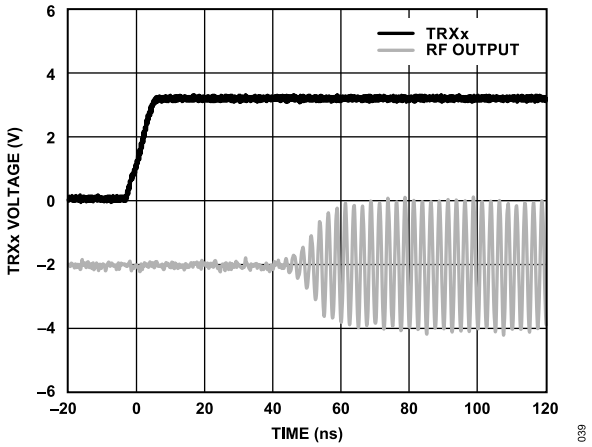

Figure 33. Receiver to Transmitter Mode Switching Time

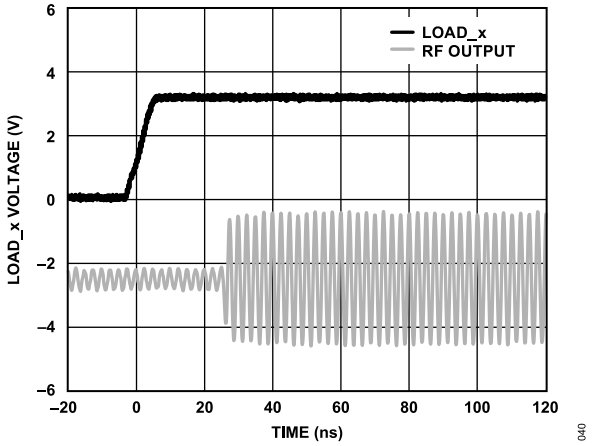

Figure 34. Gain Settling Time

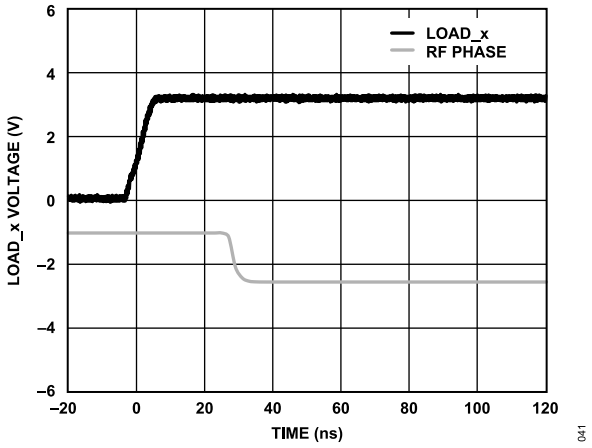

Figure 35. RF Phase Settling Time

TYPICAL PERFORMANCE CHARACTERISTICS

Transmitter RFV to RFH Plane Isolation Performance

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, and T_C = 25°C, unless otherwise noted. Measurements are performed in receive mode, RF amplitude = −30 dBm, and set DVGA 1 and DVGA 2 to maximum gain, unless otherwise noted.

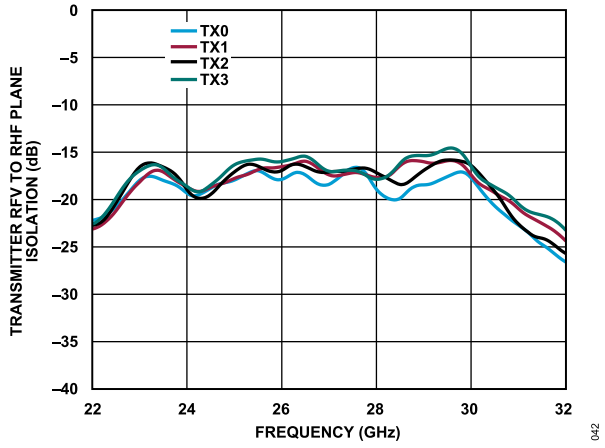

Figure 36. Transmitter RFV to RFH Plane Isolation vs. Frequency for Transmitter 0 (TX0), Transmitter 1 (TX1), Transmitter 2 (TX2), and Transmitter 3 (TX3)

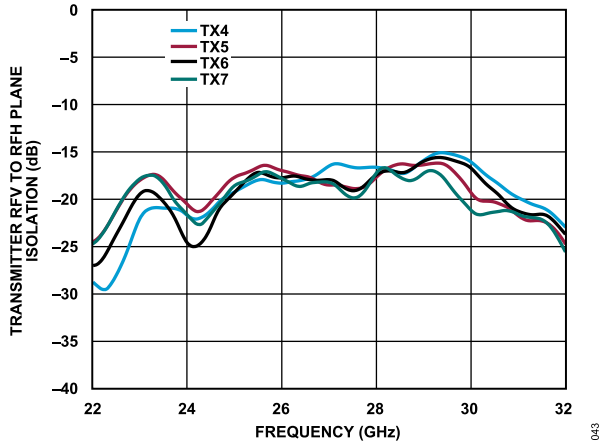

Figure 37. Transmitter RFV to RFH Plane Isolation vs. Frequency for Transmitter 2 (TX4), Transmitter 5 (TX5), Transmitter 6 (TX6), and Transmitter 7 (TX7)

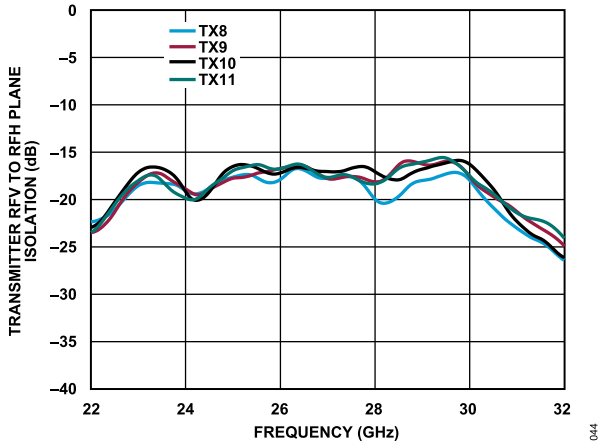

Figure 38. Transmitter RFV to RFH Plane Isolation vs. Frequency for Transmitter 8 (TX8), Transmitter 9 (TX9), Transmitter 10 (TX10), and Transmitter 11 (TX11)

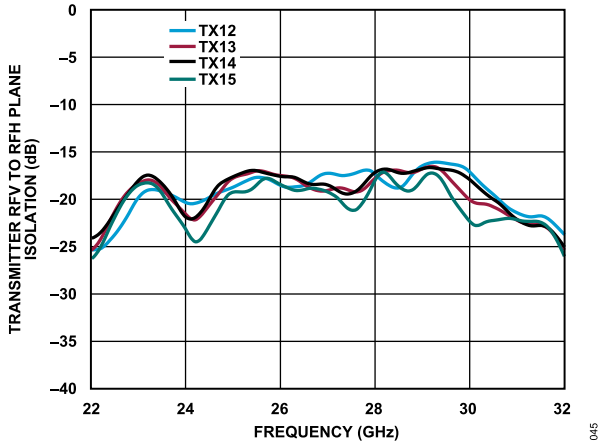

Figure 39. Transmitter RFV to RFH Plane Isolation vs. Frequency for Transmitter 12 (TX12), Transmitter 13 (TX13), Transmitter 14 (TX14), and Transmitter 15 (TX15)

TYPICAL PERFORMANCE CHARACTERISTICS

Transmitter Reverse Isolation Performance

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, and T_C = 25°C, unless otherwise noted. Measurements are performed in receive mode, RF amplitude = −30 dBm, and set DVGA 1 and DVGA 2 to maximum gain, unless otherwise noted.

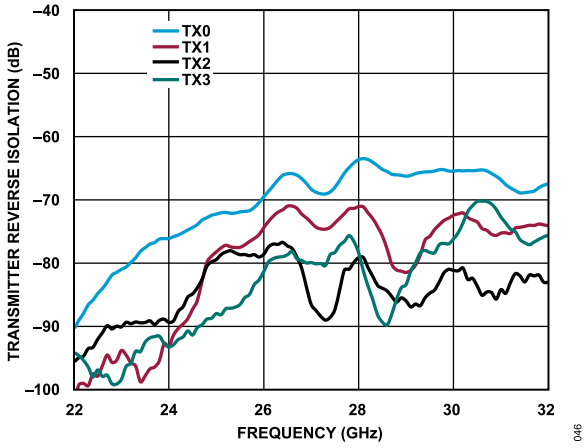

Figure 40. Transmitter Reverse Isolation vs. Frequency for TX0 to TX3

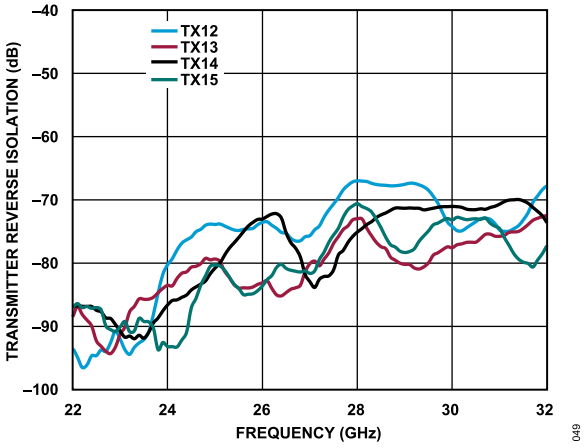

Figure 43. Transmitter Reverse Isolation vs. Frequency for TX12 to TX15

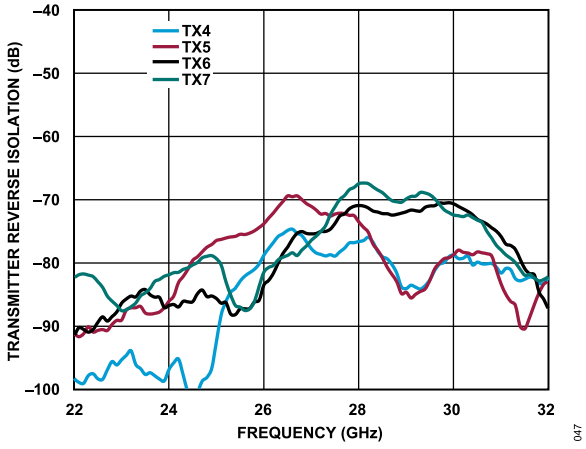

Figure 41. Transmitter Reverse Isolation vs. Frequency for TX4 to TX7

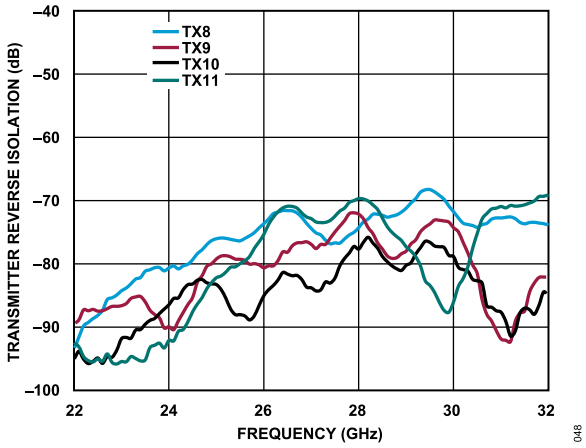

Figure 42. Transmitter Reverse Isolation vs. Frequency for TX8 to TX11

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE MODE

VDD1 to VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, T_C = 25°C, RF amplitude = −30 dBm, and set the receiver DVGA to maximum gain, unless otherwise noted.

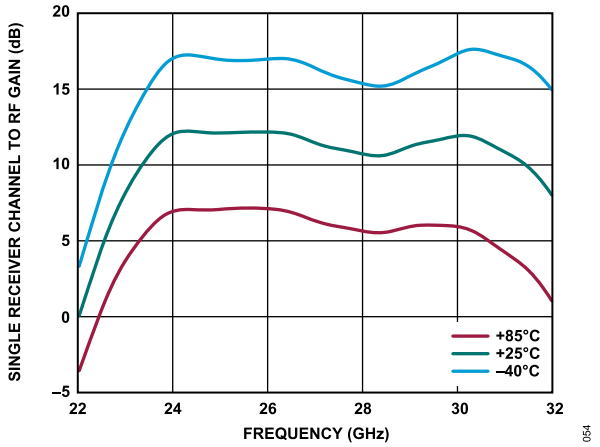

Figure 44. Single Receiver Channel to RF Gain vs. Frequency at Various Temperatures at Maximum Gain

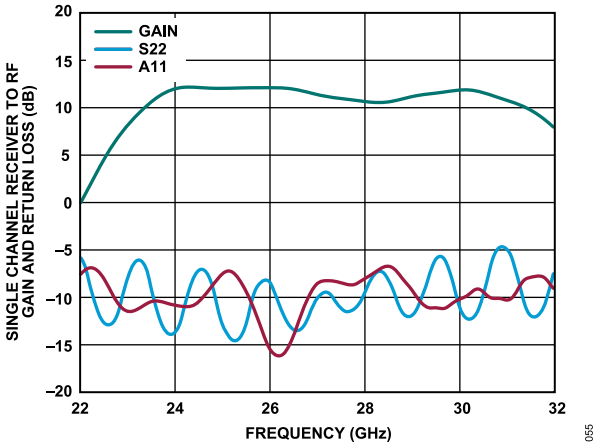

Figure 45. Single Channel Receiver to RF Gain and Return Loss vs. Frequency at Maximum Gain

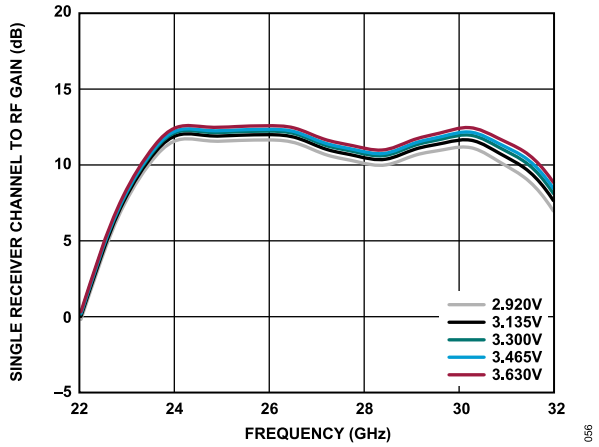

Figure 46. Single Receiver Channel to RF Gain vs. Frequency at Various Supply Voltages at Maximum Gain

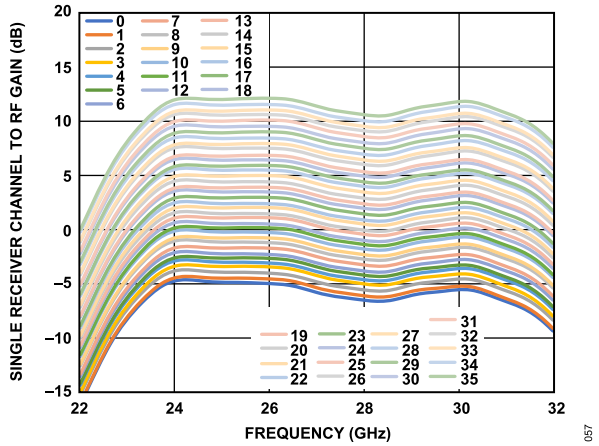

Figure 47. Single Receiver Channel to RF Gain vs. Frequency at Various Receiver DVGA Settings from 0 to 35

TYPICAL PERFORMANCE CHARACTERISTICS

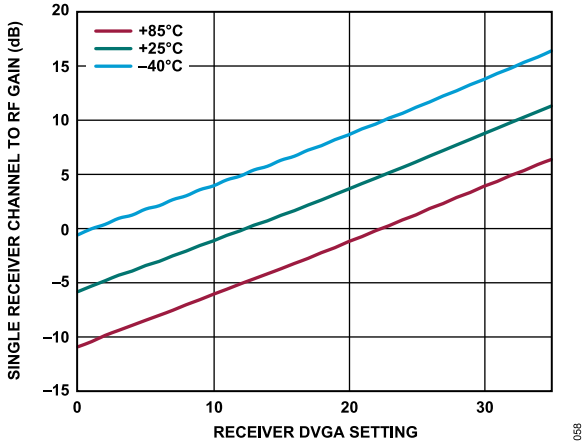

Figure 48. Single Receiver Channel to RF Gain vs. Receiver DVGA Setting from 0 to 35 over Various Temperatures at 27 GHz

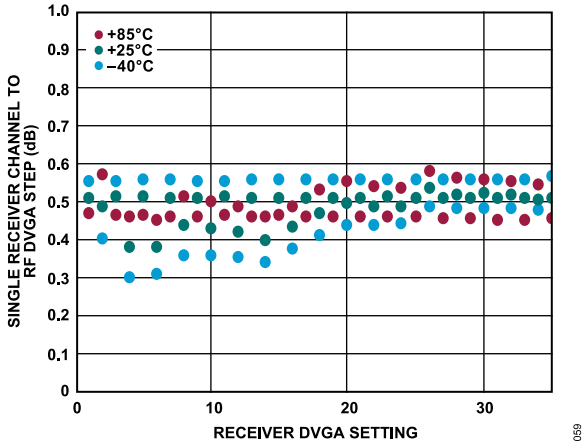

Figure 49. Single Receiver Channel to RF DVGA Step vs. Receiver DVGA Setting from 0 to 35 over Various Temperatures at 27 GHz

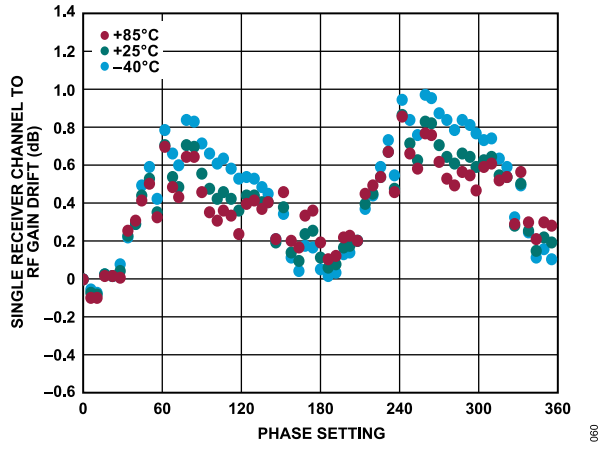

Figure 50. Single Receiver Channel to RF Gain Drift vs. Phase Setting from 0° to 360° over Temperature at 27 GHz, Set to Maximum Gain

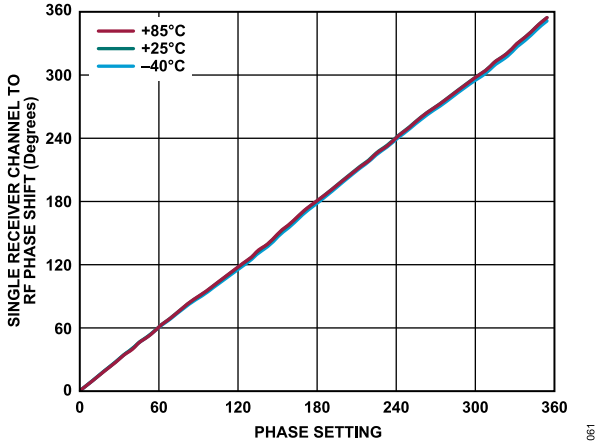

Figure 51. Single Receiver Channel to RF Phase Shift vs. Phase Setting from 0° to 360° over Various Temperatures at 27 GHz, Set to Maximum Gain

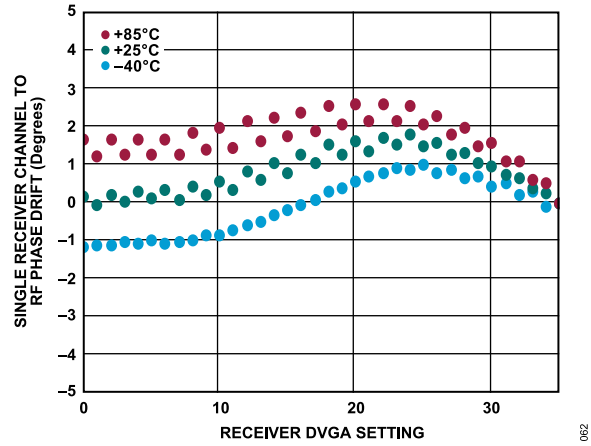

Figure 52. Single Receiver Channel to RF Phase Drift Setting from 0 to 35 over Various Temperatures at 27 GHz

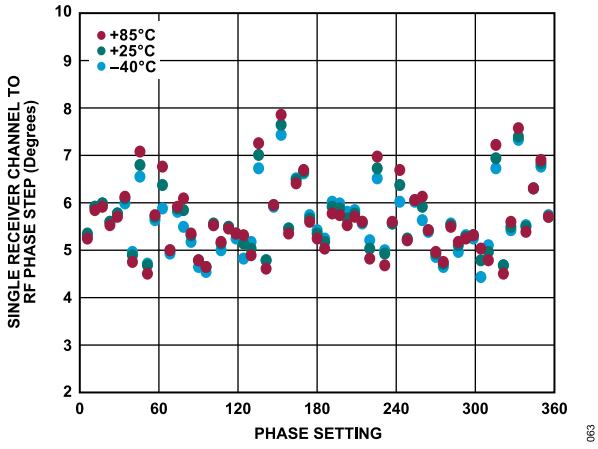

Figure 53. Single Receiver Channel to RF Phase Step vs. Phase Setting from 0° to 360° over Various Temperatures at 27 GHz, Set to Maximum Gain, Nominal Step = 5.625°

TYPICAL PERFORMANCE CHARACTERISTICS

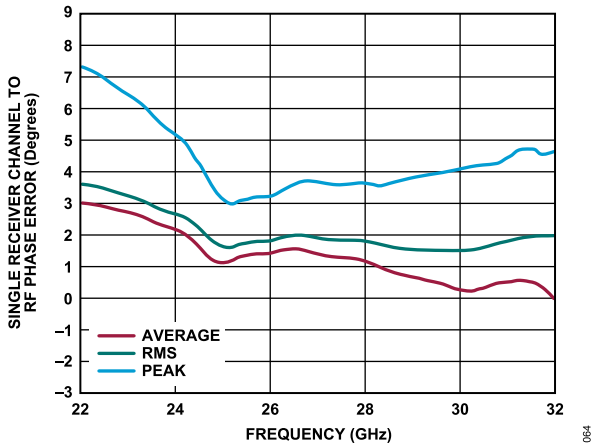

Figure 54. Single Receiver Channel to RF Phase Error vs. Frequency for Peak, Average, and RMS Error

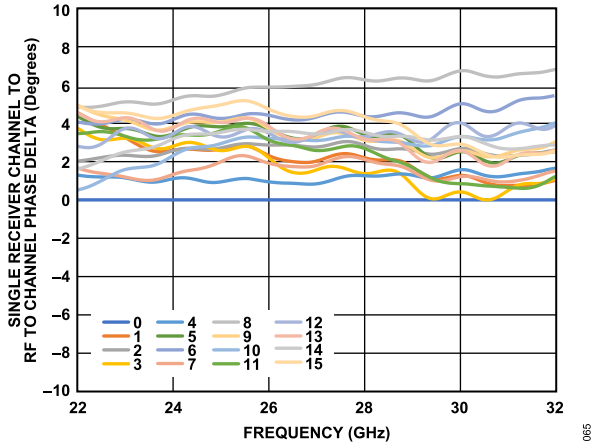

Figure 55. Single Receiver Channel to RF to Channel Phase Delta vs. Frequency at Maximum Gain, Where Numbers in Legend Are Channel Numbers

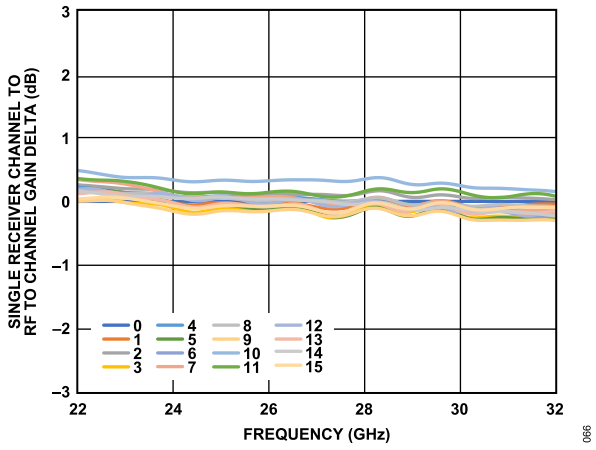

Figure 56. Single Receiver Channel to RF to Channel Gain Delta vs. Frequency at Maximum Gain, Where Numbers in Legend Are Channel Numbers

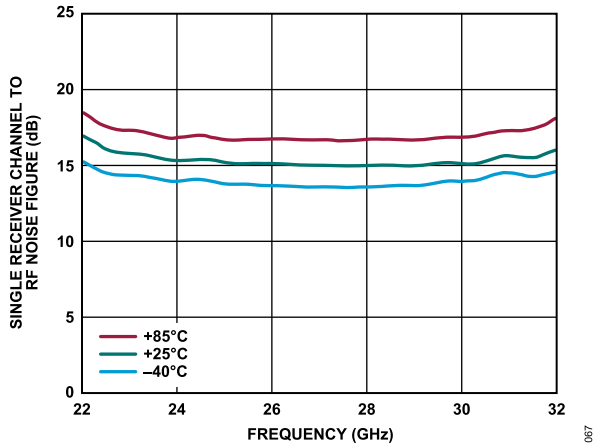

Figure 57. Single Receiver Channel to RF Noise Figure vs. Frequency at Various Temperatures at Maximum Gain

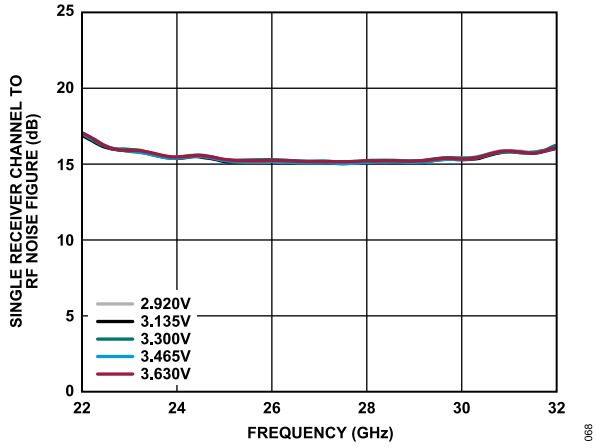

Figure 58. Single Receiver Channel to RF Noise Figure vs. Frequency at Various Supply Voltages at Maximum Gain

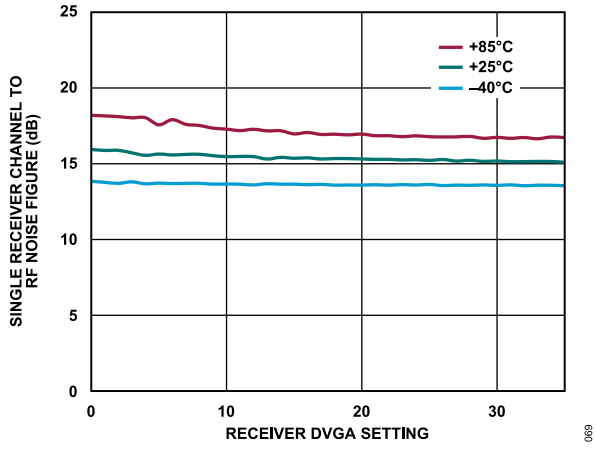

Figure 59. Single Receiver Channel to RF Noise Figure vs. Receiver DVGA Setting from 0 to 35 over Various Temperatures at 27 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

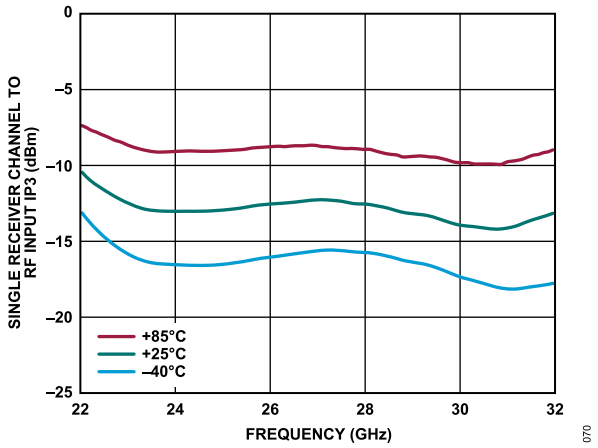

Figure 60. Single Receiver Channel to RF Input IP3 vs. Frequency at Various Temperatures at Maximum Gain

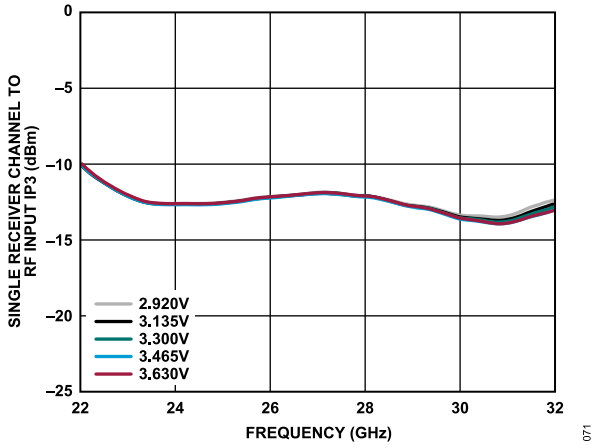

Figure 61. Single Receiver Channel to RF Input IP3 vs. Frequency at Various Supply Voltages at Maximum Gain

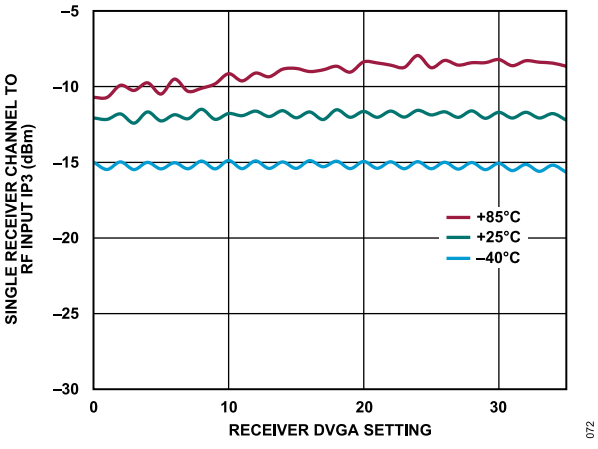

Figure 62. Single Receiver Channel to RF Input IP3 vs. Receiver DVGA Setting from 0 to 35 over Various Temperatures at 27 GHz

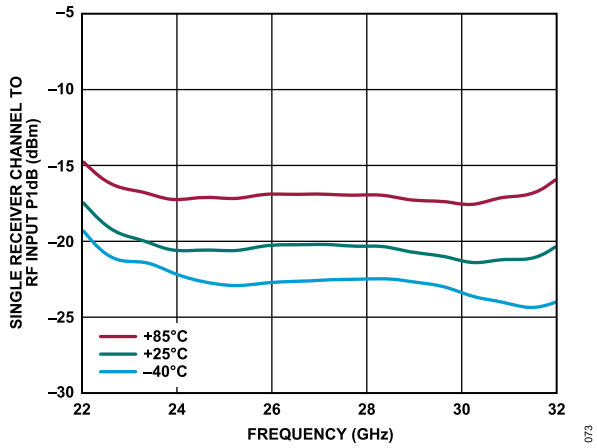

Figure 63. Single Receiver Channel to RF Input P1dB vs. Frequency at Various Temperatures at Maximum Gain

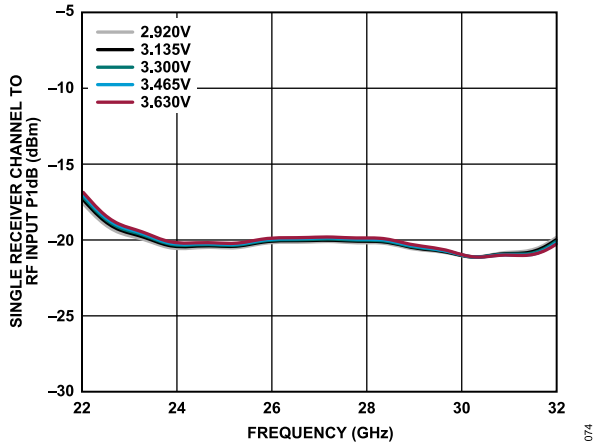

Figure 64. Single Receiver Channel to RF Input P1dB vs. Frequency at Various Supply Voltages at Maximum Gain

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSMITTER TO RECEIVER SWITCHING SPEED AND AMPLITUDE/PHASE SETTLING TIME

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6= = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on the start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, T_C = 25°C, RF amplitude = −30 dBm, and set the receiver DVGA to maximum gain, unless otherwise noted.

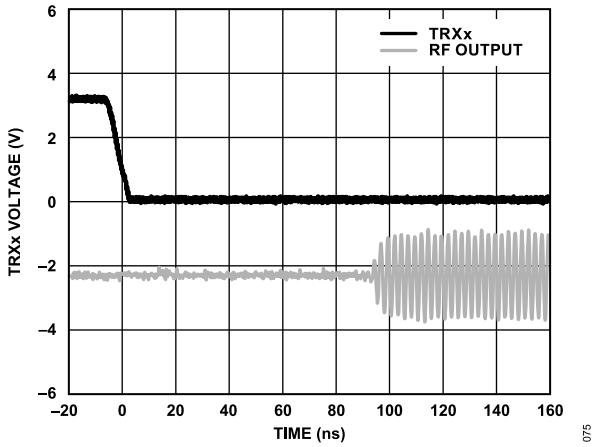

Figure 65. Transmitter to Receiver Mode Switching Time

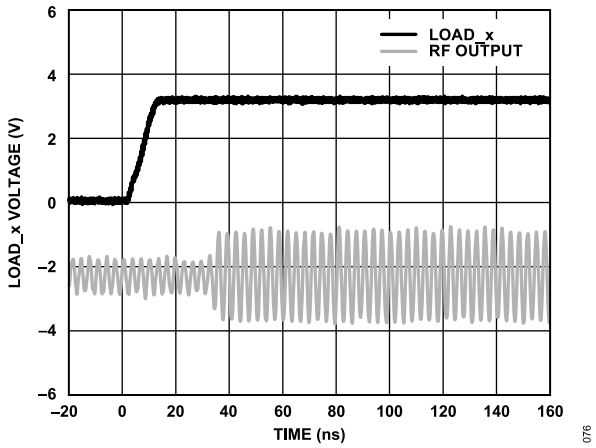

Figure 66. Gain Settling Time

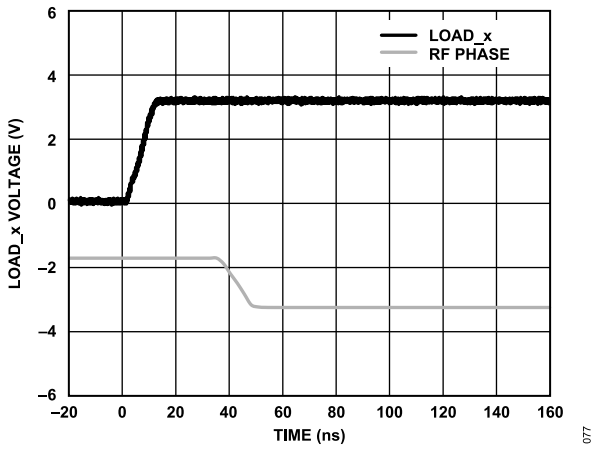

Figure 67. RF Phase Settling Time

TYPICAL PERFORMANCE CHARACTERISTICS

Receiver RFV to RFH Plane Isolation Performance

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set the SPI values based on start-up sequence described in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, and T_C = 25°C, unless otherwise noted. Measurements performed in receive mode, RF amplitude = −30 dBm, set the receiver DVGA to maximum gain, unless otherwise noted.

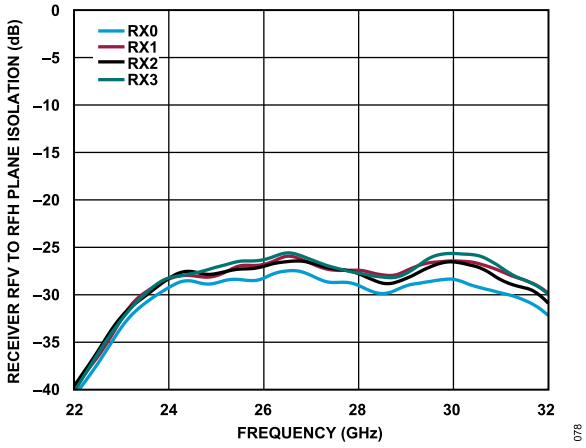

Figure 68. Receiver RFV to RFH Plane Isolation vs. Frequency for Receiver 0 (RX0), Receiver 1 (RX1), Receiver 2 (RX2), and Receiver 3 (RX3)

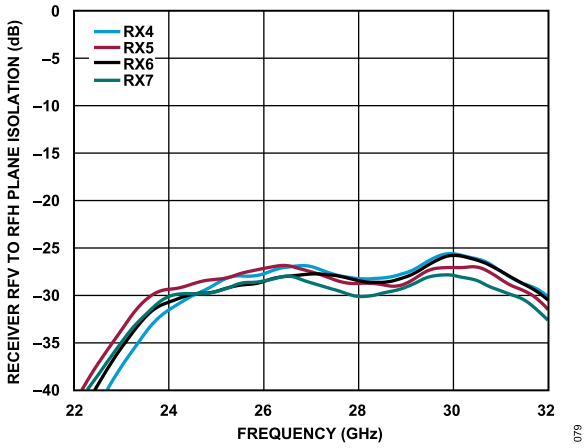

Figure 69. Receiver RFV to RFH Plane Isolation vs. Frequency for Receiver 4 (RX4), Receiver 5 (RX5), Receiver 6 (RX6), and Receiver 7 (RX7)

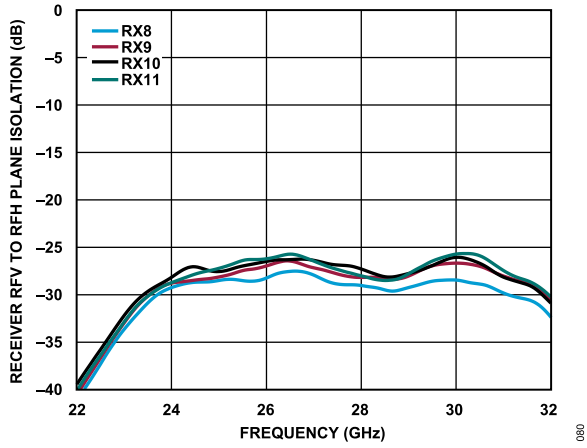

Figure 70. Receiver RFV to RFH Plane Isolation vs. Frequency for Receiver 8 (RX8), Receiver 9 (RX9), Receiver 10 (RX10), and Receiver 11 (RX11)

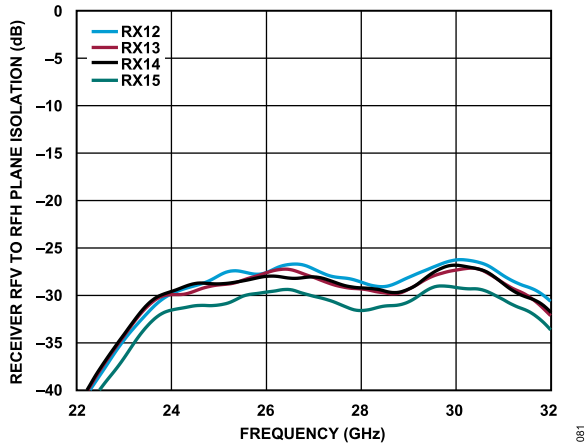

Figure 71. Receiver RFV to RFH Plane Isolation vs. Frequency for Receiver 12 (RX12), Receiver 13 (RX13), Receiver (RX14), and Receiver 15 (RX15)

TYPICAL PERFORMANCE CHARACTERISTICS

Receiver Reverse Isolation Performance

VDD1 = VDD2 = VDD3 = VDD4 = VDD5 = VDD6 = VDD7 = VDD8 = VCC_BG_3P3V = VDD_DIG_3P3V = VDD_ADC_3P3V = 3.3 V, set SPI values based on start-up sequence in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, and T_C = 25°C, unless otherwise noted. Measurements performed in receive mode, RF amplitude = −30 dBm, DVGA set to maximum gain, unless otherwise noted.

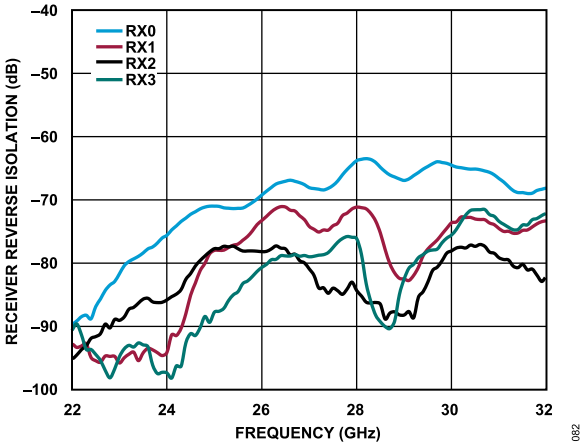

Figure 72. Receiver Reverse Isolation vs. Frequency for RX0 to RX3

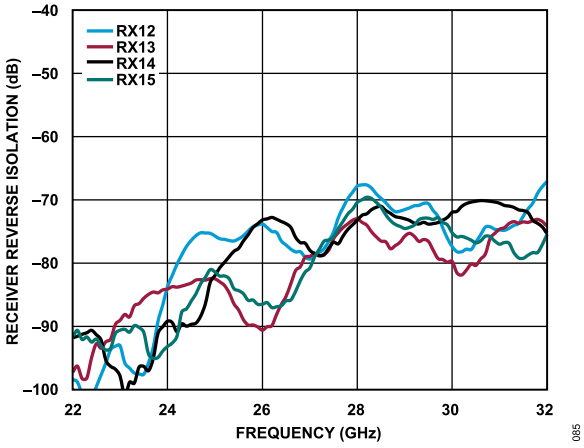

Figure 75. Receiver Reverse Isolation vs. Frequency for RX12 to RX15

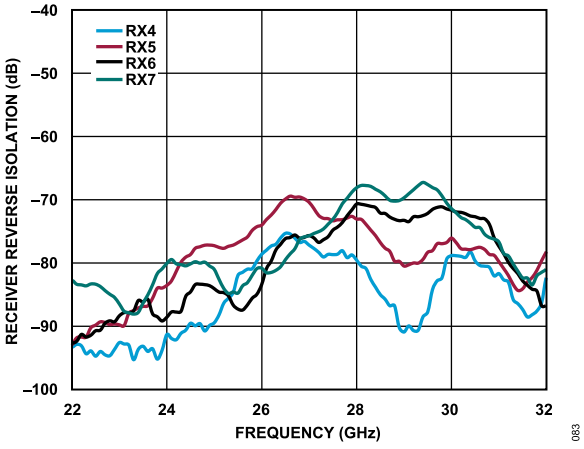

Figure 73. Receiver Reverse Isolation vs. Frequency for RX4 to RX7

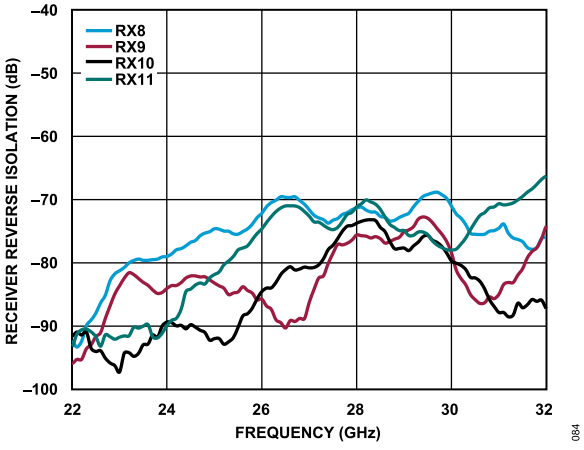

Figure 74. Receiver Reverse Isolation vs. Frequency for RX8 to RX11

THEORY OF OPERATION

The ADMV4821 is a highly integrated beamformer optimized for mmW 5G applications in the 24 GHz to 29.5 GHz frequency range. See Figure 1 for a functional block diagram of the device. The 16 independent channels of the ADMV4821 support both transmit and receive functions. The odd numbered channels are connected internally on chip to the horizontal polarization signal path of the RFH input/output pin. The even numbered channels are connected internally on chip to the vertical polarization signal path to the RFV input/output pin.

RECOMMENDED GAIN/PHASE COEFFICIENT INITIALIZATION

There are two methods for setting the gain and phase of the individual channels selected to provide efficient start-up time with minimal overhead based on the use case. One method is to use the beam pointer register, Register 0x081. This register recalls user defined beam positions from the SRAM. The beam pointer loads the beam steering values to the 16 channels. The LOAD_x pin is toggled three times to write the gain and phase setting from the memory to the selected channels. The load feature ensures that the phase and gain settings are applied to the selected channels at the same time.

Use the optional bypass mode to bypass beam pointer mode. This mode allows users to configure and debug the phase and gain settings for each channel before implementing beam pointer mode. The user can change and apply gain and phase directly to each individual channel using the channel phase and gain SRAM, common gain SRAM, and transmit and receive SRAM. The LOAD_x pin is toggled three times to write the gain and phase setting from the memory to the selected channels. The load feature ensures that the phase and gain settings are applied to selected channels at the same time. Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for detailed information.

RF SIGNAL PATH

The primary function of the chip is to accurately set the relative phase and gain of each channel so that the signals coherently add in the desired direction. The individual element gain control can compensate for many impairments presented to the chip in normal operation. Such impairments include temperature variation, chip to chip or channel to channel variation, supporting external circuitry variation for phase and gain, and the ability to enable tapering for the beam to achieve low-side lobe levels.

All 16 channel signal paths are identical to provide symmetrical performance between channels, which reduces the amount of phase and amplitude calibration to allow TDD operation. As shown in Figure 77, each transmit channel includes a DVGA 2, an in phase and quadrature (I/Q) VM, a DVGA 1, a power amplifier (PA), a power detector, and two single-pole, double throw (SPDT) switches. Each receive channel includes a low noise amplifier (LNA), an I/Q VM, a channel DVGA, and two SPDT switches. The switches select between transmit and receive paths. These paths connect the RF signal paths to the corresponding package input/output pins (RFV, RFH, and 16 channels) through a passive combining and splitting network.

PHASE AND GAIN CONTROL

Phase control is implemented using an I/Q VM architecture, as shown in Figure 76. The incoming signal is split in equal amplitude, in-phase and quadrature (I and Q) signals that are amplified independently by two identical, biphase VGAs and summed at the output to generate the required phase shift. Each VGA is controlled by 7 independent bits, 6 bits for amplitude control and 1 bit for polarity control, for a total of 14 bits per phase shifter. The vector modulator output voltage amplitude (V_{OUT}) and phase shift (Φ) are given by the following equations:

$$V_{OUT} = \sqrt{{V_Q}^2 + {V_I}^2}$$

$$\Phi = \arctan\frac{V_Q}{V_I}$$

where:
V_Q is the output voltage of the Q channel VGA.
V_I is the output voltage of the I channel VGA.

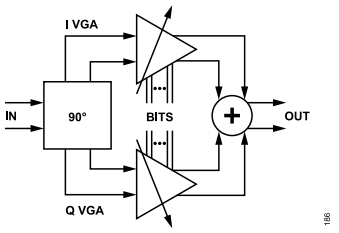

Figure 76. I/Q VM Phase Shift Block Diagram

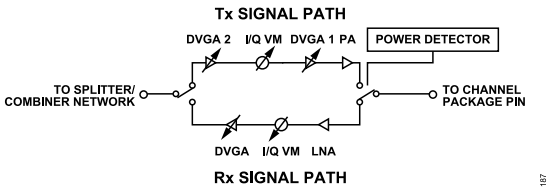

Figure 77. Transmit and Receive Channel Functional Block Diagram

THEORY OF OPERATION

When evaluating the arctangent function, the proper phase quadrant must be selected. The signs of V_I and V_Q determine the phase quadrant according to the following parameters:

- If V_I and V_Q are both negative, the phase shift is between 0° and 90°.
- If V_I is positive and V_Q is negative, the phase shift is between 90° and 180°.
- If V_I and V_Q are both positive, the phase shift is between 180° and 270°.
- If V_I is negative and V_Q is positive, the phase shift is between 270° and 360°.

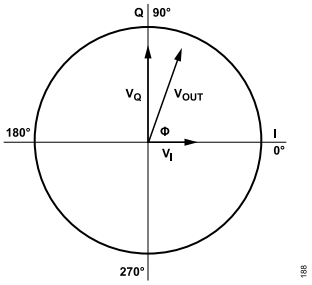

Figure 78. Vector Gain Representation

In general, select the V_I and V_Q values to generate the desired phase shift and to minimize the variation in the V_{OUT} (gain). However, allowing some amplitude variation may result in finer phase step resolution and/or lower phase errors.

Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for detailed information for phase control and features.

If the values given in the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* are used for the I and Q VGAs, the DVGAs in either the transmit or receive signal path execute gain control.

In the transmit signal path, there are two independent DVGAs to control the gain. The flexible, on-chip SPI control of each DVGA allows different options to control the dynamic range of each DVGA, based on system requirements. The DVGAs can control the channel gain for each transmit channel, and the common gain to allow all channels to be set together. The common gain is added directly to the output of the channel gain. Set a common gain offset independently for each transmit channel by using Register 0x02B, Bits[5:1]. Each DVGA allows a typical dynamic range of 16 dB, totaling 32.4 dB of total dynamic range for the transmit signal path. The common gain step resolution is 1.0 dB and the channel gain has a 0.5 dB step. By default, channel gain settings control DVGA 1 and the common gain settings control DVGA 2. This assignment of controls can be swapped by setting Register 0x02B, Bit 0 to 1. Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for detailed information.

In the receive signal path, there is a single DVGA for gain control. Program this DVGA independently to control the gain of each of the 16 receive channels. The DVGA allows a typical dynamic range of 17.1 dB for the receive signal path. The DVGA digital step resolution is 0.5 dB. The DVGA is controlled by channel gain settings and each of the 16 receive channels has independent control of the DVGA settings.

Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for detailed information about gain control and features.

TRANSMIT AND RECEIVE CONTROL

Transitioning from transmit mode to receive mode, and vice versa, is a key operating condition for a TDD phased array system. The ADMV4821 has independent transmit and receive control switches for the independent vertical and horizontal polarization signal paths. This functionality is based on the transmit and receive control signal input pins (TRXH and TRXV).

The TRXH and TRXV pins require a 1.8 V logic signal to control the switching between modes correctly. Upon turning on the ADMV4821, hold the TRXx lines at logic low to start in receiver mode. The TRXH and TRXV pins can accept a square wave up to 1.5 MHz. However, the amplitude settling time of the transmit and receive paths are in the order of 70 ns.

To transition from receive to transmit mode, the TRXH or TRXV pin must transition from logic low (0 V) to logic high (1.8 V). The rising edge of the transition from low to high logic signifies a transition to transmit mode.

To transition from transmit to receive mode, the TRXH or TRXV pin must transition from a logic high (1.8 V) to logic low (0 V). The falling edge of the transition from high to low logic signifies a transition to receive mode.

During a mode transition, all necessary settings for either mode are restored to allow fast switching for TDD applications.

Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for detailed information about transmit and receive control.

POWER DETECTORS

Sixteen power detectors (one per transmitter channel) are provided to sample the peak power coupled from the output of each power amplifier in transmit operation. These power detectors provide power monitoring and calibration for channel gain, as well as channel to channel gain mismatch. Each independent power detector circuit routes to the on-chip analog-to-digital converter (ADC) to provide SPI readback for each power detector reading with eight bits of resolution.

The input power range of the power detector is programmable and can adjust the input power sense window of 10 dBm from −12 dBm to +16 dBm in 2 dBm steps.

THEORY OF OPERATION

The 16 individual power detector values can be read back only when in transmit mode. Register 0x040 to Register 0x04F are the readback registers for the power detectors from Channel 0 to Channel 15.

The power detector readback values can be converted to dBm, as shown in Figure 30 and Figure 31.

See the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for specific SPI readback and range setting adjustment information.

TEMPERATURE SENSOR

The ADMV4821 on-chip temperature sensor can be used to sample the temperature reading on the chip in transmit operation. The temperature sensor data can be read back from the ADC and is only updated in transmit mode.

To convert the on-chip temperature sensor readback values to Celsius, use the following equation (also shown in Figure 79):

$$Temperature = 1.07 \times Temperature\ Sensor\ Value - 96$$

where the *temperature sensor value* is a decimal value.

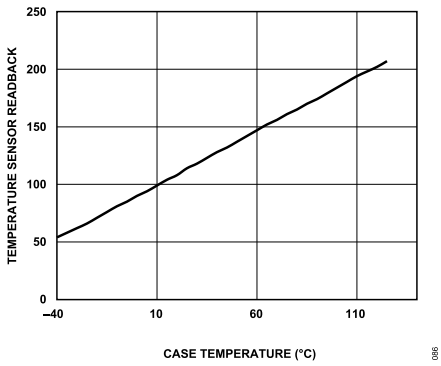

Figure 79. Temperature Sensor Readback vs. Case Temperature

Register 0x050 is used to read back the temperature sensor reading. The temperature sensor can sense from −40°C to +125°C.

Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for specific SPI readback information.

ADC OPERATION

The on-chip, 8-bit ADC is implemented to sample each of the 16 on-chip power detectors and the on-chip temperature sensor. Upon turning on the ADMV4821, set the ADC_CLK_EN bit (Register 0x030, Bit 3) to 1.

Refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for specific SPI settings and information regarding power detector and temperature sensor readback.

BIAS CONTROL FOR VARIOUS POWER MODES

Medium and low power modes are recommended to reduce dc power consumption with corresponding levels of RF performance (see the Applications Information section).

The three bias modes are nominal power, medium power, and low power mode.

In nominal power mode,

- The VDD1 to VDD8, VDD_DIG_3P3V, VDD_ADC_3P3V, and VCC_BG_3P3V pins are set to 3.3 V.
- See the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for the default preset SPI values for all registers.

In medium power mode,

- The VDD1, VDD3, VDD5, and VDD7 pins are set to 3.3 V.
- The VDD2, VDD4, VDD6, VDD8, VDD_DIG_3P3V, VDD_ADC_3P3V, and VCC_BG_3P3V pins are set to 2.5 V.
- See the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* for the default preset SPI values for all registers.

In low power mode,

- The VDD1 to VDD8, VDD_DIG_3P3V, VDD_ADC_3P3V, and VCC_BG_3P3V pins are set to 2.5 V.
- Set the Register 0x029 bit as follows: PA_BIAS_1, Bits[2:0] to 0x02 and PA_BIAS_2, Bits[5:3] to 0x00.
- Set the Register 0x2A bit as follows: PA_BIAS_3, Bits[3:0] to 0x04 and PA_VCC_SEL, Bit 4 to 0x01.

Nominal power mode provides the highest level of performance shown in the Typical Performance Characteristics section. Medium power mode and low power mode reduce the overall power consumption of the ADMV4821 for transmit mode by 20% and 40%, respectively. Note that the overall transmit gain, linearity, and output compression degrades for each lower power mode.

For receive mode, the overall power consumption reduces by 3% and 30% in medium power mode and low power mode, respectively. The receive gain also degrades in each mode. The performance characteristics vs. power mode is shown in the Performance at Various Power Modes section.

MEMORY ACCESS

On-chip SRAM is provided for storing phase and amplitude settings for up to 256 beam positions that can be located in any configuration between transmit and receive modes. The beam pointer register is used as an address reference to 256 beam positions, each with individual gain and I/Q VM settings for all 16 channels.

THEORY OF OPERATION

Upon initiating a soft reset with SPI Register 0x000, the channel and global registers restore the default values. However, the channel and global SRAM registers retain their values.

After initiating a hard reset by pulling the $\overline{RST}$ pin to a logic low, all registers, including channel, global, and global SRAM registers, are restored to the default values. However, the channel SRAM registers retain their values.

To reset all registers, including the channel SRAM registers, a power cycle is required.

Neither channel nor global SRAM registers have specific default values. These SRAM registers must be written on startup.

For more information regarding using the SRAM and other control features to achieve system level requirements, refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*.

CALIBRATION

The rms phase error resulting from using the I and Q settings is determined from the equations shown in the Phase and Gain Control section, as well as the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*. The rms phase error can be improved by running a full over the air active electronically scanned array (AESA) calibration of each channel at the desired frequency operation. Then, the proper phase adjustment for each channel can be applied to the settings of each I and Q coefficient provided to improve the rms phase error. These coefficients can then be loaded to the on-chip SRAM. The gain error can be compensated for each channel by using the individual common gain SRAM registers to improve the potential gain error for each channel.

SPI INFORMATION

The SPI of the ADMV4821 allows the user to configure the device for specific operation using one of the following two SPI configurations: a 3-wire SPI (SCLK, SDIO, and $\overline{CS}$) or a 4-wire SPI (SCLK, SDIO, SDO, and $\overline{CS}$). This interface provides users with added flexibility and customization. The SPI is compatible with 1.8 V dc logic and the on-chip LDO regulators generate the necessary 1.8 V for the global and channel digital circuitry.

The ADMV4821 protocol consists of a read and write bit followed by 15 register address bits (A14 to A0) and 8 data bits (D7 to D0). The default value for both the address and data fields are organized MSB first and end with the LSB when Register 0x000, Bit 6 is set to 0. For a write, set the first bit of each command to 0, and set the first bit of each command to 1 for a read.

The standard SPI data is set to eight bits wide. However, the ADMV4821 includes various registers that require data wider than eight bits to be able to set the register values correctly. To write to these specific registers, Register 0x008 identifies whether a command is addressing the 8 LSBs or the 8 MSBs in 16-bit registers. Writing 0x01 in Register 0x008 before writing to a 16-bit register indicates that the eight bits of data are written to the 8 LSBs. Writing 0x02 in Register 0x008 before writing to a 16-bit register indicates that the eight bits of data is written to the 8 MSBs.

Certain registers feature a LOAD_x pin that must be toggled three times to load the register values written to the device. This loading feature enables the register data to be written while remaining on standby until the LOAD_x pin is toggled.

For more information about the ADMV4821 SPI, refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*.

Standard SPI Protocol

Figure 80 shows the standard SPI protocol.

Use the $\overline{CS}$, SCLK, SDIO, and optional SDO pins to communicate with the slave device. The rising edge of the SCLK latches the data to, and from, the slave device. Table 5 shows the typical timing specifications for the SPI registers.

Note that for static random access memory (SRAM) registers, the user must send the read command twice to read back from the registers.

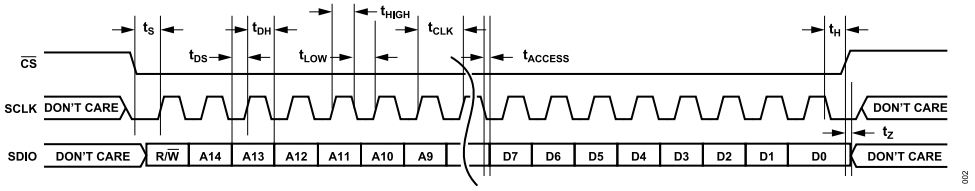

Figure 80. SPI Register Timing Diagram for Standard SPI, MSB First

THEORY OF OPERATION

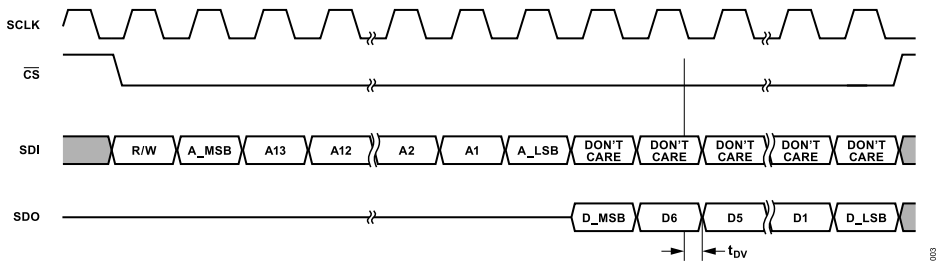

Figure 81. Timing Diagram for Standard SPI Register Read, 4-Wire Mode,

THEORY OF OPERATION

Streaming Mode

When operating in standard protocol, holding the $\overline{CS}$ pin low and shifting multiple data bytes during a single transmission reduces the amount of overhead associated with data transfer. Sequential addresses are assumed in ascending or descending order based on how the configuration registers are set. Use streaming mode to quickly load gain and phase data for the SRAM for user defined beam positions. This technique of streaming mode allows one or more bytes to be written to or read from without providing an address for each.

The timing diagram shown in Figure 82 shows a typical write to a device streaming three consecutive addresses. The first address written to is defined by the address bits, A14 to A0, and the first eight bits of data are written to this first address. The following eight bits are written to the next ascending or descending address, depending on which order is selected in Register 0x000, Bit 5. The default state for addressing sequential addresses is descending.

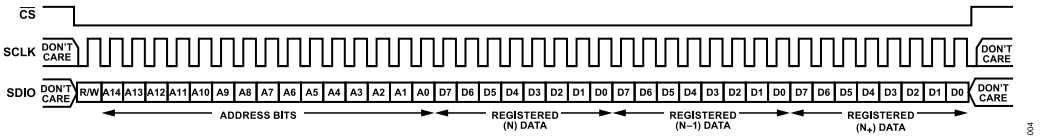

Figure 82. Streaming Mode Write Timing Diagram, MSB First, Address Descending

THEORY OF OPERATION

SPI SDO Delay During Register Reads

During a SPI read operation, data is available on the SDO pin 7 ns after the 16th falling SCLK edge arrives at the SCLK pin. This SDO delay remains constant, regardless of the SCLK speed. Refer to Figure 83 for more information.

For example, if a 10 MHz signal is applied to the SCLK pin, the SDO bit is ready to be sampled approximately 43 ns before the rising edge of the SCLK. This SCLK rate operates properly and provides margin for a reasonable amount of board propagation. At 61.44 MHz, the rising edge of SCLK is closely aligned with the falling edge of the SDO bit and the read operation may be corrupted. If operating the SCLK above 30.72 GHz, two workarounds are recommended. One workaround is to use an asymmetrical SCLK for SCLK17 to SCLK26 (longer low period). This setup keeps the rising edge of the SCLK aligned with the SDO bit. See Figure 84. The other workaround is to use a delayed SCLK at the field-programmable gate array (FPGA) to align the rising edge of SCLK with the SDO bit. See Figure 85.

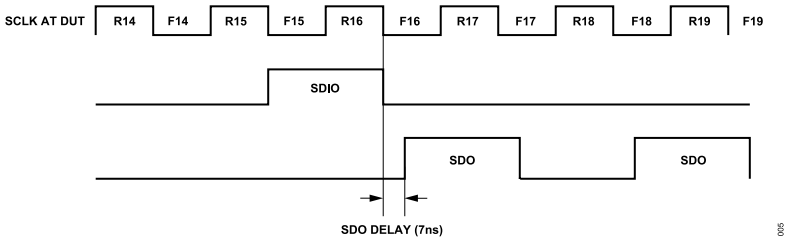

Figure 83. SDO Delay Timing Diagram

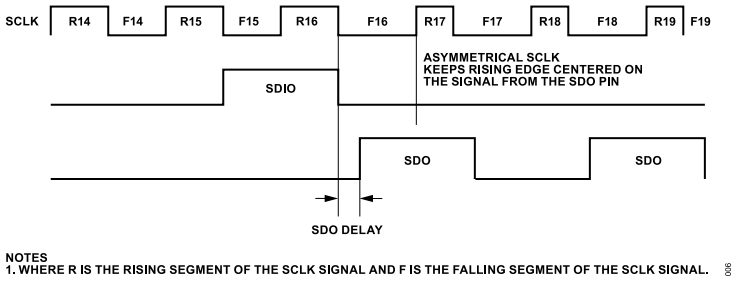

Figure 84. Using Asymmetric Clock Pulses

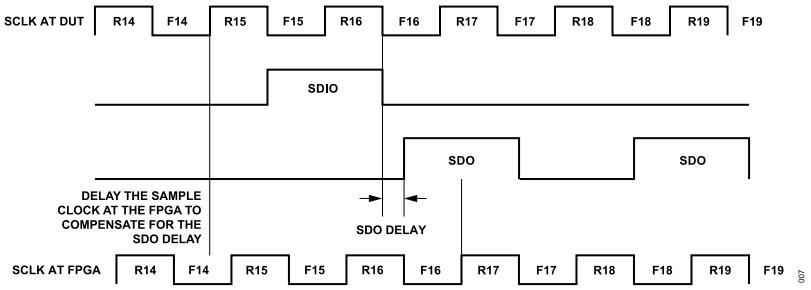

Figure 85. Using a Delayed SCLK

APPLICATIONS INFORMATION

The AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note* has detailed information regarding gain and phase control via the SPI as well as all other features described in the Theory of Operation section. Included in the application note is an example of SPI programming for the recommended method for initializing and loading all necessary registers to achieve system level performance.

POWERING THE ADMV4821

The ADMV4821 has one power supply domain, 3.3 V. An on-chip voltage regulator, internal to the ADMV4821, generates the necessary 1.8 V supply for all circuits within the chip. All supply lines that share the same supply domain can be connected to a single supply voltage to ensure that the proper decoupling capacitors are incorporated near the ADMV4821 supply pins, as shown on the ADMV4821-EVALZ user guide.

HEAT SINK SELECTION

Both the top side and bottom side heat sinks can be attached to the device for efficient heat transfer.

The bottom side heat sinks require a large exposed copper area on the board bottom layer under the device.

For the top side heat sink, the size of the heat sink must be the same as the device. A smaller heat sink can cause inefficient heat transfer. Thermal interface material (TIM) is required to attach the top side heat sink to the device. The TIM fills the gap between the device and heat sink, improving the thermal contact of the device and heat sink. Typically, 0.5 mm thick TIM is recommended for optimum heat transfer and device performance.

The maximum force to apply the heat sink to the device is specified in Table 6. The board under the component must be fully supported to prevent the board from flexing. Apply the force perpendicular to the component to evenly distribute the pressure on the topside of the component.

PERFORMANCE AT VARIOUS POWER MODES

Nominal, Medium, and Low Power Mode Data for Transmit Mode

Figure 86 through Figure 90 show the performance of each parameter using the bias conditions described in the Bias Control for Various Power Modes section.

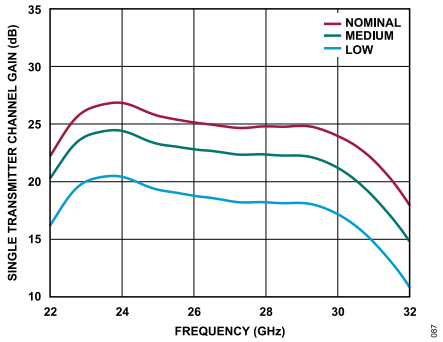

Figure 86. Single Transmitter Channel Gain vs. Frequency at Various Power Modes, Maximum Gain

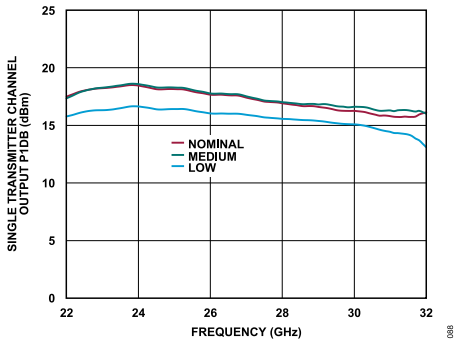

Figure 87. Single Transmitter Channel Output P1dB vs. Frequency at Various Power Modes, Maximum Gain

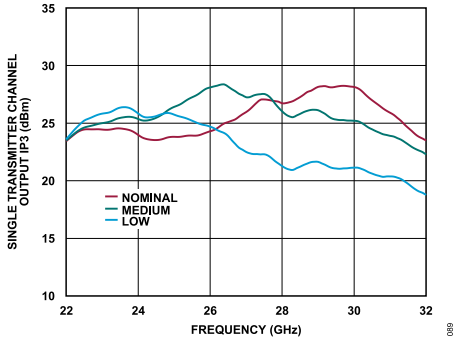

Figure 88. Single Transmitter Channel Output IP3 vs. Frequency at Various Power Modes, Maximum Gain

APPLICATIONS INFORMATION

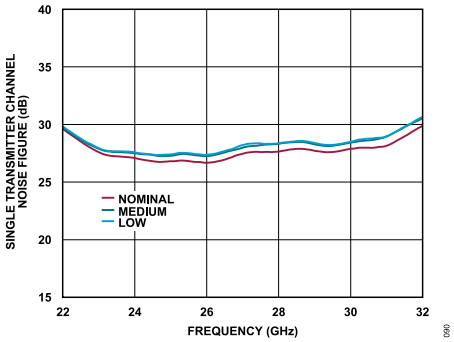

Figure 89. Single Transmitter Channel Noise Figure vs. Frequency at Various Power Modes, Maximum Gain

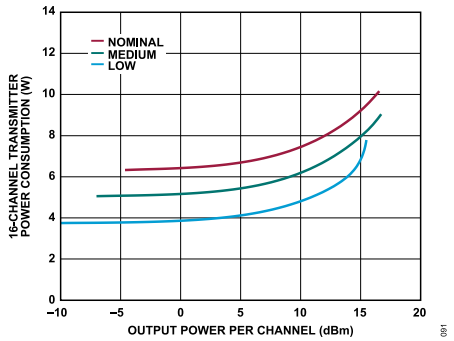

Figure 90. 16-Channel Transmitter Power Consumption vs. Output Power per Channel, Maximum Gain

Nominal, Medium, and Low Power Mode Data for Receive Mode

Figure 91 through Figure 94 show the performance of each parameter using the bias conditions discussed in the Bias Control for Various Power Modes section.

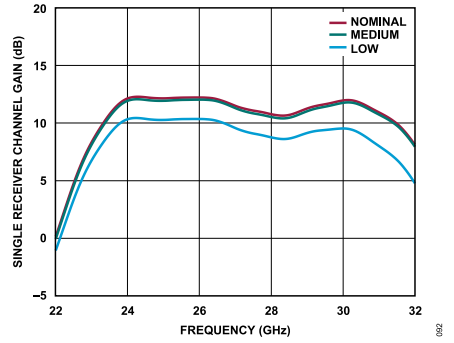

Figure 91. Single Receiver Channel Gain vs. Frequency at Various Temperatures, Maximum Gain

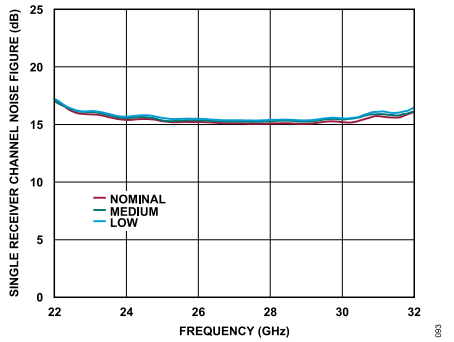

Figure 92. Single Receiver Channel Noise Figure vs. Frequency at Various Temperatures, Maximum Gain

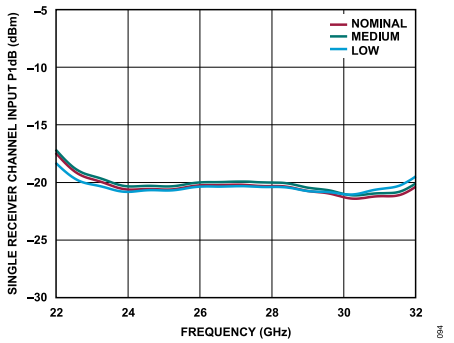

Figure 93. Single Receiver Channel Input P1dB vs. Frequency at Various Temperatures, Maximum Gain

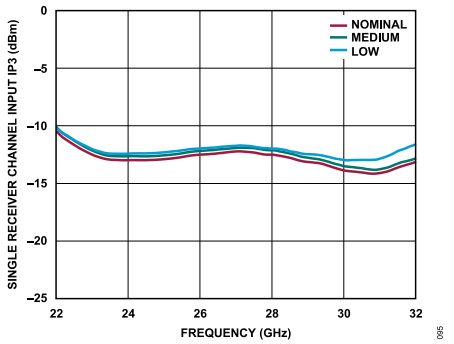

Figure 94. Single Receiver Channel Input IP3 vs. Frequency at Various Temperatures, Maximum Gain

TRANSMIT MODE ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

Figure 95 shows the single transmitter channel EVM vs. output power per channel of the ADMV4821 at maximum gain. The EVM measurement is performed using four 100 MHz, 5G new radio (NR), 256 quadrature amplitude modulation (QAM).

APPLICATIONS INFORMATION

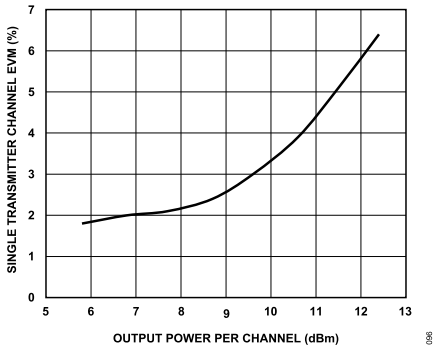

Figure 95. Single Transmitter Channel EVM vs. Output Power Per Channel at Maximum Gain

OUTLINE DIMENSIONS

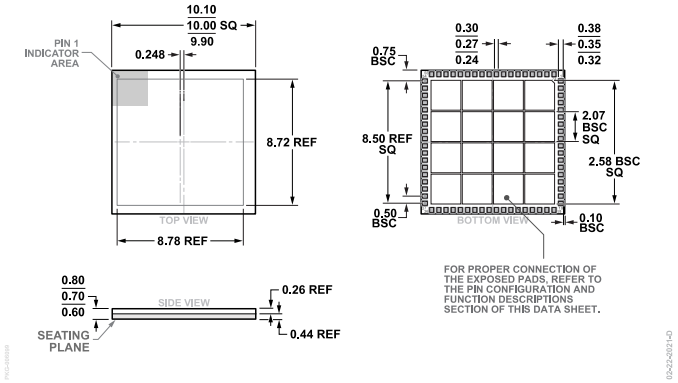

Figure 96. 72-Terminal Land Grid Array [LGA]
(CC-72-3)
Dimensions shown in millimeters

Updated: February 13, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADMV4821BCCZ	-40°C to +95°C	72-Terminal LGA (10mm x 10mm x 0.7mm)	Tray, 31	CC-72-3

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADMV4821-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.