

Evaluating the ADMV4821 24 GHz to 29.5 GHz Transmitter/Receiver, Dual Polarization Beamformer

FEATURES

- Fully featured evaluation board for the ADMV4821
- On-board SDP-S connector for SPI control
- ▶ 5 V operation through LDO regulators
- ACE software interface for SPI control

EVALUATION KIT CONTENTS

► ADMV4821-EVALZ

EQUIPMENT NEEDED

- ▶ 5 V dc power supply
- ▶ RF signal generator
- Spectrum analyzer or network analyzer
- ▶ USB to mini USB cable
- ▶ SDP-S controller board

DOCUMENTS NEEDED

- ADMV4821 data sheet
- AN-2021 Application Note, ADMV4801/ADMV4821 SPI Application Note (contact Analog Devices at mmwave5G@analog.com)

EVALUATION BOARD PHOTOGRAPH

SOFTWARE NEEDED

► ACE software

GENERAL DESCRIPTION

The ADMV4821-EVALZ evaluation board incorporates the ADMV4821 silicon germanium (SiGe), 24 GHz to 29.5 GHz, 5G beamformer with low dropout (LDO) regulators, level shifters, and an EVAL-SDP-CS1Z (SDP-S) controller board to allow the simplified and efficient evaluation of the ADMV4821. The RF IC is highly integrated and contains 16 independent transmitter and receiver channels. The device supports eight horizontal and eight vertical polarized antennas via independent RFV and RFH input/outputs (I/Os). The chip can be programmed using a 3-wire or 4-wire serial port interface (SPI). The SDP-S controller allows the user to interface with the ADMV4821 SPI through the Analog Devices, Inc., Analysis, Control, Evaluation (ACE) software. The level shifters translate the 1.8 V chip logic level to the 3.3 V SDP-S logic level. The LDO regulators allow the ADMV4821 to be powered on by a single supply.

For full details on the ADMV4821, see the ADMV4821 data sheet, which must be consulted in conjunction with this user guide when using the ADMV4821-EVALZ.

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Figure 1.

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REVISION HISTORY

3/2022—Revision	A: Initial Version
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EVALUATION BOARD HARDWARE

The ADMV4821-EVALZ has an on-board ADMV4821 chip. Figure 2 shows the block diagram of the ADMV4821-EVALZ.

Figure 3 shows the ADMV4821 lab bench setup for transmitter mode. Connect the 5 V dc power supply to the ADMV4821-EVALZ 5V test point and ground the power supply to the GND1 test point. Set the power supply current compliance to 3 A. Use the mini USB connector to connect the PC to the ADMV4821-EVALZ. For transmitter mode, connect the RFV or RFH port to an RF signal generator. Connect the spectrum analyzer to the channel being evaluated. All unused channels must be 50 Ω terminated.

For receiver mode, connect the RFV or RFH port to the spectrum analyzer (see Figure 4). Connect an RF signal generator to the channel being evaluated. All unused channels must be 50 Ω terminated.

Note that the ADMV4821-EVALZ comes with a bottom side heat sink that provides improved visually for the single device on board. For final application, a top side heat sink is recommended.



Figure 2. ADMV4821-EVALZ Block Diagram



Figure 3. ADMV4821-EVALZ Lab Bench Setup for Transmitter Mode (Example for Evaluating Channel 2 and RFV Port)

EVALUATION BOARD HARDWARE



Figure 4. ADMV4821-EVALZ Lab Bench Setup for Receiver Mode (Example for Evaluating Channel 2 and RFV Port)

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND THE ADMV4821 PLUGINS AND DRIVERS

The ADMV4821-EVALZ uses the ACE software for testing. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

If the ACE software is already installed on the PC, ensure that the installed software is the latest version, as shown on the www.ana-log.com/ACE page. If the previously installed software is not the latest version, take the following steps to install the updated ACE software:

- 1. Uninstall the current version of the ACE software.
- 2. Delete the ACE folder in C:\ProgramData\Analog Devices.
- Install the latest version of the ACE software. During the installation, ensure that the PreRequisites boxes are selected for installation as well (see Figure 5).

ACE Setup	– 🗆 X
Choose Components	
Choose which features of ACE	you want to install.
Check the components you war install. Click Install to start the	nt to install and uncheck the components you don't want to installation.
Select components to install:	
	< >
	Description
Space required: 4.7 GB	Position your mouse over a component to see its description.
Nullsoft Install System v3.05	
	< Back Install Cancel

Figure 5. Drivers to Install with ACE Software

- When the ACE software installs, download the ADMV4821.acezip file provided by Analog Devices.
- When the download completes, double click the ADMV4821.acezip file to install the ADMV4821 plugin on the ACE software.

When the plugin installations complete, the ADMV4821-EVALZ plugin (**ADMV4821 Board**) appears when the ACE software opens (see Figure 6).



Figure 6. ADMV4821-EVALZ Plugin Window After Opening ACE Software

HARDWARE SETUP

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To set up the ADMV4821-EVALZ for testing, take the following steps:

- 1. Connect a USB cable to the PC and then to the ADMV4821-EVALZ.
- Power up the ADMV4821-EVALZ with a 5 V dc supply. When the USB cable is connected to the PC, the PC recognizes the ADMV4821-EVALZ.
- 3. Open the ACE software. The ADMV4821 Board plugin appears in the Attached Hardware section. Double click the plugin.

If the device is turned off and then on, or if the USB cable is unplugged and plugged back in while the ACE software is open, contact with the ADMV4821-EVALZ is lost. To regain contact, click the **System** tab, click the **USB** symbol on the **ADMV4821** subsystem, and then click **Acquire**. This command allows the user to reconnect to the ADMV4821-EVALZ. If this command does not work, the user must restart ACE.

 The ADMV4821 Board tab opens. Double click the ADMV4821 icon in the middle of the window (see Figure 7).

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

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Figure 7. ADMV4821-EVALZ Plugin View

5. The ADMV4821 plugin appears (see Figure 8).



Figure 8. ADMV4821 Plugin Home Page in ACE Software

The ADMV4821 plugin has the following functions and features:

- Device initialization.
- Switching between transmitter mode and receiver mode.
- ▶ Dual polarization evaluation.
- Changing gain and phase settings for all channels or an individual channel.
- ▶ On-chip static random access memory (SRAM) read and write.
- ▶ Beam pointer mode and bypass mode.
- Readback from on-chip temperature sensor and power detectors.

See the ADMV4821 data sheet for a full description of each block and register, as well as the corresponding settings.

Note that the ACE software provides a simplified tutorial for testing the ADMV4821. For more customized and detailed implementation, refer to the AN-2021 Application Note, ADMV4801/ADMV4821 SPI Application Note.

INITIALIZATION AND QUICK START

Figure 9 shows the ADMV4821-EVALZ home page in the ACE software. The device is reset automatically after opening the home page.

For first time device evaluation, take the following steps:

- 1. Turn on the 5 V power supply. Set the current compliance to 3 A.
- 2. Open the ACE software and the ADMV4821 Board plugin.
- Choose TX from the Choose Mode dropdown list (Label F) and 17 dB from the Tx Common Gain dropdown list (Label B) in both the Vertical (Even) Channels section and the Horizontal (Odd) Channels section.
- 4. Choose Bypass Beam Pointer SRAM in the BeamPointer SRAM dropdown list (Label G).
- 5. Select the Same Values for all channels checkbox (Label C).
- 6. Click Write Tx Channel and Common Gain and Phase (Label H1) and click Write PA Power (Label H5) to load the gain and phase settings. All transmitter channels turn on. The current consumption is about 2.2 A.

Table 1 describes the functions of each block in the ADMV4821home page shown in Figure 9.

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		Cannel 6	
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		Channel 9 Convertencements Support V MON V 0 (1962 V 0 (10 (1979 0 (1)))	
		Channel 10 Dever Security Proper V RON V S (1922 V S (1) 192 V S (
		Channel 11 Dever Selection Pager 4 10.01 4 5 (10.2 4 5 (
		Channel 12 Obave Selectific Progen V Roth V 0 1 VR2 V 0 1 0 1 P10 V 0 1 0 1 P10 V 0 1 Obave V 0 1 Obav	
		Oannel 13 Diamel Statestic Angent v 840 v 0 0 1062 v 0 0 0 1055 v 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
		Channel 14 Dearent Selected Selected Transport V RACK V 0 1 VR2 V 0 1 0 1 115 V 0 1 0 1 0 1 0 0 0 1 115 V 0 1 Attenuator V 1 1 Channel 14	
		Channel 13 Deave Sector's Progent V RACK V 0 0 VKR2 V 0 0 0 0 112 VKR2 V 0 0 0 0 112 VKR2 V 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Report Issue			Proceed to Memory N

Figure 9. ACE Software Home Page ADMV4821-EVALZ

Label	Function	
A	Click Reset Chip to reset the device (same function as Reset Chip in Label M3).	
В	Use the Tx Common Gain dropdown list to select the transmitter common gain level to write to Register 0x08E for vertical polarization and Register 0x08F for horizontal polarization (see the AN-2021 Application Note, <i>ADMV4801/ADMV4821 SPI Application Note</i>). The common gain selected is applied to the DVGA 2 block in the transmit path by default. Refer to the ADMV4821 data sheet for more details on the digital variable gain amplifiers (DVGAs) in the RF signal path.	

Table 1. ACE Plugin Home Page Labels and Functions Label Function

Labei	Function	
С	Select the Same Values for all channels checkbox to bring up the settings section for all channels (Label I). Changes made in this section are applied to all channels in the Label J, Label K, and Label L sections but are not loaded until Label H1 to Label H6 are clicked. Note that the changes are not loaded to channels that are not selected to program in the Select Channel section (Label J).	
D	Click Navigate to SRAM Tables to access the gain and phase SRAM and the beam position SRAM.	
E	Click TempSensor and Tx Detectors to open the readback page. See the Temperature Sensor and Power Detector section for details.	
F	Use the Choose Mode dropdown list to choose transmitter mode or receiver mode for each polarization.	
G	Use the BeamPointer SRAM dropdown list to choose bypass mode or beam pointer mode	
H1	Click Write Tx Channel and Common Gain and Phase to load the gain and phase changes to the device. It is not recommended to click Apply Changes (La	
H2	Click Write Rx Channel Gain and Phase to load the gain and phase changes to the device. It is not recommended to click Apply Changes (Label M1) when writing to channels.	
H3	Click Read Last Programmed Values to read the channel settings from the last programmed channels.	
H4	Click Write LNA Attn Values to load the LNA attenuation values to the device. Clicking Apply Changes (Label M1) is not recommended.	
H5	Click Write PA Power to load the power amplifier power setting to the device. Clicking Apply Changes (Label M1) is not recommended.	
H6	Click Write Common Gain Offset and VGA Type to load the common gain offset and VGA type to the device. Clicking Apply Changes (Label M1) is not recommended.	
I	This section is visually enabled when the Same Values for all channels checkbox is selected. All 16 channels can be changed simultaneously in this section.	
J	Label J is the Select Channel section. When Channel Selected to Program is chosen for a channel, any changes occurring in the TX and RX sections (Label K and Label L) are loaded when the Write Tx Channel and Common Gain and Phase (Label H1) or Write Rx Channel Gain and Phase (Label H2) buttons are clicked. When Channel NOT Selected to Program is chosen for a channel, changes to the channel are not loaded to the device.	
K	The TX section includes the following transmitter gain and phase functions:	
	PA Power: turns the power amplifier on or off for each channel.	
	Common Gain Offset : scroll up or down to change the common gain offset, Register 0x02B, Bits[5:1], of each transmit channel. The offset is added to the common gain in dB. For example, choose a value of 1 to add 1 dB to the common gain.	
	Common Gain DVGA Select : use the individual dropdown lists to choose which DVGA to assign to the common gain. The unassigned DVGA is assigned to the channel gain. It is recommended to use the default setting, where DVGA 1 is chosen for the channel gain and DVGA 2 is chosen for the common gain.	
	Channel Gain SRAM Index : scroll up or down to choose the preset gain states stored in the transmitter gain SRAM for each channel gain. Offset 0 to Offset 31 correspond to the transmitter gain SRAM, Register 0x1C0 to Register 0x1DF. The transmitter gain SRAM table can be changed in the Navigate to SRAM Tables page (Label D) (see the AN-2021 Application Note, <i>ADMV4801/ADMV4821 SPI Application Note</i>).	
	Channel Phase SRAM Index: scroll up or down to choose the preset phase states stored in the transmitter phase SRAM of each transmit channel. Offset 0 to Offset 63 correspond to the transmitter phase SRAM, Register 0x180 to Register 0x1BF. The transmitter phase SRAM table can be changed in the Navigate to SRAM Tables page (Label D) (see the AN-2021 Application Note, ADMV4801/ADMV4821 SPI Application Note).	
	Channel Gain Level: displays the real gain levels.	
	Phase: displays the real phase values.	
L	The RX section includes the following receiver gain and phase functions:	
	Channel Gain SRAM Index: scroll up or down to choose the preset gain states stored in the receiver gain SRAM for the receiver gain of each receive channel. Offset 0 to Offset 31 correspond to the receiver gain SRAM, Register 0x140 to Register 0x15F. The receiver gain SRAM table can be changed in the Navigate to SRAM Tables page (Label D) (see the AN-2021 Application Note, <i>ADMV4801/ADMV4821 SPI Application Note</i>).	
	Channel Phase SRAM Index : scroll up or down to choose the preset phase states stored in the receiver phase SRAM of each receive channel. Offset 0 to Offset 63 correspond to the receiver phase SRAM, Register 0x100 to Register 0x13F. The receiver phase SRAM table can be changed in the Navigate to SRAM Tables page (Label D) (see the AN-2021 Application Note, <i>ADMV4801/ADMV4821 SPI Application Note</i>).	
	Channel Gain Setting: displays the real gain levels.	
	LNA Attenuation: scroll up or down to choose the LNA attenuation of each receive channel.	
	Phase: displays the real phase values.	
M1	It is not recommended to click Apply Changes in normal operation. Use Label H1 to Label H6 to read and write to the channels.	
M2	It is not recommended to click Read All in normal operation. Use Label H1 to Label H6 to read and write to the channels.	

Label	Function
M3	Reset Chip has the same functionality as Label A.
M4	It is not recommended to click Diff in normal operation. Use Label H1 to Label H6 to read and write to the channels.
M5	Click Software Defaults to restore the software default register values.
M6	Click Memory Map Side-By-Side to enable the side by side memory map view.
N	Click Proceed to Memory Map to open the ADMV4821 memory map.

TRANSMITTER AND RECEIVER GAIN AND PHASE STATES SRAM

Bypass mode and beam pointer mode use the gain and phase states SRAM. For simplified evaluation, the graphical user interface (GUI) presets and loads the SRAM at initialization. The SRAM can be changed and customized based on the user application.

The transmitter and receiver gain states SRAM stores up to 32 channel gain states for the transmitter states settings that can be applied to an individual transmitter or receiver channel by specifying the gain states index, as shown in Table 2 and Table 3. Click **Navigate to SRAM Tables** in the ACE home page to access the tables shown in Figure 10.

The ACE software predefines the gain SRAM. To change the gain SRAM, use the export or import .CSV file function instead of modifying the gain SRAM directly in the GUI.

Click the appropriate export icon in Figure 10 and then save the .CSV file to any local directory. The .CSV file looks like the example shown in Figure 11. Row 2 to Row 33 correspond to Gain States Index 0 through Gain States Index 31 in Table 2 and Table 3. Each cell in the .CSV file stores the decimal representation of the gain shown in Table 4. There are 36 available gain levels to choose from, from 0 dB to 17.5 dB in 0.5 dB steps. Table 4 shows the hexadecimal and decimal representations for the 36 gain values.

When the updated gain states SRAM file imports, click the **Write to SRAM** button shown in Figure 10 to load the values to the device.

Click the **Fill SRAM Tables** button shown in Figure 10 to reset the gain and phase to default values (see the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*).

Table 2. Receiver Gain States SRAM

Address	Index	Channel Gain
Register 0x140	0	User defined
Register 0x141	1	User defined
Register 0x142	2	User defined
Register 0x15F	31	User defined
Table 3. Transmitter Gain States SRAM		

Address	Index	Channel Gain
Register 0x1C0	0	User defined
Register 0x1C1	1	User defined

Table 3. Transmitter Gain States SRAM			
Address	Index	Channel Gain	
Register 0x1C2	2	User defined	
Register 0x1DF	31	User defined	

Table 4. Gain Level Truth Table

Gain (dB)	Data (Hexadecimal)	Data (Decimal)
0	00	0
0.5	01	1
1	02	2
1.5	03	3
2	04	4
2.5	05	5
3	06	6
3.5	07	7
4	08	8
4.5	09	9
5	OA	10
5.5	OB	11
6	OC	12
6.5	0D	13
7	0E	14
7.5	OF	15
8	10	16
8.5	11	17
9	12	18
9.5	13	19
10	14	20
10.5	15	21
11	16	22
11.5	17	23
12	18	24
12.5	19	25
13	1A	26
13.5	1B	27
14	1C	28
14.5	1D	29
15	1E	30

Table 4. Gain Level Truth Table			Level Truth Table	
Data (Hexadecimal)	Data (Decimal)	Gain (dB)	Data (Hexadecimal)	Data (Decimal)
1F	31	17	22	34
20	32	17.5	23	35
21	33			
	S2011/254 Samples ADMANDES ADMANDES			-
	BEAM SETTINGS SRAM	BEAM SETTINGS I <		PHASE STATES SRAM



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	٨	P	C	D	E	E	C
1	A	D RyChannel	Gain thi	U	E	r	G
2	35	35					
3	34	34					
4	33	33					
5	32	32					
6	31	31					
7	30	30					
8	29	29					
9	28	28					
10	27	27					
11	26	26					
12	25	25					
13	24	24					
14	23	23					
15	22	22					
16	21	21					
17	20	20					
18	19	19					
19	18	18					
20	17	17					
21	16	16					
22	15	15					
23	14	14					
24	13	13					
25	12	12					
26	11	11					
27	10	10					
28	9	9					
29	8	8					
30	7	7					
31	6	6					
32	5	5					
33	4	4					
34							

Figure 11. Transmitter and Receiver Gain SRAM .CSV File

The transmitter and receiver phase SRAM stores up to 64 phase states for the transmitter and receiver, respectively. The phase

states can be applied to individual transmitter or receiver channels by specifying the index, as shown in Table 5 and Table 6.

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To change the phase SRAM, use the export or import .CSV file function instead of modifying the phase SRAM directly in the GUI. See Figure 12 for the correct .CSV file. Row 2 to Row 65 correspond to the Phase States Index 0 through Phase States Index 63 in Table 5 and Table 6. Note that each cell in the .CSV file stores the real phase value in a 5.625° step size instead of the hexadecimal or decimal representation. Real phase values are only used in the ACE software. For final applications, refer to the AN-2021 Application Note, *ADMV4801/ADMV4821 SPI Application Note*, for further details on the phase state SRAM.

When the updated phase states SRAM file imports, click the **Write to SRAM** button shown in Figure 10 to load to the device.

Click the **Fill SRAM Tables** button shown in Figure 10 to reset the gain and phase to default values.

Table 5. Receiver Phase States SRAM

Address	Index	In Phase	Quadrature Phase
Register 0x100	0	User defined	User defined
Register 0x101	1	User defined	User defined
Register 0x102	2	User defined	User defined
Register 0x13F	63	User defined	User defined

Table 6. Transmitter Phase States SRAM

Address	Index	In Phase	Quadrature Phase
Register 0x180	0	User defined	User defined
Register 0x181	1	User defined	User defined
Register 0x182	2	User defined	User defined
Register 0x1BF	63	User defined	User defined

A	1	•	\times	\checkmark	f _x	Phase
	۵				в	
1	PhaseTX tbl		Pha	seRX tbl	0	
2			0			0
3		5.6	525			5.625
4		11	.25			11.25
5		16.8	3/5			16.875
7		20.	2.0			22.0
8		20.	75			33.75
9		39.3	375			39.375
10			45			45
11		50.6	525			50.625
12		56	.25			56.25
13		61.8	375			61.875
15		73	7.5			73 125
16		78	75			78.75
17		84.3	375			84.375
18			90			90
19		95.6	525			95.625
20		101	.25			101.25
21		106.8	3/5			106.875
23		118 1	2.5			118 125
24		123	75			123 75
25		129.3	375			129.375
26			135			135
27		140.6	525			140.625
28		146	.25			146.25
29		151.8	375			151.875
30		100	7.5			107.5
32		163.	75			168 75
33		174.3	375			174.375
34			180			180
35		185.6	525			185.625
36		191	.25			191.25
37		196.8	375			196.875
39		208 -	2.0			202.5
40		213	75			213 75
41		219.3	375			219.375
42		2	25			225
43		230.6	525			230.625
44		236	.25			236.25
45		241.8	75			241.875
40		253	125			253.125
48	1	258	.75			258.75
49		264.3	375			264.375
50		2	270			270
51		275.6	525			275.625
52		281	25			281.25
50		200.0	25			200.075
55		298 1	125			298.125
56		303	.75			303.75
57		309.3	375			309.375
58		:	315			315
59		320.6	525			320.625
60		326	.25			326.25
62		331.b วว	75			331.875
63		343	125			343 125
64		348	.75			348.75
65		354.3	375			354.375

Figure 12. Transmitter and Receiver Phase SRAM .CSV File

BYPASS MODE

For first time evaluation, it is recommended to use bypass beam pointer mode. This mode allows simplified and efficient evaluation of the gain and phase for each channel.

The following is an example of how to turn on a single transmitter channel (Channel 0) and adjust the gain in bypass mode (see Figure 9):

- 1. Choose Bypass Beam Pointer SRAM from the BeamPointer SRAM dropdown list.
- Select the Same Values for all channels checkbox. Set the power amplifier power to off in all channels settings. All 16 transmitter channel power amplifiers are switched to off.
- 3. In the Channel 0 row, set the power amplifier power to on and click Write PA Power to have only Transmit Channel 0 on.

4. Choose the Common Gain Offset, Channel Gain SRAM Index, and Channel Phase SRAM Index values. The real gain level and phase value are shown in the Channel Gain Level and Phase columns.

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 Click Write Tx Channel and Common Gain and Phase to load the new gain and phase settings (see Figure 9). If multiple channels must be set together, use the Select Channel section to enable or disable certain channels. See the AN-2021 Application Note, ADMV4801/ADMV4821 SPI Application Note for implementation details.

BEAM POINTER MODE AND BEAM POSITION SRAM

Beam pointer mode allows fast switching between 256 user defined beam positions, and only a single register is used to recall the beam position. Choose **Use Beam Pointer SRAM** from the **Beam**-

Pointer SRAM dropdown list on the ACE home page to enable beam pointer mode. Several sections turn grey, as shown in Figure 13. These blocks are defined in the beam settings SRAM.

To configure the beam settings SRAM, click **Navigate to SRAM Tables**. The beam settings SRAM table is shown in Figure 10.

Similar to the gain and phase SRAM, use the export or import .CSV file function instead of modifying the beam settings SRAM directly in the GUI. Click the export icon and then save the .CSV file to any local directory. See Figure 14 for the correct .CSV file. In the spreadsheet, Row 2 to Row 257 corresponds to Beam Settings Index 0 through Beam Settings Index 255.

The beam settings SRAM table stores up to 256 beam settings for all 16 channels. Each beam setting includes gain states indexes,

phase states indexes, transmit or receive mode (TRX) settings, and transmit common gain settings for all 16 channels. The gain and phase settings in each beam position recall the user defined gain and phase states SRAM shown in the Transmitter and Receiver Gain and Phase States SRAM section.

Table 7 describes the usage for each column in the .CSV file, and Table 8 describes the functionality of each block in beam pointer mode.

When the updated gain settings import, click the **Write to SRAM** button shown in Figure 10 to load the new settings to the device.

Click the **Fill SRAM Tables** button shown in Figure 10 to reset the gain and phase to default values.



Figure 13. Beam Pointer SRAM Mode



Figure 14. Beam Settings SRAM .CSV File

Table 7. Beam	Settings S	preadsheet	(see Figure 14)
---------------	------------	------------	-----------------

Column	Functionality
BP_CG_Addrx	Channel gain settings, each cell stores the gain states index, where x refers to the specific channel from Channel 0 to Channel 15.
BP_PH_Addrx	Channel Phase settings, each cell stores the phase states index, where x refers to the specific channel from Channel 0 to Channel 15.
TRX_Polarization_SRAM_V,	Transmit and receive settings for vertical (even) and horizontal (odd) polarization channels. This setting specifies whether the beam
TRX_Polarization_SRAM_H	position is set to transmitter mode or receiver mode. The ACE software forces the first 128 beam positions to be placed in transmitter
	mode, while the other 128 beam positions are placed in receiver mode. The ACE software does not provide access to change the TRX

Table 7. Beam Settings Spreadsheet (see Figure 14)

Column	Functionality
	SRAM, but the TRX SRAM can be changed in a customized application. Refer to the AN-2021 Application Note, ADMV4801/ADMV4821 SPI Application Note for more details.
Common_Gain_SRAM_V, Com- mon_Gain_SRAM_H	Transmitter common gain setting for vertical and horizontal channels from 0 dB to 17 dB in 1dB steps.

Table 8. Block Functionality for Beam Pointer Mode (see Figure 13)

Label	Function
0	Beam Pointer, scroll up or down to specify which beam position to use.
P1	Click Write Common Gain Offset and VGA Type to load the common gain and VGA setting to the device. It is not recommended to click Apply Changes.
P2	Click Write PA Power to load the power amplifier setting to the device. It is not recommended to click Apply Changes.
P3	Click Write LNA Attn Values to load the low noise amplifier (LNA) attenuation values to the device. It is not recommended to click Apply Changes.
P4	Click Read Beam Pointer to read back from the device.
P5	Click Write Beam Pointer to load the beam pointer to the device.

TEMPERATURE SENSOR AND POWER DETECTOR

Click **TempSensor and Tx Detectors** (see Label E in Figure 9) to open the temperature sensor and power detector window shown in Figure 15. The temperature sensor and power detectors are sampled by the on-chip analog-to-digital converter (ADC) and can be read back from the SPI. Note that the ADC is only available in transmitter mode. Therefore, the temperature sensor and power detector data only shows transmitter mode status.

Table 9 describes the functionality of each block in the temperature sensor and power detector window.

Label	Function
Q	Choose the channel and estimated power range from the Select Channel and TX Detector Range dropdown lists. Refer to the ADMV4821 data sheet for the detector characteristics. The TX Detector Readback column lists the ADC readback value.
R	The Approximate Temperature value is the real estimated temperature based on the ADC readback.
S	Click Readback Temperature and Detectors to read back the values.
Т	Click Return To Main Block to return to the main ACE software page.
U	Select the Use Same Pointer checkbox to set all 16 channels together.
V	The ADC Temperature Value is the readback from the ADC.
W	Click Reset Chip to reset the device.



Figure 15. Temperature Sensor and Power Detector Window



Figure 16. ADMV4821-EVALZ Evaluation Board Schematic, Page 1



Figure 17. ADMV4821-EVALZ Evaluation Board Schematic, Page 2











Figure 21. ADMV4821-EVALZ, Layer 2



Figure 23. ADMV4821-EVALZ, Layer 4



Figure 25. ADMV4821-EVALZ, Bottom Layer

CONFIGURATION OPTIONS

BILL OF MATERIALS

Table 10.

Qty	Reference Designator	Description	Manufacturer	Part Number
3	1P8, 3P3, 5V	Printed circuit board (PCB) connector test points, red	Components Corpora- tion	TP-104-01-02
18	C1, C2, C5 to C9, C12, C17 to C20, C27, C29, C30, C32, C41, C43	Ceramic capacitors, X5R, 4.7 µF	Murata	GRM155R60J475ME87D
3	C10, C24, C25	Ceramic capacitors, multilayer, X5R, 3.3 µF	ТДК	C1005X5R1A335M
7	C11, C70 to C75	Ceramic capacitors, X7R, broadband, 0.1 μF	American Technical Ce- ramics	530L104KT16T
9	C3, C4, C13 to C16, C28, C31, C42	Ceramic capacitors, multilayer NP0, high tempera- ture, 100 pF	TDK	C1005NP01H101J050BA
11	C21 to C23, C33, C49 to C52, C61 to C63	Ceramic capacitors, X5R, 10 µF	Samsung	CL05A106MP5NUNC
1	C26	Ceramic capacitor, X7R, broadband, 0.1 μF	American Technical Ce- ramics	530L104KT16T
8	C34, C35, C40, C44, C53 to C56	Ceramic capacitors, X5R, 1 µF	Samsung	CL05A105KA5NQNC
4	C36 to C39	Do not install	Not applicable	Not applicable
8	C45 to C48, C57 to C60	Ceramic capacitors, X5R, 0.15 µF	AVX	04026D154KAT2A
3	C64 to C66	Ceramic chip capacitors, X8R, 0.01 µF	TDK	C1005X8R1E103K
3	C67 to C69	Ceramic monolithic chip capacitors for automotive, C0G, 100 pF	Murata	GCM1555C1H101JA16D
3	C76 to C78	Ceramic capacitors, X7R, 4.7 µF	Kemet	C1206C475K3RACTU
18	CH0 to CH15, RFV, RFH	PCB coaxial connectors	Hirose Electric	HK-LR-SR2(12)
1	GND1	PCB connector test point, black	Components Corpora- tion	TP-104-01-00
1	J3	Board to board connector receptacle	Hirose Electric	FX8-120S-SV(21)
2	P1, P15	Connector headers	Samtec, Inc.	TSW-106-08-G-S
5	P6 to P10	Connector headers	Samtec	TSW-103-07-F-D
10	R1, R2, R5 to R7, R10, R12, R14, R26, R29	Do not install	Not applicable	Not applicable
12	R39 to R49, R100	Standard thick film resistors, 0 Ω	Vishay	CRCW06030000Z0EAHP
20	R3, R4, R11, R13, R15, R24, R28, R30, R31, R35 to R38, R74, R80 to R85	Thick film chip resistor jumpers, automotive, 0 $\boldsymbol{\Omega}$	Panasonic	ERJ-2GE0R00X
2	R16, R17	High stability, thin film chip resistors, 1.1 k Ω	Vishay	TNPW06031K10BEEA
11	R18, R22, R23, R58 to R61, R70 to R73	Thick film chip resistors, automotive, 1.5 $\boldsymbol{\Omega}$	Panasonic	ERJ-2GEJ1R5X
2	R19, R20	Thick film chip resistors, automotive, 0 $\boldsymbol{\Omega}$	VISHAY	CRCW04020000Z0EDHP
8	R21, R32 to R34, R76 to R79	Thick film chip resistors, automotive, 22 Ω	Panasonic	ERJ-2GEJ220X
2	R25, R27	Precision thick film chip resistors, 100 k Ω	Panasonic	ERJ-2RKF1003X
16	R50 to R57, R62 to R69	Resistors, automotive, 6.04 Ω	Vishay	CRCW04026R04FKED
1	R8	High stability flat chip resistor, 10 k Ω	Vishay	TNPW040210K0BEED
10	R86 to R95	Chip resistor jumpers, 0 Ω	Panasonic	ERJ-2GE0R00X
1	R9	Thin film chip resistor, 0 Ω	Multicomp (SPC)	MC 0.1W 0805 0R
1	R96	Precision thick film chip resistor, 49.9 k Ω	Panasonic	ERJ-3EKF4992V
1	R97	Precision thick film chip resistor, 18.2 k Ω	Panasonic	ERJ-3EKF1822V
1	R98	Precision thick film chip resistor, 200 k Ω	Panasonic	ERJ-3EKF2003V
1	R99	Film resistor, 220 kΩ	Multicomp (SPC)	MC 0.063W 0603 1%
1	RST	Mechanical keyswitch	OMRON	B3S1000
9	U1, U3 to U10	LDO regulators	Analog Devices	ADM7171ACPZ-3.3-R7

CONFIGURATION OPTIONS

Table 10.

Qty	Reference Designator	Description	Manufacturer	Part Number
1	U11	IC, 24 GHz to 29.5 GHz beamformer, 16-inch, single polarization	Analog Devices	ADMV4821BCCZ
3	U12 to U14	ICs, low volume, dual supply, 4-bit signal transla- tors	Fairchild Semiconductor	FXL4TD245BQX
1	U15	IC, 20 V, 200 mA, ultralow noise, ultrahigh power supply rejection ratio (PSRR), RF linear regulator	Analog Devices	LT3042EDD#PBF
1	U2	Electrically erasable programmable read-only memory (EEPROM)	Microchip Technology	24LC32A-I/MS



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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