REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

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TITLE

MICROCIRCUIT, DIGITAL-LINEAR, DIGITALLY TUNABLE, 2 GHZ TO 18 GHZ, HIGH PASS AND LOW PASS FILTER, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/21604

REV	PAGE 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance digitally tunable, 2 GHz to 18 GHz, high pass and low pass filter microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21604	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADMV8818-EP	Digitally tunable, 2 GHz to 18 GHz, high pass and low pass filter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	56	See figure 1	Land grid array (LGA) with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltages:	
V_{DD1}	-0.3 V to +2.8 V
V_{DD2}	-0.3 V to +3.6 V
V_{SS1}	-3.6 V to +0.3 V
Digital control inputs:	
Voltage	-0.3 V to V_{DD2} + 0.3 V
Current	2 mA
RF input power	20 dBm 2/
Temperature:	
Operating range	-55°C to +105°C
Storage temperature range (T_{STG})	-65°C to +150°C
Junction to maintain 1,000,000 hours mean time to failure (MTTF)	135°C
Nominal junction (T_{PADDLE} = 85°C)	90°C
Moisture sensitivity level (MSL) rating	MSL3
Electrostatic discharge (ESD) rating:	
Human body model (HBM) per JEDEC JS-001	2,000 V
Field induced charge device model (FICDM) :	
Per JEDEC JEDS22-C101	500 V
Per JEDEC JS-002	750 V

1.4 Recommended operating conditions. 3/

Operating temperature range (T_A)	-55°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Maximum RF input power valid for frequencies above 1 GHz. For incident signals below this frequency, contact the manufacturer.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JEDEC JS-002	–	Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency range (f3db)		3 dB cutoff					
Bypass configuration			+25°C	01	2	18	GHz
HPF 1, state 0			+25°C	01	1.75 typical		GHz
HPF 1, state 15			+25°C	01	3.55 typical		GHz
HPF 2, state 0			+25°C	01	3.40 typical		GHz
HPF 2, state 15			+25°C	01	7.25 typical		GHz
HPF 3, state 0			+25°C	01	6.60 typical		GHz
HPF 3, state 15			+25°C	01	12.00 typical		GHz
HPF 4, state 0			+25°C	01	12.50 typical		GHz
HPF 4, state 15			+25°C	01	19.90 typical		GHz
LPF 1, state 0			+25°C	01	2.05 typical		GHz
LPF 1, state 15			+25°C	01	3.85 typical		GHz
LPF 2, state 0			+25°C	01	3.35 typical		GHz
LPF 2, state 15			+25°C	01	7.25 typical		GHz
LPF 3, state 0			+25°C	01	7.00 typical		GHz
LPF 3, state 15			+25°C	01	13.00 typical		GHz
LPF 4, state 0			+25°C	01	12.55 typical		GHz
LPF 4, state 15			+25°C	01	18.85 typical		GHz
Insertion loss							
Bypass configuration, 2 GHz			+25°C	01	-3.2 typical		dB
Bypass configuration, 10 GHz			+25°C	01	-4.4 typical		dB
Bypass configuration, 18 GHz			+25°C	01	-6.0 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Insertion loss – continued.							
2 GHz to 6 GHz		HPF 1 state 2 and LPF 2 state 11	+25°C	01	-7.3 typical		dB
6 GHz to 10 GHz		HPF 2 state 11 and LPF 3 state 8	+25°C	01	-8.6 typical		dB
10 GHz to 14 GHz		HPF 3 state 10 and LPF 4 state 5	+25°C	01	-11.8 typical		dB
14 GHz to 18 GHz		HPF 4 state 5 and LPF 4 state 13	+25°C	01	-14.6 typical		dB
Bandwidth (3 dB)		Small bandwidth possible with more insertion loss.					
2 GHz to 10 GHz			+25°C	01	0.5 to 4 typical		GHz
10 GHz to 18 GHz			+25°C	01	1 to 4 typical		GHz
Resolution		4 bits per filter (LPF and HPF)					
HPF 1			+25°C	01	0.12 typical		GHz
HPF 2			+25°C	01	0.26 typical		GHz
HPF 3			+25°C	01	0.36 typical		GHz
HPF 4			+25°C	01	0.49 typical		GHz
LPF 1			+25°C	01	0.12 typical		GHz
LPF 2			+25°C	01	0.26 typical		GHz
LPF 3			+25°C	01	0.40 typical		GHz
LPF 4			+25°C	01	0.42 typical		GHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Wideband rejection frequency offset. Measured at 35 dB rejection							
HPF 1, state 0			+25°C	01	-0.65 typical		ΔGHz
HPF 1, state 15			+25°C	01	-1.25 typical		ΔGHz
HPF 2, state 0			+25°C	01	-0.85 typical		ΔGHz
HPF 2, state 15			+25°C	01	-2.00 typical		ΔGHz
HPF 3, state 0			+25°C	01	-1.15 typical		ΔGHz
HPF 3, state 15			+25°C	01	-1.90 typical		ΔGHz
HPF 4, state 0			+25°C	01	-2.35 typical		ΔGHz
HPF 4, state 15			+25°C	01	-3.10 typical		ΔGHz
LPF 1, state 0			+25°C	01	0.70 typical		ΔGHz
LPF 1, state 15			+25°C	01	1.00 typical		ΔGHz
LPF 2, state 0			+25°C	01	0.90 typical		ΔGHz
LPF 2, state 15			+25°C	01	1.60 typical		ΔGHz
LPF 3, state 0			+25°C	01	2.30 typical		ΔGHz
LPF 3, state 15			+25°C	01	3.20 typical		ΔGHz
LPF 4, state 0			+25°C	01	2.50 typical		ΔGHz
LPF 4, state 15			+25°C	01	3.95 typical		ΔGHz
Re-entry frequency		≤ 35 dB	+25°C	01	32 typical		GHz
Return loss			+25°C	01	10 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance							
Input power for 0.1 dB compression	P0.1dB		+25°C	01	18 typical		dBm
Input third order intercept	IP3	Input power (PIN) = 5 dBm per tone 2/	+25°C	01	45 typical		dBm
Group delay flatness			+25°C	01	< 0.8 typical		ns
Amplitude settling time		To within ≤1 dB static insertion loss	+25°C	01	1 typical		µs
Phase settling time		To within ≤2° static insertion phase	+25°C	01	2 typical		µs
Drift rate, amplitude		At 8 GHz	+25°C	01	-0.018 typical		dB/°C
Drift rate, frequency		6 GHz to 10 GHz constant bandwidth state	+25°C	01	-100 typical		ppm/°C
Residual phase noise at 1 MHz offset			+25°C	01	-165 typical		dBc/Hz
Supply voltage	VSS1		+25°C	01	-2.5 typical		V
					-2.6	-2.4	
Supply voltage	VDD1		+25°C	01	2.5 typical		V
					2.4	2.6	
Supply voltage	VDD2		+25°C	01	3.3 typical		V
					3.2	3.4	
Supply current (Static)	VSS1		+25°C	01	-50		µA
Supply current (Static)	VDD1		+25°C	01		200	µA
Supply current (Static)	VDD2		+25°C	01		50	µA
Supply current (Dynamic)	VDD2	Where f_{SCLK} is the SCLK toggle frequency in MHz, for example, continuous SPI writing at 10 MHz yields 5 mA of dynamic supply current	+25°C	01	f_{SCLK}/2 typical		mA
Logic ($\overline{RST}$, $\overline{CS}$, SCLK, SDI, SD0, SFL)							
Logic low			+25°C	01	0 typical		V
					-0.3	+0.8	
Logic high			+25°C	01	3.3 typical		V
					1.2	3.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications		See figure 4					
$\overline{RST}$ low time to perform reset	t_1		-55°C to +105°C	01	10		ns
SCLK cycle time (write)	t_2		-55°C to +105°C	01	10		ns
SCLK cycle time (read)					20		
SCLK high time	t_3		-55°C to +105°C	01	2.5		ns
SCLK low time	t_4		-55°C to +105°C	01	2.5		ns
$\overline{CS}$ falling edge to SCK rising edge setup time	t_5		-55°C to +105°C	01	5		ns
SCLK rising edge to $\overline{CS}$ hold time	t_6		-55°C to +105°C	01	2		ns
Minimum $\overline{CS}$ high time for latching in data (for multiple SPI transactions)	t_7		-55°C to +105°C	01	5		ns
$\overline{CS}$ rising edge to next SCLK rising edge ignore	t_8		-55°C to +105°C	01	5		ns
SDI data setup time	t_9		-55°C to +105°C	01	5		ns
SDI data hold time	t_{10}		-55°C to +105°C	01	2		ns
SFL falling edge (existing SFL mode) to $\overline{CS}$ falling edge time (start SPI transaction)	t_{11}		-55°C to +105°C	01	10		ns
$\overline{CS}$ rising edge (end SPI transaction) to SFL rising edge time (entering SFL mode)	t_{12}		-55°C to +105°C	01	10		ns
SFL rising edge to $\overline{CS}$ falling edge time	t_{13}		-55°C to +105°C	01	10		ns
$\overline{CS}$ cycle time (SFL mode)	t_{14}		-55°C to +105°C	01	10		ns
$\overline{CS}$ high time (SFL mode)	t_{15}		-55°C to +105°C	01	2.5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications – continued.		See figure 4					
$\overline{CS}$ low time (SFL mode)	t_{16}		-55°C to +105°C	01	2.5		ns
SCLK falling edge to SDO valid	t_{17}	Load capacitance (C_L) = 10 pF	-55°C to +105°C	01	6 typical		ns
SDO rise and fall time	t_{18}	C_L = 10 pF	-55°C to +105°C	01	5 typical		ns
$\overline{CS}$ rising edge to SDO tristate	t_{19}	C_L = 10 pF	-55°C to +105°C	01	4 typical		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ When the insertion loss is less than -20 dB, P_{IN} = 8 dBm per tone.

Case X

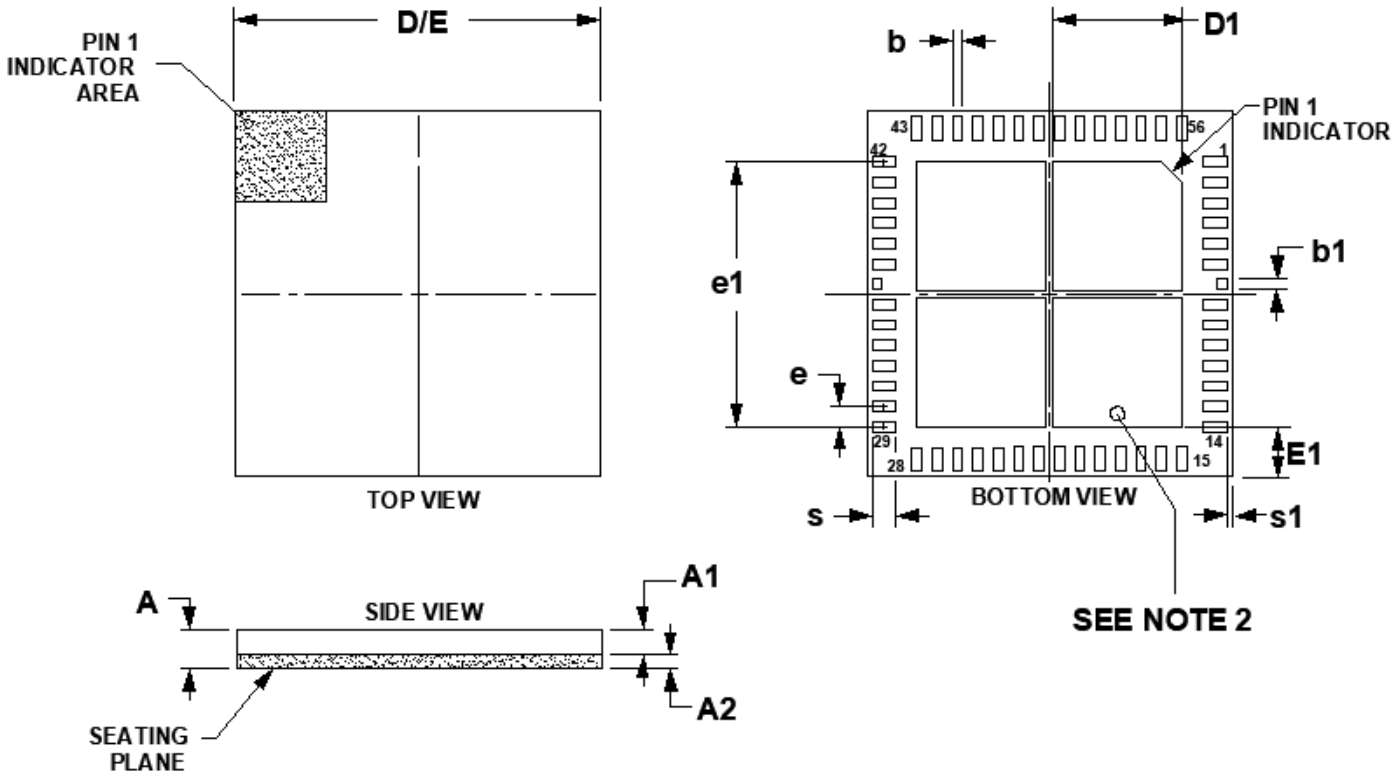

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/21604
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Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.036	.038	.040	0.91	0.97	1.03
A1	.021 REF			0.53 REF		
A2	.015	.017	.019	0.398	0.438	0.478
b	.009	.010	.011	0.22	0.25	0.28
b1	.009 SQ	.010 SQ	.011 SQ	0.22 SQ	0.25 SQ	0.28 SQ
D/E	.348	.354	.360	8.85	9.00	9.15
D1	.123	.124	.125	3.12	3.15	3.18
E1	.049 REF			1.25 REF		
e	.020 BSC			0.50 BSC		
e1	.256 SQ			6.50 SQ		
s	.024	.025	.027	0.62	0.65	0.68
s1	.004 REF			0.10 REF		

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pads. Refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Exposed pad. The exposed pad must be connected to the RF and dc ground.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	29	GND
2	GND	30	GND
3	GND	31	VDD1
4	GND	32	GND
5	GND	33	GND
6	GND	34	GND
7	RFIN	35	GND
8	GND	36	RFOUT
9	GND	37	GND
10	GND	38	GND
11	GND	39	VDD2
12	GND	40	GND
13	GND	41	VSS1
14	$\overline{\text{RST}}$	42	GND
15	GND	43	GND
16	SCLK	44	GND
17	GND	45	GND
18	$\overline{\text{CS}}$	46	GND
19	GND	47	GND
20	SDO	48	GND
21	GND	49	GND
22	SDI	50	GND
23	GND	51	GND
24	SFL	52	GND
25	GND	53	GND
26	GND	54	GND
27	GND	55	GND
28	GND	56	GND

FIGURE 2. Terminal connections.

Terminal symbol	Description
GND	Ground. Connect the GND pins to the RF and dc ground.
RFIN	RF Input Pin. RFIN is dc-coupled and matched to 50 Ω. Do not apply an external voltage to RFIN.
$\overline{\text{RST}}$	Chip Reset. 3.3 V logic. Active low. The $\overline{\text{RST}}$ pin is internally pulled high with a 260 kΩ resistor.
SCLK	Serial Peripheral Interface (SPI) Clock. 3.3 V logic. The SCLK pin is internally pulled low with a 260 kΩ resistor.
$\overline{\text{CS}}$	SPI Chip Select. 3.3 V logic. Active low. The $\overline{\text{CS}}$ pin is internally pulled low with a 260 kΩ resistor.
SDO	SPI Data Output. 3.3 V logic. The SDO pin is internally pulled low with a 260 kΩ resistor.
SDI	SPI Data Input. 3.3 V logic. The SDI pin is internally pulled low with a 260 kΩ resistor.
SFL	SPI Fast Latch Enable. 3.3 V logic. Set SFL high to enable fast latching of filter states on each rising edge of $\overline{\text{CS}}$. While SFL is in this mode, the SCLK, SDO, and SDI pins are not active. The SFL pin is internally pulled low with a 260 kΩ resistor.
VDD1	2.5 V Power Supply Pin. Place 0.1 µF and 100 pF decoupling capacitors close to VDD1.
RFOUT	RF Output Pin. RFOUT is dc-coupled and matched to 50 Ω. Do not apply an external voltage to RFOUT.
VDD2	3.3 V Power Supply Pin. Place 0.1 µF and 100 pF decoupling capacitors close to VDD2.
VSS1	–2.5 V Power Supply Pin. Place 0.1 µF and 100 pF decoupling capacitors close to VSS1.
EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground.

FIGURE 2. Terminal connections – Continued.

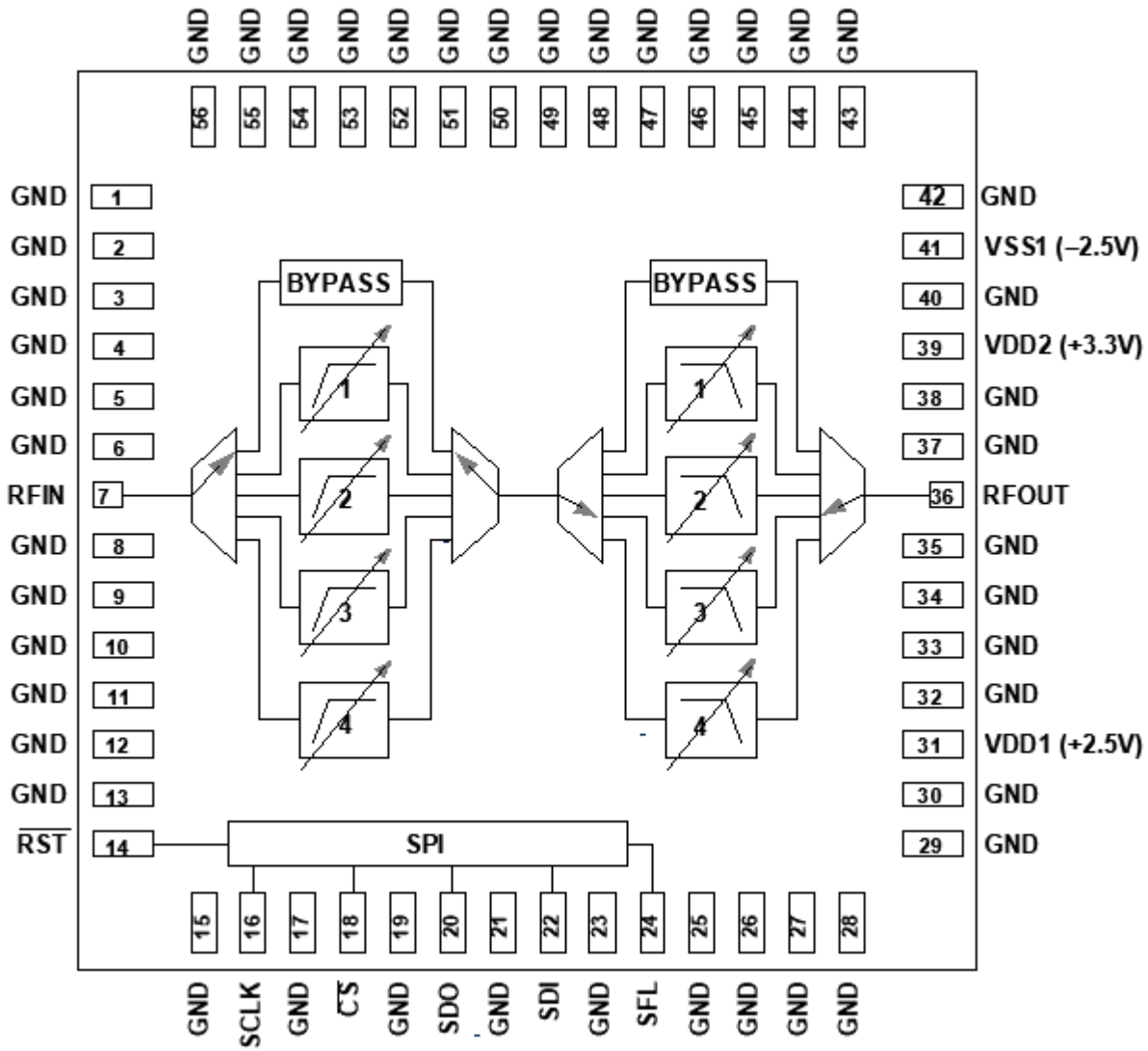

FIGURE 3. Functional block diagram.

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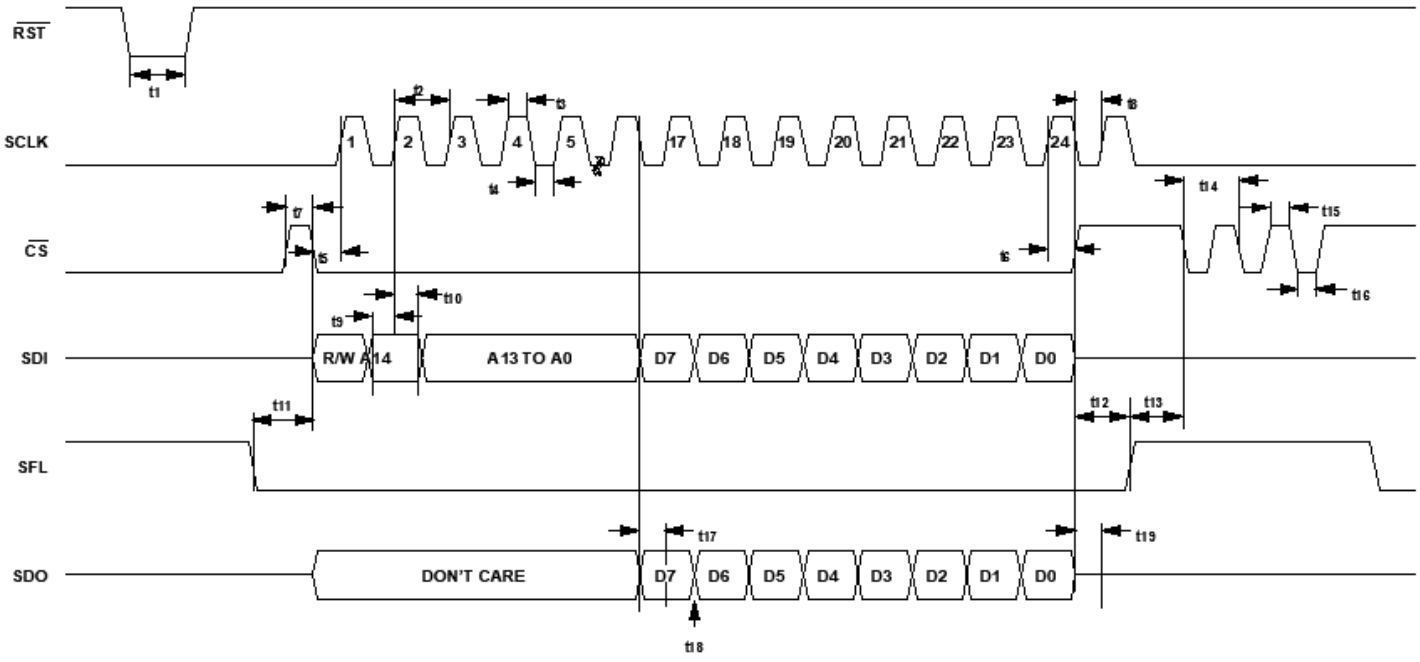

FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21604-01XE	24355	Tray, 260 units	ADMV8818	ADMV8818SCCZ-EP
		Reel, 250 units	ADMV8818	ADMV8818SCCZ-EP-R2
		Tape, 1 unit	ADMV8818	ADMV8818SCCZ-EP-P7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123