Optical Evaluation Kit for the ADN2525

EVAL-ADN2525-NT/ADN2525-OP

GENERAL DESCRIPTION

This data sheet describes the optical evaluation kit for the ADN2525, a 10 Gbps, active back-termination, differential laser diode driver. The differential configuration of the output stage combined with on-chip active back-termination ensures high quality eye diagrams at lower power consumption compared with traditional approaches on 10 Gbps laser diode drivers. Complete specifications can be found in the ADN2525 data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this data sheet when using the evaluation board. The EVAL-ADN2525-OP evaluation kit consists of an evaluation board that provides optical evaluation of the ADN2525 with an Opnext 10 Gbps 1310 nm TOSA (LD5033SMDL). The EVAL-ADN2525-NT evaluation kit consists of the same evaluation board without a TOSA attached.

To evaluate the performance of the ADN2525, the board must be connected to the test setup as shown in Figure 1. A fiber patch cord with an appropriate connector for the TOSA end is required to connect the TOSA to the oscilloscope.

The power supply must be able to deliver 400 mA at 3.3 V. The amplitude of the data signal from the pattern generator must be adjusted to within the ADN2525 data sheet specifications for data inputs, typically 1 V peak-to-peak differential (500 mV single-ended on DATAP and DATAN). The oscilloscope/digital communications analyzer must have a 1310 nm optical channel that can accept and display properly the optical signals generated by the TOSA.

The coaxial cables used to connect the pattern generator to the evaluation board DATAP/DATAN inputs must be suitable for carrying 10 Gbps signals without significant reduction of rise/fall time or introduction of pattern jitter. They should also be a matched pair with a delay skew of ≤2 ps. An example of suitable cables is the 60 cm Lab-Flex® 160 cables with 2.4 mm connectors from Florida RF Labs.

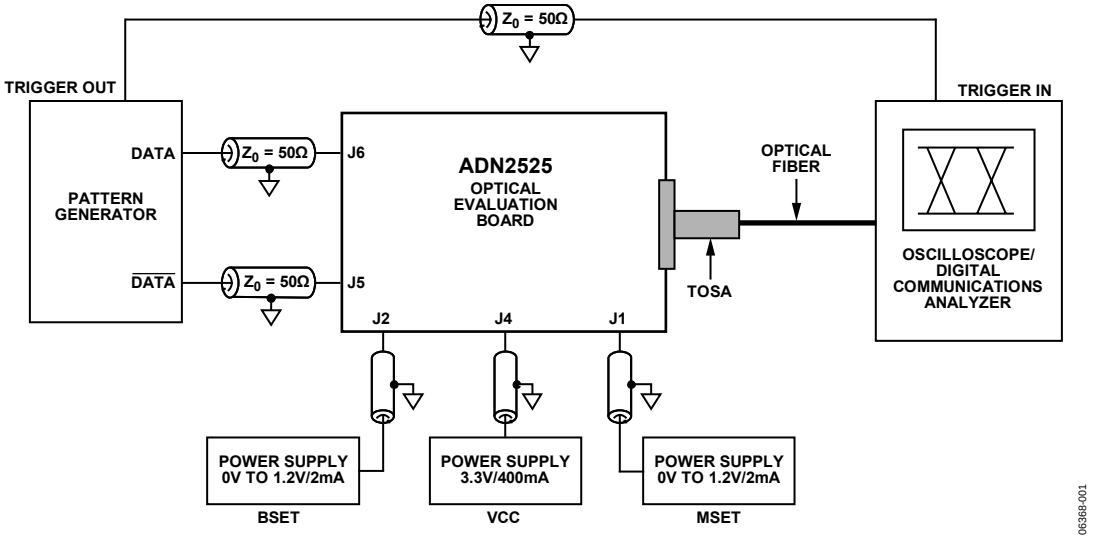

Figure 1. ADN2525 Optical Evaluation Board Test Setup

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

7/07—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

CONNECTORS

The ADN2525 is capable of delivering an 80 mA differential modulation current and 100 mA bias current. Applying dc voltages to the ADN2525 BSET and MSET pins sets the bias and modulation currents. The board is set up so that the outputs of the ADN2525 are ac-coupled to the TOSA. The board is fitted with connectors that allow the user to connect the evaluation board to the test setup. Table 1 describes the name and function of each connector on the board.

Table 1. Connector Description

Connector	Description
J1	Allows the user to apply an external dc voltage source to control the differential modulation current provided by the ADN2525.
J2	Allows the user to apply an external dc voltage source to control the bias current provided by the ADN2525.
J3	Automatic Laser Shutdown. Allows the user to enable/disable the bias and modulation current by applying a low/high logic level (not greater than VCC).
J4	Power Supply Connector. The board supply voltage is 3.3 V with respect to GND.
J5	Negative data input. A PECL/CML data signal should be applied.
J6	Positive Data Input. A PECL/CML data signal should be applied.
J9	25 Ω Test Transmission Line.

TERMINALS

The evaluation board accommodates the terminal assignment of the multisource agreement for the 10 Gbps XMD miniature device (EVAL-ADN2525-OP).

Table 2. XMD MSA TOSA Terminal Function Definition

Terminal Number	Option 1	Option 2
1	PD Cathode	PD Cathode
2	Signal Ground	Signal Ground
3	LD Cathode	LD Cathode
4	LD Anode	LD Anode
5	Signal Ground	Signal Ground
6	Thermistor	NC

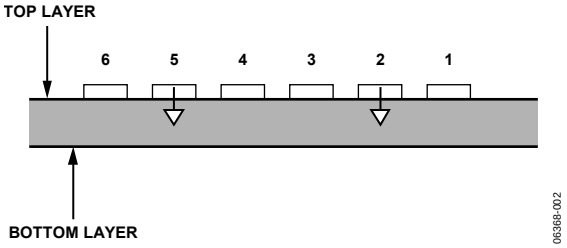

Figure 2. Pinout of TOSA Footprint on PCB (Looking Toward the Edge of the Board Cross Section)

For additional optical eye diagram performance data and for information on optimizing the performance of the evaluation board for different TOSAs, contact a local Analog Devices representative.

JUMPERS

Automatic laser shutdown is configurable, driven either by voltages generated on the board or by external voltages as described in Table 3.

Table 3. Jumper Configurations

Jumper	Jumper Setting	Configuration Description
P4	A	Enables the bias and differential modulation currents.
	B	Disables the bias and differential modulation currents.
	Removed	Allows the user to enable/disable the bias and differential modulation currents by applying a low/high logic level to J3 from an external source.

QUICK START FOR OPTICAL EVALUATION

1. If using evaluation kit EVAL-ADN2525-NT, solder a TOSA to the evaluation board, following soldering guidelines in the TOSA data sheet.
2. If required, change the ALS jumper settings to obtain the desired configuration, using Table 3.
3. Connect the evaluation board to an oscilloscope, pattern generator, and power supplies as shown in Figure 1. A suitable pattern generator is the Anritsu MP1763B and a suitable oscilloscope is the Agilent 86100B with 86105C optical plug-in. Use coaxial cables for DATAP and DATAN of the type recommended in the General Description section.
4. Run any applicable user calibrations on the oscilloscope optical input.
5. Turn on the power supply (3.3 V) connected to J4. Check that the current drawn from the 3.3 V power supply is within the limits of the I_{SUPPLY} specifications in the ADN2525 data sheet.
6. Increase the voltage applied to J2 starting from 0 V until the desired optical average power is obtained.
7. Increase the voltage applied to J1 starting from 0 V until the desired extinction ratio is obtained.
8. To prevent damage to the TOSA, it is advisable to gradually adjust the BSET and MSET voltages back to 0 V before turning off the power supplies.

Using the EVAL-ADN2525-OP Evaluation Kit

When using the EVAL-ADN2525-OP evaluation kit, it is recommended that the kit be initially set up to reproduce the sample optical eye diagram that is included with the kit. This confirms that the test setup is configured correctly to produce a high quality optical eye diagram. The following steps should be followed to reproduce the sample optical eye diagram:

1. Set up the board following the recommendations in the Quick Start for Optical Evaluation section.
2. Adjust the data rate and pattern to the settings used in the sample optical eye diagram and select the appropriate optical filter and wavelength on the oscilloscope.
3. Adjust the BSET and MSET voltages to the settings used in the sample optical eye diagram.
4. Confirm that the VCC supply current (I_{CC}) and the IBMON voltage at TP1 are close to the values reported in the sample optical eye diagram. If either of the values is significantly different, this indicates that there is a problem with the test setup, evaluation board, or TOSA, and this should be investigated.
5. Confirm that the real average power is close to the value reported in the sample optical eye diagram. The real average power is the average power as measured by the test equipment plus the measured attenuation of any optical attenuators in the optical signal path. If the value is significantly different, this indicates that there is a problem with the test setup, evaluation board, or TOSA, and this should be investigated. Less significant differences can sometimes be attributed to one or more of the following:
   a. Dirt in the fiber connectors, optical attenuators, or oscilloscope optical input can cause errors in average power.
   b. Optical coupling can be quite variable at the TOSA because there is no latching mechanism for the fiber connector. By ensuring that the connector is fully inserted and rotating, the connector can eliminate small discrepancies in real average power.
   c. Calibration differences between the oscilloscope in the test setup and the oscilloscope used to measure the sample optical eye diagram can cause small discrepancies in measured average power.
6. Confirm that the extinction ratio is close to the value reported in the sample optical eye diagram. If the value is significantly different, this indicates that there is a problem with the test setup, evaluation board, or TOSA and this should be investigated. Because the extinction ratio is a sensitive measurement, small discrepancies can be attributed to using different oscilloscope or optical plug-in models or even different optical plug-ins of the same model.
7. Select the same eye mask and mask Y-alignment method as used in the sample optical eye diagram.
8. Select the same number of waveforms for the eye diagram capture as used in the sample optical eye diagram.
9. Confirm that the average mask margin is close to the value reported in the sample optical eye diagram. If the value is significantly different, this indicates that there is a problem with the test setup, evaluation board, or TOSA and this should be investigated. Differences can be attributed to one or more of the following:
   a. A poor quality differential electrical eye diagram at the output of the coaxial cables from the pattern generator results in a poor optical eye diagram. Measuring the electrical eye diagram on these signals confirms or eliminates this possibility. Delay skew >2 ps between the DATAP and DATAN signals is one example of a degraded input signal that leads to a degraded optical eye diagram.
   b. Small discrepancies can be attributed to using different oscilloscope or optical plug-in models or even different optical plug-ins of the same model. Different optical plug-in models have different bandwidths, noise, and time-base jitter and this can affect eye mask margin. Different optical plug-ins of the same model can have different frequency responses in the optical filter that is within the allowed tolerance and this can affect eye mask margin.
   c. If an optical attenuator is required to keep the eye diagram within the oscilloscope range, an attenuation value should be chosen that keeps the optical signal in the upper end of the oscilloscope range. Otherwise, the effect of oscilloscope noise on the eye mask margin is increased.

USING THE EVALUATION BOARD PCB LAYOUT IN AN OPTICAL TRANSMITTER DESIGN

The evaluation kit PCB is fabricated using FR4 (Polyclad PCL-FR-370HR) with 4.5 mil dielectric thickness between the top-side signal and ground layers. When using the evaluation board PCB layout as a guide for designing an optical transmitter, it is recommended that the same dielectric material and thickness be used and the PCB layout associated with the ADN2525, the ac-coupling components, and the TOSA be copied exactly. This includes features such as component pad positions and sizes, track widths and lengths, via sizes, and positions. These features affect the high frequency performance in ways that are difficult to predict; therefore, changing them increases the risk of losing some mask margin performance. Following this recommendation gives the highest likelihood that eye diagram performance measured on the evaluation board is reproduced in the optical transmitter (ignoring any performance loss contributed by retiming or other circuitry that precedes the ADN2525). It is possible that changing the PCB dielectric material or making small changes to the PCB layout causes negligible degradation in the performance or even improves the performance. However, this is difficult to predict.

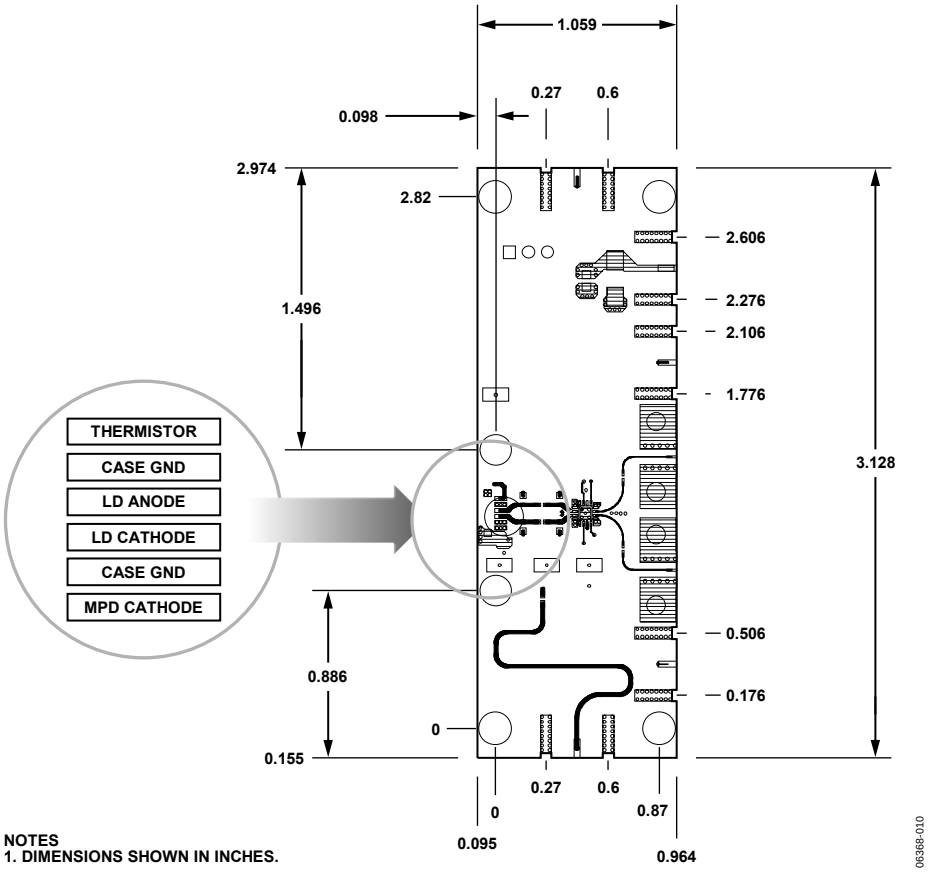

Figure 3. Evaluation Board Outline

EVALUATION BOARD SCHEMATICS AND ARTWORK

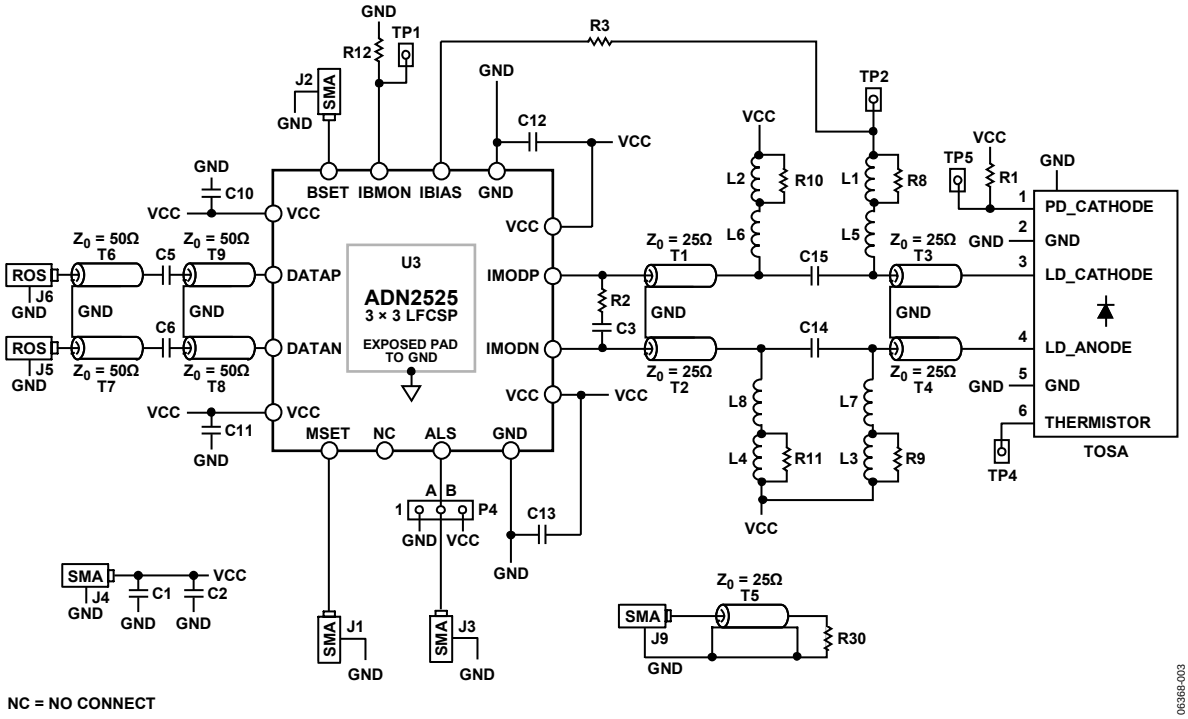

Figure 4. Schematic of Generation F Evaluation Board

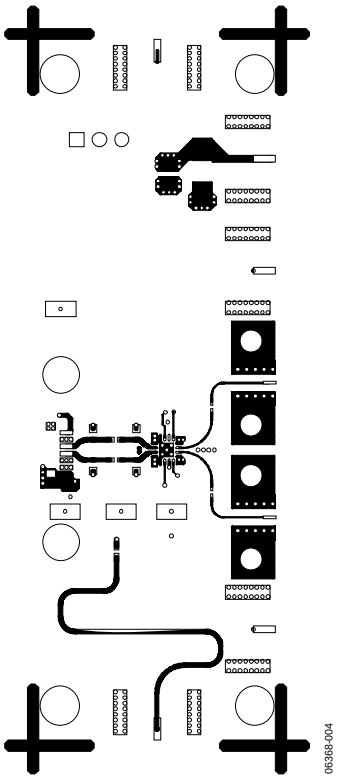

Figure 5. Layer 1 (Signal)

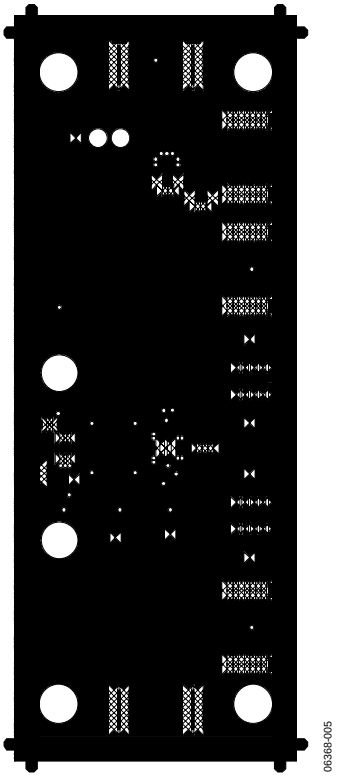

Figure 6. Layer 2 (GND)

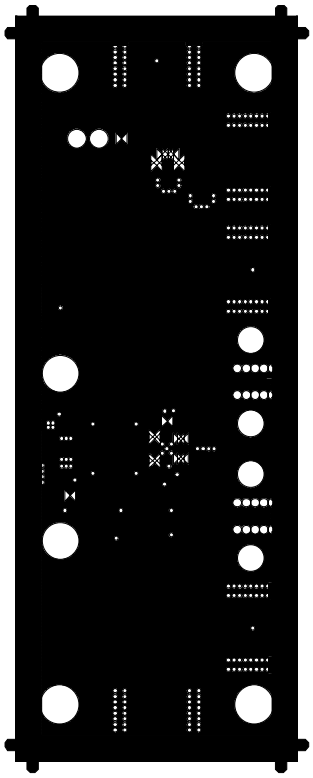

Figure 7. Layer 3 (VCC)

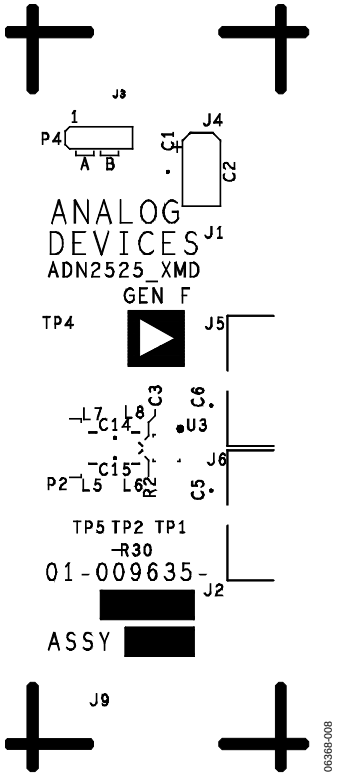

Figure 8. Layer 4 (Signal)

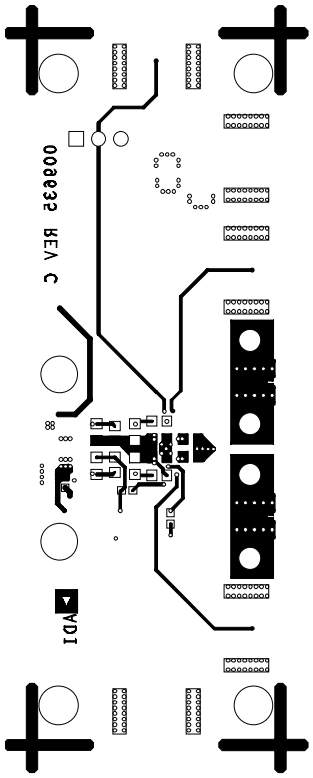

Figure 9. Silkscreen Top

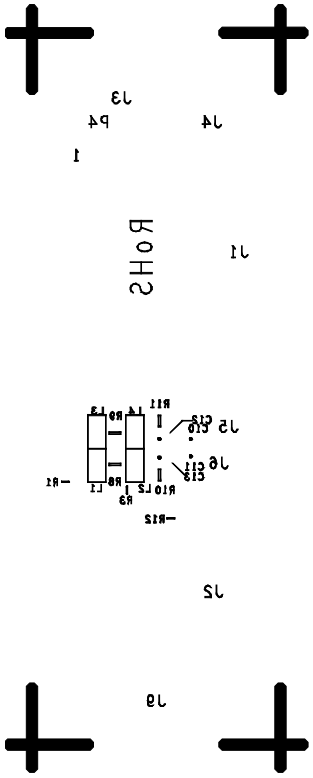

Figure 10. Silkscreen Bottom (Bottom View)

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty	Reference Designator	Description	Supplier/Number
2	R1, R3	0 Ω, 0402 size resistor	
2	R10, R11	10 Ω, 0603 size resistor	
2	R8, R9	100 Ω, 0603 size resistor	
2	C14, C15	1000 nF, 0402 size capacitor;	Panasonic ECJ-0EB0J105K
4	C10, C11, C12, C13	100 nF, 0402 size ceramic capacitor;	BC Components VJ0402V104ZXJCW1BC
3	C1, C5, C6	10 nF, 0402 size ceramic capacitor;	BC Components VJ0402Y103KXJCW1BC
2	L6, L8	18 nH, 0402 size inductor;	Murata LQW15AN20NJ0
2	L5, L7	0402 size ferrite	Murata BLM15HG102SN1
4	L1, L2, L3, L4	10 µH, 0805 size inductor	Murata LQM21FN100M70L
1	R2	33 Ω, 0201 size resistor; mounted upside-down	Panasonic ERJ-1GEF330C
1	C3	0.1 pF, 0201 size capacitor	AVX 02013J0R1PBWTR
1	C2	10 µF, Case-C tantalum capacitor	
1	P4	Jumper and 3-pin header	
1	R12	1 kΩ, 0603 size, 0.1% resistor	
1	R30	25 Ω, not populated	
2	J5, J6	2.92 mm connector	Rosenberger
4	J1, J2, J3, J4	Side-launch SMA connector	
1	U3	10.7 Gbps differential laser diode driver	Analog Devices ADN2525
1	TOSA (EVAL-ADN2525-OP only)	10 Gbps XMD TOSA	OpNext LD5033SMDL

ORDERING GUIDE

Model	Description
EVAL-ADN2525-OPZ[1]	Optical Evaluation Board with an XMD TOSA Populated
EVAL-ADN2525-NTZ[1]	Optical Evaluation Board Without an XMD TOSA Populated

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.