ANALOG DEVICES

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APPLICATION NOTE

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Acquisition Times of the ADN2812

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INTRODUCTION

When the ADN2812 is in its default operating mode, lock to input data mode, it will automatically lock to the incoming data pattern without programming and without the aid of external reference clocks. In this mode of operation, the acquisition time of the ADN2812 is dependent on the state of the inputs at the moment that the frequency acquisition begins. Following a software reset or if the input data is switched cleanly from one data rate to the next, the ADN2812 has a short acquisition time (e.g., ~1.2 ms @ 2.7 G). However, there are scenarios in which the acquisition time can be much longer, up to 300 ms. This application note details those different scenarios and provides a solution to reduce this long acquisition period to ~30 ms.

In Lock to Refclk mode, the ADN2812 locks with the aid of an external reference clock and has a 10 ms acquisition time, regardless of the state of the inputs prior to frequency acquisition.

The process that the ADN2812 goes through for a new frequency acquisition is as follows (an understanding of the architecture of the ADN2812 is required):

- The lock detector senses transitions at its input and determines the frequency of the incoming data has changed.
- LOL (Loss of Lock) is asserted and the frequency locked loop pulls the VCO to within 250 ppm of its intended frequency. At this point the LOL signal is de-asserted.
- Control of the VCO is handed over to the D/PLL to pull in the remaining 250 ppm of frequency error as well as align the phase of the incoming data with the VCO.

It is important to understand that the LOL signal of the ADN2812 was designed to be asserted when the FLL is in control of the VCO, and de-asserted when the D/PLL is in control of the VCO. This is because under normal operating conditions when the D/PLL takes control of the VCO, the frequency of the VCO is within 0.025% of its final value. The D/PLL will acquire the remaining 0.025% of frequency error as well as the phase. For all intents and purposes, when the D/PLL is in control of the VCO, the ADN2812 is essentially "locked."

FREQUENCY ACQUISITION WITH A VALID INPUT

In lock to data mode, if the input data at the PIN and NIN inputs to the ADN2812 is valid at the time that LOL is asserted to indicate a new frequency acquisition has been initiated, then the acquisition time (t_{ACQ}) will be as specified in the ADN2812 data sheet, e.g., t_{ACQ} = 1.3 ms at OC48 and is approximately 3.4 ms at OC3. This applies to the following conditions:

- Input data valid at the time of power-up.
- Input data valid following a software reset.
- A quick, clean switch from one data rate to the next, e.g., from a crosspoint switch (see Figure 1).

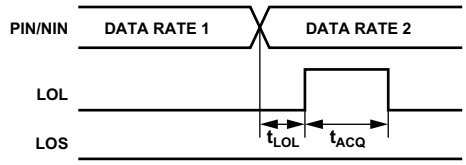

Figure 1. A Clean Data Rate Switch and Acquisition

A quick, clean switch can be considered any data rate switch that occurs where the subsequent signal level and data rate is valid prior to LOL triggering. This must occur within t_{LOL}, which is typically 1 μs for data rates higher than OC12 but could be as much as 4 ms for 12.5 Mb/s.

OTHER ACQUISITION SCENARIOS

The ADN2812 has a built-in "acquisition dead band" that following the initiation of a frequency acquisition will not allow a subsequent frequency acquisition to occur for ~300 ms. This dead band can be programmed to be ~30 ms which is explained later in this application note. There are two scenarios that could affect the acquisition time of the ADN2812.

1. When the valid data goes away, it is followed by a period of noise prior to a new, valid data stream being present at the ADN2812 inputs.
2. When the valid data goes away, it is followed by no signal with nothing that would be perceived by the ADN2812 as transitions—basically, a constant stream of zeroes.

In scenario one, the valid data goes away and is followed by noise. The ADN2812 will perceive this as high frequency data. The lock detector will detect these high frequency transitions, realize that the data rate at the input to the ADN2812 has changed, assert the LOL signal, and initiate a new frequency acquisition. At this point, there is an internal *acquisition dead band* that will not allow another frequency acquisition to occur for up to 300 ms.

The ADN2812 begins every frequency acquisition at the bottom of its range, ~5 MHz. In a situation where there is high frequency noise present at the input, the frequency locked loop will quickly drive the VCO to the top of its range, ~2.8 GHz. At this point, the VCO can go no higher and the ADN2812 will still not be locked. Once the acquisition dead band expires, the lock detector will detect that the ADN2812 is still not locked and a new frequency acquisition will be initiated. This cycle will repeat itself as long as there is noise at the input to the ADN2812. The time of this cycle will be between ~150 ms and ~300 ms and is dictated by the internal timeout and dead band circuits.

If the data becomes valid at any point after the ADN2812 has already begun attempting to lock to noise, the dead bands will still need to expire in order for an acquisition of the valid data to take place. This is because the frequency acquisition always starts from the bottom of the VCO's range and only goes in one direction. So, if the VCO is attempting to lock to noise and quickly ramps up to the top of its range, even if a valid data signal appears prior to the dead band expiring, at 622 Mb/s for example, the ADN2812 will not be able to reverse the VCO's acquisition direction. The dead band must expire and a new acquisition must be initiated from the bottom of the VCO range so that the valid 622 Mb/s data can be acquired.

In scenario two, if the data is pulled away cleanly such that the input to the ADN2812 goes from a valid data stream to an input that is absolutely transitionless, or at a noise level that is so small that it would not be perceived as transitions, essentially a few hundred μV, then the ADN2812 will not declare loss of lock and a new frequency acquisition will not be initiated. This is because when the ADN2812 is in lock to data mode the lock detector is looking for transitions on the input to compare to the VCO. If there are no transitions then the lock detector has nothing to compare to the VCO and therefore will not declare loss of lock and a new frequency acquisition will not be initiated. However, without a data input to keep the ADN2812's VCO phase and frequency locked, the VCO will begin to drift. When a new input data stream is applied to the inputs of the ADN2812, the acquisition time will depend on how far the VCO has drifted off while there was no input data. The lock detector will see the transitions of the new input data stream and it will determine how far off the frequency of the input data is from the VCO. If the difference is greater than 1,000 ppm, then the LOL will be asserted and a normal frequency and phase acquisition will take place with an acquisition time as specified in the data sheet, e.g., 1.3 ms for OC48. If the VCO frequency is less than 1,000 ppm from where it needs to be when the input data is reapplied, then all that is needed is a phase acquisition which can be done in hundreds of ns. LOL will not assert in this case. In either case, the dead bands do not apply to this situation.

PROGRAMMING A SHORTER DEAD BAND

The acquisition dead band can be reduced from 300 ms to ~30 ms by setting up the proper I²C® registers. First, a "1" must be written into Bit 7 of register CTRLC. Then, a "1" must be written into Bit 6 of address 0x0b. All zeros must be written into the rest of the bits of address 0x0b such that addr 0x0b = 0x40. A software reset of the ADN2812 will not overwrite these values. These values are only set to their defaults at power-up.

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