Supporting FDDI with the ADN2812
by Kevin Buckley

INTRODUCTION

The ADN2812 continuous-rate clock and data recovery device (CDR) can support all NRZ and NRZI random data patterns between 12.3 Mbps and 2.7 Gbps, and is protocol agnostic. The default operating mode of the ADN2812, lock to data mode, is for the CDR to lock on to any incoming data rate automatically, without the need of programming or external reference clocks. This requires that the incoming data is random NRZ or NRZI data. In lock to data mode, it is required that the bit pattern have transitions at the desired frequency (e.g., 0101), so that the frequency-locked loop can detect the correct frequency of the bit pattern.

If the data pattern does not meet this requirement, then it is possible to program the ADN2812 to lock to an external reference clock so that nonrandom bit patterns can be accommodated at the desired frequency. An example of a situation where the ADN2812 needs to be placed in lock to REFCLK mode is when an FDDI port is attempting to connect to another FDDI port.

FDDI CONNECTION PROTOCOL

Within every FDDI station there are SMT (station management) entities called PCM (physical connection management). The number of PCM entities within a station is exactly equal to the number of ports that the station has. This is because each PCM is responsible for one port.

The PCM entities are the part of SMT that controls the ports. In order to make a connection, two ports must be physically connected to each other by means of a fiber-optic or copper cable. When this happens, the PCMs that are responsible for those ports can recognize each other's existence and begin communicating. They do this by sending line states out of the port and onto the fiber. The PCM at the other end of the connection will recognize the line state and respond accordingly.

When the PCM sees another PCM on the other end of the connection, they will synchronize and communicate with each other. During this communication, a couple of important things happen:

1. The PCMs figure out the types of each port, and determine if they are compatible.

2. The PCMs perform an LCT (link confidence test).

REV. 0

The LCT determines if the quality of the link is good enough to establish a connection on. If it is not, the PCMs will not make a connection. If everything goes well during this signaling, the PCMs will establish a connection and place the ports on the token path that goes through that station. At this point, data (in the form of frames) can be sent through these ports and the ports become part of the network.

PCM entities have a number of internal states that they can be in. While in any state, the PCM has the port send out a certain line state. This line state will be received by the PCM on the other side of the connection. The other PCM entity (at the other end of the connection) will be able to tell which state the original PCM is in. PCMs use this information to signal data across the connection.

The connection attempt begins with the PCM state: break. The break state is the entry point in the start of a PCM connection. In the break state, a continuous stream of Q symbols (QLS; 00000) is transmitted to force the other end of the connection to break any existing connection and restart the connection initialization sequence. The break state is entered upon the start of a connection attempt, or if there was a problem with the previous connection attempt.

Once the PCM has begun to receive the correct symbols from the other side, the link will transition to the connect state. The connect state is used to synchronize the ends of the connection for the signaling sequence.

In the connect state, the PCM transmits a continuous stream of H symbols (HLS; 00100). The PCM stays in this state until it receives HLS from the other end of the connection. The reception of HLS indicates that the other PCM is also in the connect state. If the PCM is not attached to anything at all, then it will be receiving QLS and will remain here until it is connected to another PCM that sources HLS.

Once the connect state is successful, the link transitions to the next state. While in the next state, a continuous stream of I symbols is transmitted (ILS; 11111). The next state is used to separate the signaling performed in the signal state and it is where the LCT (link confidence test) is performed.

NRZI ENCODING

FDDI uses NRZI encoding. The ADN2812 inherently supports NRZI encoded data without the need of reference clocks or any external programming as long as the NRZI data is random. Due to the nonrandom nature of the FDDI connection protocol in addition to the NRZI encoding of the data, it is required that the ADN2812 be put into lock to REFCLK mode to support FDDI.

In order to understand why the ADN2812 needs to be used in lock to REFCLK mode to support this FDDI protocol, an explanation of NRZI encoded data is required. NRZI encoded data is a type of NRZ data that is encoded such that long strings of consecutive ones are broken up with transitions. This provides more transitions to CDR (clock data recovery) devices which make it easier for the CDR to lock and stay locked to incoming NRZ type patterns. A NRZI encoded data pattern will have a transition every time there is a 1 in the pattern and there will be no transition every time there is a 0. This is illustrated in the following diagrams which show patterns of consecutive Q, H, and I symbols in an FDDI link.
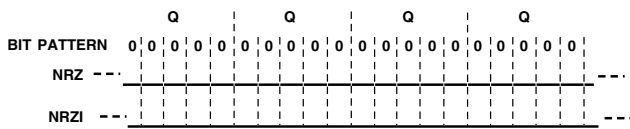

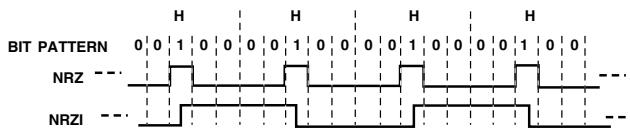*Figure 1. Consecutive "Q" Symbols During PCM State: Break*

Figure 2. Consecutive "H" Symbols During PCM State: Connect
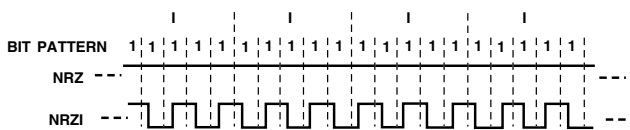

Figure 3. Consecutive "I" Symbols During PCM State: Next

ADN2812 DEFAULT MODE: LOCK TO DATA

The ADN2812 is a continuous rate clock and data recovery device that is designed to automatically lock on to any random NRZ or NRZI data pattern between 12.3 Mbps and 2.7 Gbps. The frequency-locked loop of the ADN2812 frequency locks the VCO to the incoming bit stream and then the delay and phase-locked loop aligns the phase of the VCO with the incoming bit stream. This is the default mode of operation of the ADN2812. There is no need for programming or any external reference clocks to operate in this mode.

The reason that this default mode cannot support the FDDI protocol is because, during the initial PCM states, the data that is presented to the ADN2812 is not random and it does not contain any transitions at the FDDI data rate of 125 Mbps. During the PCM states, the data that is presented to the ADN2812 is consecutive Q symbols followed by consecutive H symbols, followed by consecutive I symbols in that order. The period of time that each of these states lasts could be hundreds to thousands of milliseconds.

The first data presented to the ADN2812 is the Q symbols, which are all zeroes (Figure 1). Obviously, the ADN2812 will not lock to this when it's in lock to data mode since there are no transitions on the data. The subsequent data that the ADN2812 sees will be the consecutive H symbols. The H symbols, with NRZI encoding, look like a 25 Mbps NRZ data pattern of 10101010 … (Figure 2). Therefore, in lock to data mode, the ADN2812 will lock to 25 Mbps during the transmission of the consecutive H symbols. When the link transitions to the PCM state: next, consecutive I symbols are present at the input to the ADN2812. NRZI encoded, the I symbols will look like a true 125 Mbps bit pattern (Figure 3). The ADN2812's lock detector will sense that the frequency of the input data has changed from 25 Mbps to 125 Mbps and a new frequency acquisition will be initiated. At this point, the ADN2812 will lock to 125 Mbps. This temporary loss of synchronization by the ADN2812 is unacceptable. The result is that the FDDI link will never be able to achieve a valid connection.

SOLUTION: LOCK TO REFCLK MODE

A reference clock is not required to perform clock and data recovery on random NRZ and NRZI data patterns with the ADN2812. However, support for an optional reference clock is provided for situations where there is extended periods of time where the input data is nonrandom, repetitive, and does not have transitions at the desired frequency.

In lock to REFCLK mode, the ADN2812 uses an external reference clock as an acquisition aid. The VCO will be frequency locked with respect to an external reference clock and the lock detector will compare the VCO frequency against the reference clock frequency, not the input data. Using the ADN2812 in this mode will allow the part to lock to 125 Mbps when the consecutive H symbols are being received at the ADN2812 inputs even though there are no transitions at 125 Mbps present. When the PCM state transitions to the next state, the ADN2812 will already be locked at the correct frequency, 125 Mbps. When the input data switches from consecutive H symbols (PCM state: connect) to consecutive I symbols (PCM state: next) the ADN2812 will simply stay locked at 125 Mbps and there will not be a loss of synchronization.

The lock to REFCLK control bits are found in I^{2}C® Register CTRLA. The ADN2812 locks onto a frequency derived from the reference clock according to the following equation:

$$\text{Data Rate}/2^{\text{CTRLA[5:2]}} = \text{REFCLK}/2^{\text{CTRLA[7:6]}}$$

For example, suppose there is a 125 MHz system clock available in the FDDI system. To enable the ADN2812 to lock at 125 Mbps using this 125 MHz reference clock, the user needs to program the following bits:

CTRLA[7:6:] = [11]: sets F_{REF} range to 100 MHz–200 MHz
CTRLA[5:2] = [0011]: sets data rate/REFCLK ratio

After CTRLA[7:2] have been programmed, a 0 to 1 transition must be written into CTRLA[0] to enable the lock to REFLCLK mode. See the ADN2812 data sheet for a detailed description of lock to REFCLK mode as well as other programmable options.

CONCLUSION

It is important to note that the ADN2812 does not have to be programmed to use a reference clock in order to support random NRZI and NRZ data. The only reason this mode is required for FDDI is because of the very long periods of nonrandom data where there are no true 125 Mbps transitions occurring at the input to the device (e.g., 0101). For a continuous rate CDR that automatically locks to the input data without the need of programming or reference clocks, it is required that transitions be present at the desired frequency. For cases where a non-random, repetitive data pattern needs to be supported (e.g., FDDI connection states), there is an optional lock to REFCLK mode available.

AN05043–0–10/05(0)