ANALOG DEVICES

AN-657
APPLICATION NOTE

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ADN2812 Evaluation Board

INTRODUCTION

This application note describes the EVAL-ADN2812EBZ. The EVAL-ADN2812EBZ board design can easily convert into an EVAL-ADN28xxEBZ by replacing the on-board ADN2812 with one of the enhanced ADN28xx CDR derivatives of ADN2812: ADN2804, ADN2805, ADN2806, ADN2813, ADN2814, ADN2815, ADN2816, ADN2817, and ADN2818. Therefore, this application can also describe the use of the EVAL-ADN28xxEBZ evaluation board.

As an ADN2812 derivative, the ADN28xx supports either a fixed data rate or programmable data rate range of 10 Mbps to 2.7 Gbps. To simplify the description, this application note focuses on the ADN2812 as an on-board device under test (DUT), unless otherwise specified.

The ADN2812 is a continuous rate clock-recovery, data-retiming device based on a multiloop PLL architecture. The ADN2812 can automatically lock to any data rate from 10 Mbps to 2.7 Gbps, recover the clock, and retime the data without programming and without the need for an external reference clock as an acquisition aid. An I^2C interface is available to access special features of the ADN2812; however, it is not required for normal operation.

The EVAL-ADN2812EBZ is fabricated using standard FR-4 materials. All high speed differential signal traces are matched to within 3 mils length and maintain a 50 Ω characteristic impedance to preserve signal integrity.

QUICK START GUIDE FOR NORMAL OPERATING MODE (NO REFCLK AND NO I^2C PROGRAMMING REQUIRED)

1. Populate Jumpers P2 and P3. This disables the SLICEx adjust function by tying those pins to GND.
2. Populate Jumpers P4 and P6 to tie off the REFCLKx inputs. P4 connects REFCLKP to VCC and P6 connects REFCLKN to GND. Note that a reference clock is not required as an acquisition aid for the ADN2812. The device locks to any rate without the use of a reference clock.
3. It is unnecessary to make any connections to the I^2C interface of the ADN2812 for normal operation.
4. Apply a 3.3 V supply to the VCC (TP5) and GND (TP4) vector pins. No supply needs to be connected to I^2C_VCC (TP11) and GND (TP10) for the ADN2812 to operate. Those pins are used in case an external I^2C interface requires power to be supplied via the target (the ADN2812 evaluation board).
5. Connect PIN and NIN to a pattern generator that can supply a differential input to the ADN2812. It is important to use cables of matching length.
6. Connect CLKOUTP/CLKOUTN, DATAOUTP/DATAOUTN to measurement equipment using cables of matching length.
7. Apply a single-ended or differential NRZ data pattern to the inputs of the ADN2812. The frequency of the data pattern can be set to any data rate from 10 Mbps to 2.7 Gbps. An amplitude of >100 mV p-p is recommended for initial testing. The recovered clock and retimed data are present at the CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN outputs, respectively.

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5/10—Rev. 0 to Rev. A

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9/03—Revision 0: Initial Version

POWER SUPPLY

The ADN2812 evaluation board requires a single 3.3 V nominal supply for basic operation. This supply is brought on board through the VCC (TP5) and GND (TP4) vector pins.

PIN/NIN INPUTS

PIN/NIN inputs are brought onto the ADN2812 evaluation board through the J3 and J4 SMA connectors. Capacitors C3 and C4 provide ac coupling to the on-chip 50 Ω termination resistors. The capacitors used are 1.5 µF, X7R ceramic chip capacitors. It is recommended that the inputs to the ADN2812 are ac-coupled.

If dc coupling is required, C3 and C4 must be replaced with 0 Ω resistors. The common-mode level of the input signal must be greater than 2.3 V and the maximum input level cannot exceed 1 V p-p on either PIN or NIN.

CLOCK/DATA OUTPUTS

The CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN outputs are CML type outputs. CLKOUTP and CLKOUTN are brought out through 0.1 µF ac coupling capacitors to the J13 and J14 SMA connectors, respectively. DATAOUTP and DATAOUTN are brought out through 0.1 µF ac coupling capacitors to the J1 and J2 SMA connectors, respectively.

There are 100 Ω resistors to VCC placed at each of the outputs, R1 to R4. These are in parallel with on-chip 100 Ω resistors to VCC to provide a 50 Ω near-side termination for the CML outputs.

R10, R11, R16, and R17 are resistive terminations to GND that should not be populated for the CML output version of the ADN2812.

SLICEP/SLICEN

SLICEx allows the input quantizer decision level of the ADN2812 to be adjusted to accommodate amplified spontaneous emission (ASE) in long optical links that use fiber amplifiers. The slicing level can be adjusted by up to ±100 mV by applying a differential input voltage of up to ±1 V to SLICEP/SLICEN.

The SLICEP and SLICEN inputs are brought onto the ADN2812 evaluation board through the J6 and J5 SMA connectors, respectively. When not being used, the SLICEN/SLICEP inputs should be tied to GND using Jumpers P2 and P3.

LOOP FILTER CAPACITOR

The loop filter capacitor, CF, is connected between CF1 and CF2, Pin 14 and Pin 15. The CF capacitor needs to be a low leakage, 0.47 µF ceramic chip capacitor, >6.3 V, ±20%. The leakage of the capacitor needs to be <10 nA. If a leakage specification is not available for the capacitor, the leakage can be calculated using the insulation resistance specification. Assuming a maximum voltage of 3 V across the CF capacitor, the leakage is equal to

$$3 \text{ V}/I.R.$$

where *I.R.* is the insulation resistance of the capacitor.

The capacitor used on the ADN2812 evaluation board is a 0.47 µF ceramic chip capacitor, X7R dielectric, 1 GΩ insulation resistance.

LOSS OF SIGNAL DETECTOR

The ADN2812 has an on-chip loss of signal (LOS) detector. The LOS detector detects when the input level drops below a user programmable threshold and asserts an alarm on the LOS output pin. The threshold is set by connecting a resistor between the THRADJ pin and VEEx. The ADN2812 comes populated with a 10 kΩ THRADJ resistor, R6, which corresponds to a LOS threshold of ~5 mV p-p. If the input level drops below this threshold, the LOS pin is asserted to a Logic 1 by default. Writing a 1 to I^2C register bit CTRLC[2] configures the LOS pin to be active low.

There is an LED on the EVAL-ADN2812-EBZ that turns on when the LOS pin signals a loss of signal condition. This is only true if LOS is configured to be active high.

LOSS OF LOCK DETECTOR

The ADN2812 has a loss of lock (LOL) detector that signals when the ADN2812 has lost lock. Detailed descriptions of the various modes of operation of the LOL detector can be found in the ADN2812 data sheet. The LOL pin is asserted to a Logic 1 when a loss of lock condition has been detected. There is an LED on the EVAL-ADN2812EBZ that turns on when the LOL pin signals a loss of lock condition.

I^2C INTERFACE

The ADN2812 supports a 2-wire, I^2C compatible serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any device connected to the bus. There are two ways to interface to the I^2C. There is a 4-pin header that has the SCK, SDA, I^2C supply, and VEE. There is also a Molex 15-83-0064 receptacle available to the user. If the I^2C controller interfacing with the ADN2812 requires that the EVAL-ADN2812-EBZ supply the power, then a power supply can be attached to TP11.

The SCK and SDA pins are open-collector outputs that are pulled up to 3.3 V on the EVAL-ADN2812EBZ with 1.8 kΩ resistors, R9 and R22. The SDA and SCK pins should not be connected to an I^2C controller that has pull-ups to 5 V. This may damage the device.

The slave address of the ADN2812 is a 7-bit word where the MSB, SADDR6 is factory programmed to 1; SADDR5 can be set to 1 or 0 by the SADDR5 jumper on the evaluation board. SADDR[4:0] are all set to 0 on chip.

Detailed descriptions of the I^2C programmability and functionality can be found in the ADN2812 data sheet.

REFERENCE CLOCK (OPTIONAL)

There are two optional uses for a reference clock on the ADN2812. The reference clock can be used to read back the acquired data rate to within 100 ppm, and there is a lock-to-reference mode where the ADN2812 is programmed to lock to a specific data rate using the reference clock as an acquisition aid. For a detailed description of the reference clock modes, refer to the ADN2812 data sheet.

The reference clock is brought onto the EVAL-ADN2812EBZ on J9, REFCLKP, and J8, REFCLKN. The ADN2812 reference clock input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended low voltage TTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical and 100 ppm accuracy is sufficient. Reference clock frequencies from 10 MHz to 160 MHz are supported.

When the reference clock is not being used, REFCLKP should be tied to VCC with P4 and REFCLKN can be left floating or tied to GND with Jumper P6. If a high speed reference clock is used, a 100 Ω differential characteristic impedance should be maintained. R5 should then be populated with a 100 Ω, 0603 chip resistor. The REFCLK PCB traces are 50 Ω transmission lines.

TEST POINTS

Test points are supplied on a 10-pin, 5 × 2 header, as shown in Figure 1.

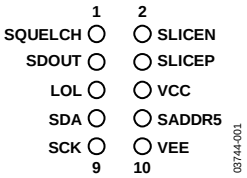

Figure 1.

CHOOSING AC COUPLING CAPACITORS

The choice of ac coupling capacitors at the input (PIN, NIN) and output (DATAOUTP, DATAOUTN) of the ADN2812 must be chosen such that the device works properly over the full range of data rates used in the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander, causing pattern dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection may require some trade-offs between droop and PDJ.

Assuming that 2% droop can be tolerated, the maximum differential droop will be 4%. Normalizing to peak-to-peak voltage:

$$Droop = \Delta V = 0.04\ V = 0.5\ V\ p\text{-}p\ (1 - e^{t/-\tau})$$

where:
τ is the RC time constant (C is the ac coupling cap, R = 100 Ω seen by C).
t is the total discharge time, nT.
n is the number of CIDs.
T is the bit period.

Therefore, $\tau = 12t$.

The capacitor value can then be calculated by combining the equations for τ and t:

$$C = 12nT/R$$

When the capacitor value is selected, the PDJ can be approximated as

$$PDJ_{pspp} = 0.5t_r(t - 3^{(-nT/RC)})/0.6$$

where:
PDJ_{pspp} is the amount of pattern dependent jitter allowed, < 0.01 UI p-p typical.
t_r is the rise time, 0.22/BW, where BW ~ 0.7(*Bit Rate*).

This expression for t_r is accurate only for the inputs; the output rise time for the ADN2812 is ~100 ps regardless of data rate.

The EVAL-ADN2812EBZ comes populated with 1.5 µF ac coupling capacitors on the inputs and 0.1 µF ac coupling capacitors on the outputs. For lower data rates, for example, in the tens of megahertz (MHz), and/or very high numbers of consecutive identical digits, these values may not be optimum.

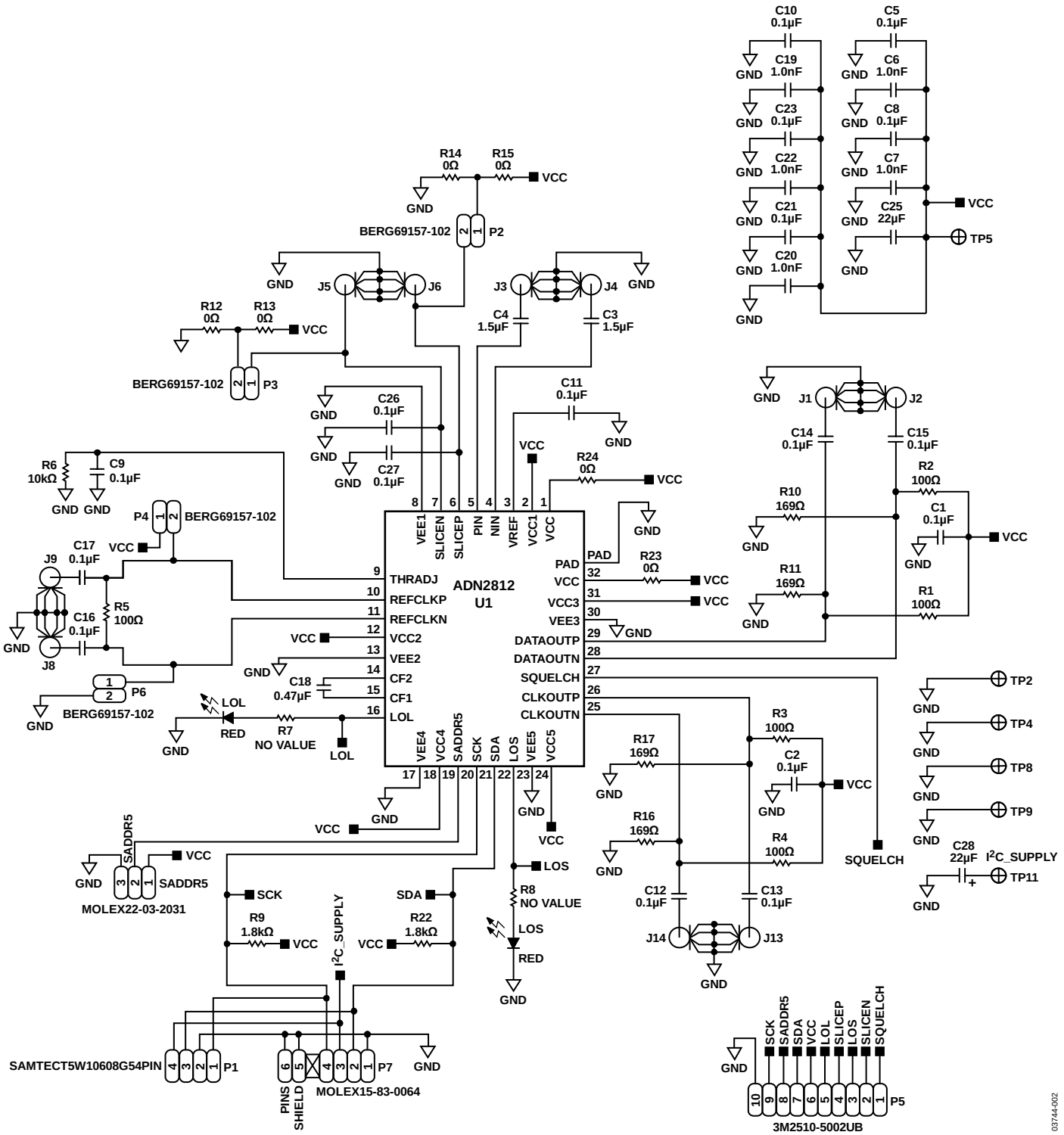

Figure 2. EVAL-ADN2812EBZ

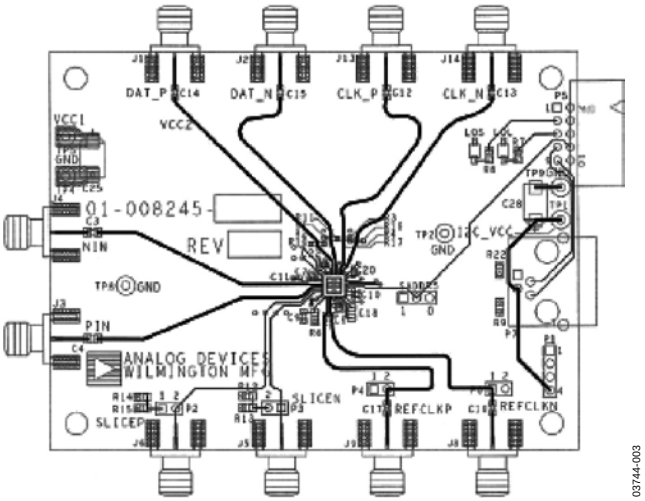

Figure 3. Primary Layer

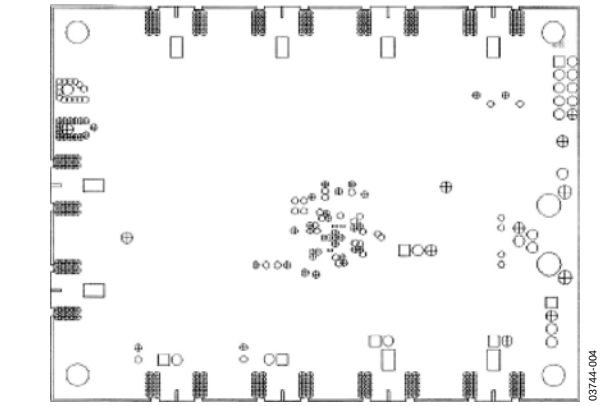

Figure 4. VEE Plane

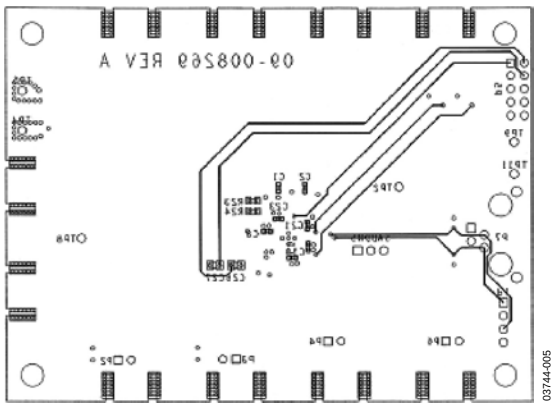

Figure 5. Secondary Layer

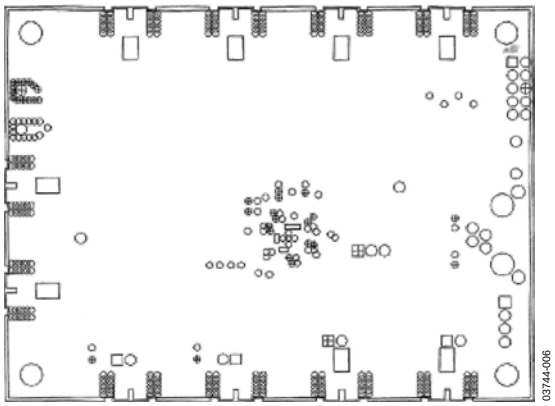

Figure 6. VEE Plane

Table 1. Component List

Qty	Reference Designator	Description	Manufacturer	Part Number
8	C1, C2, C5, C8, C10, C11, C21, C23	0.1 µF, 16 V, ceramic Y5V 0402	Yageo American	04022f104Z7B20D
2	C3, C4	1.5 µF, 6.3 V, ±10% ceramic X5R 0805	Panasonic	ECJ-2YBOJ155K
5	C6, C7, C19, C20, C22	1.0 nF, 25 V, ±10% ceramic X7R 0402	Panasonic	ECJ-0EB1E102K
7	C9, C12 to C17	0.1 µF, 16 V, ceramic X7R 0603	Panasonic	ECJ-1VB1C104
1	C18	0.47 µF, 16 V, ±10% ceramic X7R 0805	Panasonic	ECJ-2YB1C474K
2	C25, C28	22 µF, 16 V, ±20% Tantalum D case	Panasonic	ECS-H1CD226R
2	C26, C27	0.1 µF, 25 V, ceramic 0805	Panasonic	ECJ-2VB1E104K
10	J1 to J6, J8, J9, J13, J14	0.1 µF SMA PC mount end launch	Johnson	142-0701-851
1	P7	0.1 µF receptacle	Molex	15-83-0064
2	LOL, LOS	LED red clear LC gull wing SMD	Chicago Mini Lamp	CMD28-21SRC/TR8/T1
5	R1 to R5	100 Ω, 1/10 W, 0402 chip resistor	Panasonic	ERJ-2RKF1000X
1	R6	10 kΩ, 1/4 W, 0805 chip resistor	Panasonic	ERJ-P06J103V
2	R7, R8	Value is LED dependent	Panasonic	LED dependent
2	R9, R22	1.8 kΩ, 1/10 W, 0805 chip resistor	Panasonic	ERA-S33J182V
2	R12, R14	0 kΩ, 1/10 W, 0805 chip resistor	Panasonic	ERJ-6GEY0R00V
2	R23, R24	0 kΩ, 1/16 W, 0603 chip resistor	Panasonic	ERJ-3GEY0R00V
1	P1	Jumper, male, straight 4-position	Sullins Connector Solutions	S1222-04-ND
4	P2 to P4, P6	Jumper, male, straight 2-position	Sullins Connector Solutions	S1222-02-ND
1	P5	10-position (2 × 5) connector header	Molex	WM6810-ND
1	SADDR5	3-position header	Molex	22-03-2031

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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