ANALOG DEVICES

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APPLICATION NOTE

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ADN2891 Evaluation Board

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INTRODUCTION

This application note describes the ADN2891 evaluation board. The ADN2891 limiting amplifier works as a data quantizer for SONET, Gigabit Ethernet (GbE), and Fibre Channel optical receivers. Supporting a signal data rate from a minimum of 155 Mbps up to a maximum of 3.2 Gbps. The ADN2891 has a better than 4mV p-p typical input sensitivity and works well with input level up to 2 V p-p. The ADN2891 also provides loss of signal (LOS) and received signal strength indicator (RSSI) features. This makes the ADN2891 an ideal limiting amplifier for all SFF-8472-compliant SFP transceivers.

The ADN2891 evaluation board uses standard FR-4 material. Both the input/output differential transmission line pairs use 50 Ω characteristic impedance. Each pair keeps the line length from SMA connector to a respective signal pad within a 3 mils difference to preserve signal integrity.

The evaluation board uses 3.3 V power supply.

Table I. Switch Functions

Switches	Functions	Default Setting	Options
S1	PD_Cath	AVDD	NC
S2	RSSI	10 kΩ + 0.0 μF	NC
S3	SQUELCH	GND	AVCC
S4	THRADJ	100 kΩ	1 kΩ

Quick Start Guide

Please refer to Figure 1 for each of the following steps:

1. Set the switch from S1 to S4 to the factory default setting shown in Figure 1 where the Switch S3 disables the squelch function by connecting to ground. S1 and S2 set the RSSI function, and S4 sets the LOS threshold resistor (default setting is 100 kΩ).
2. Apply a 3.3 V power to test points VCC (red) and GND (black). The test points are located on the right-hand side of the evaluation board.
3. Connect PIN and NIN (two SMA connectors located at the bottom of the board) to a PRBS pattern generator. It is important to use a pair of matched length, 50 Ω cables.

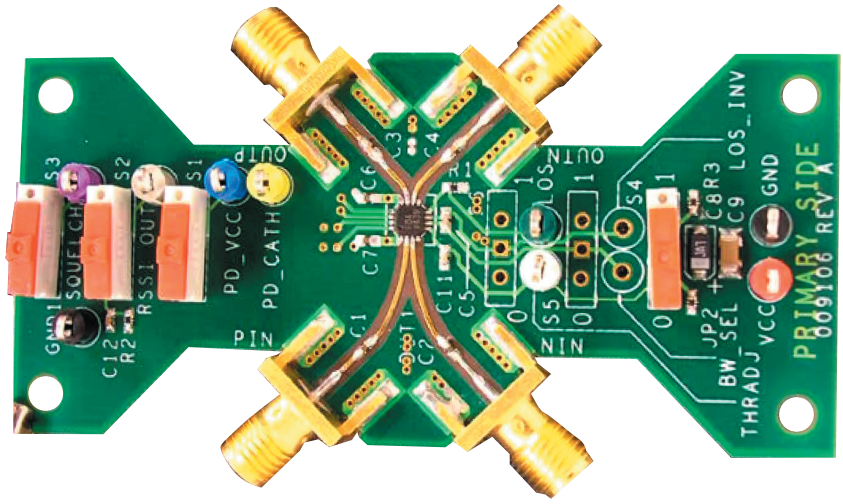

Figure 1. The Switch Factory Default Settings of the ADN2891 Evaluation Board

4. Connect OUTP and OUTN (two SMA connectors located at the top of the board) to an oscilloscope using a pair of matched length, 50 Ω cables.
5. Apply a PRBS data pattern signal (any data rate from 155 Mbps to 3.2 Gbps) to the ADN2891. A signal with amplitude >100 mV p-p is a good signal for an initial test. The ADN2891 will present its output at the OUTP and OUTN SMA connectors.

ADN2891 EVALUATION BOARD OUTLINES

Power Supply

The ADN2891 evaluation board requires a 3.3 V, ±10% nominal power supply. This supply should be brought to the board through the test points VCC (red) and GND (black).

PIN/NIN Inputs

The ADN2891 gets a differential or single-ended signal through the SMA connectors PIN and NIN. When applying a single-ended signal, one of the differential input SMA connectors should be terminated with a 50 Ω terminator.

With an ac signal coupling, ADN2891 supports not only CML but also LVDS, LVPECL, and LVCMOS. Ceramic capacitor C1 and C2 provide the ac-coupling path to the signal input. To match with the 50 Ω transmission line, the ADN2891 has on-chip, 50 Ω termination resistors for its input pins.

Data Outputs

The OUTP and OUTN outputs are CML outputs. Through 0.1 μF ceramic capacitors, the CML output signal is ac-coupled to the SMA connector OUTP and OUTN. The ADN2891 has on-chip 50 Ω termination resistors connected to its CML output pins.

Auto-Zeroing Capacitor

The ADN2891 has an on-chip offset cancellation circuit which requires an external 0.01 μF capacitor connected between Pins CAZ1 and CAZ2. To operate this offset cancellation circuit properly, the ADN2891 inputs should be ac-coupled.

Loss of Signal Detector (LOS)

The ADN2891 has an on-chip loss of signal (LOS) detector. The LOS asserts when the input level drops below a user-programmed threshold voltage. The threshold is set by selecting a resistor value between the THRADJ pin and GND. On the ADN2891 evaluation board, the Switch S4 can select resistors between a 100 kΩ (factory default setting position) or a 1 kΩ (switched to uppermost position). If an input signal level drops below the preset threshold, the LOS output will be Logic 1. LOS test point (green) connects to the LOS output pin.

Received Signal Strength Indicator (RSSI)

ADN2891 has an RSSI circuit to indicate a received optical average power. Biased a photodiode, the ADN2891 RSSI circuit senses the current supplied to the photodiode, outputs a current proportional to the average amount of the photodiode current with a 1:1 ratio. A resistor placed between the RSSI_OUT to GND converts the output current to a voltage referenced to GND. This on-chip circuit eliminates the need of an external RSSI circuitry to get a SFF-8472-compliant optical receiver.

To evaluate the ADN2891 RSSI circuit, Switch S1 must be at the factory default setting position. This setting provides power supply to the ADN2891 PD_VCC pin and the on-chip RSSI circuitry.

The PD_Cathode pin connects to a PD cathode and provides a current supply. The yellow test point on the evaluation board provides the bias voltage to the PD. The current provided from the PD_Cathode pin is mirrored to the RSSI_OUT pin.

Set S2 to the factory default setting position. The voltage is available at the RSSI_OUT test point. In this configuration, the RSSI_Output current is converted to a voltage via a 10 kΩ resistor.

When Switch S2 sets at the upper position, the output current is available at the RSSI_OUT test point (gray).

Squelch Mode

Driving the squelch input pad to logic high will disable the limiting amplifier outputs. So, for normal evaluation operation, Switch S3 should be at the factory default setting position (Logic 0). Otherwise, set it to the upper position (Logic 1) to disable the ADN2891 outputs.

Output Eye Measurements

Figure 2 shows an ADN2891 differential output with a jitter-free, 10 mV p-p differential, 3.2 Gbps, 2^{23}-1 PRBS pattern input signal.

Figure 3 shows an ADN2891 differential output with a jitter-free, 10 mV p-p differential, 2.488 Gbps, 2^{23}-1 PRBS pattern input signal.

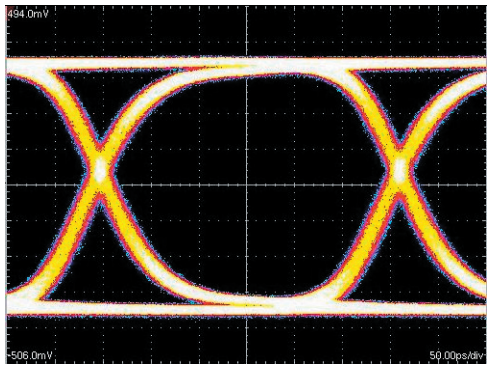

Figure 2. ADN2891 Output with 10 mV p-p, 3.2 Gbps Differential Input

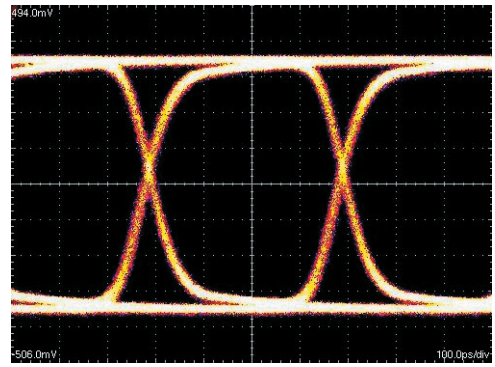

Figure 3. ADN2891 Output with 10 mV p-p, OC48 Differential Input

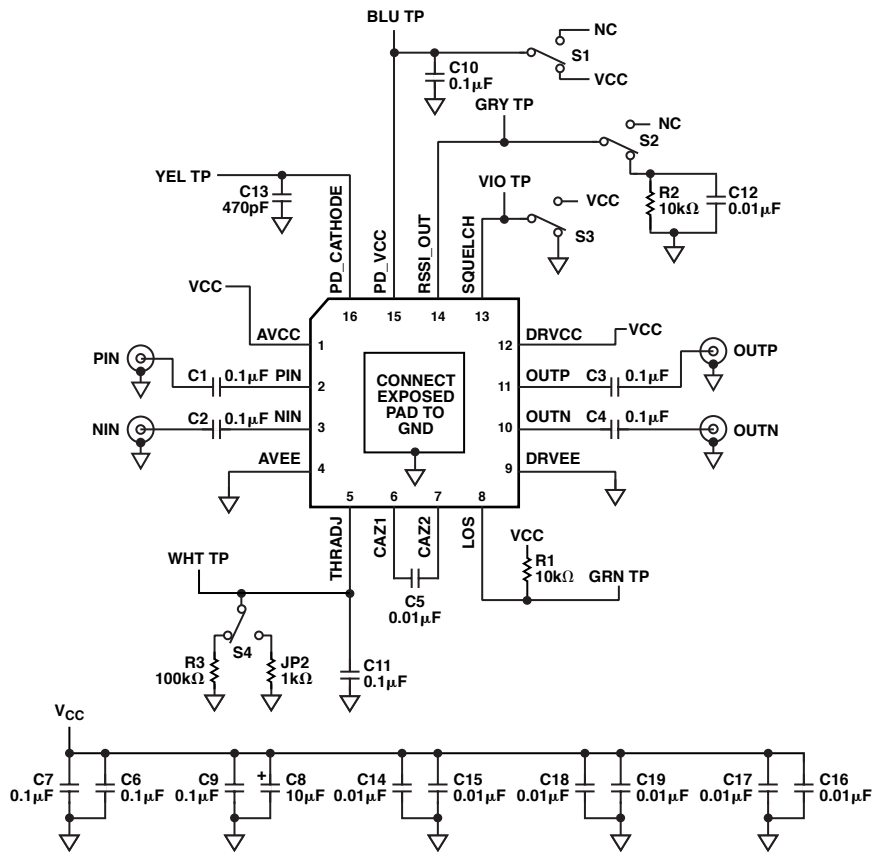

Figure 4. ADN2891 Evaluation Board Schematic

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