ANALOG DEVICES

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APPLICATION NOTE

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Using the ADN2892 Evaluation Board

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INTRODUCTION

This application note describes the ADN2892 evaluation board. The ADN2892 is a limiting amplifier optimized to support SONET, Gigabit Ethernet (GbE), and Fibre Channel applications. Supporting multiple data rate applications that range from a minimum of 155 Mbps up to a maximum of 4.25 Gbps, the ADN2892 offers better than 5 mV p-p typical input sensitivity and supports input levels of up to 2 V p-p.

The ADN2892 also provides loss of signal (LOS) and received signal strength indicator (RSSI) features. This makes the ADN2892 an ideal limiting amplifier for all SFF-8472-compliant SFP transceiver products. In addition, the ADN2892 features an on-chip selectable filter (cutoff frequency is at 1.5 GHz) to filter out the relaxation oscillation emanating from of inexpensive CD lasers used in legacy 1 Gbps fiber channel transmitters. The reduced bandwidth improves the optical Rx sensitivity at lower data rates, such as 1×FC.

The ADN2892 evaluation board uses standard FR-4 material. Input/output differential transmission line pairs use 50 Ω characteristic impedance. Each pair keeps the line length equal from the SMA connector to the respective signal pad within a tolerance of 3 mils to preserve signal integrity. The evaluation board uses a 3.3 V power supply.

To get started using this evaluation board, use the Quick Start section while referring to Table 1 and Figure 1.

Table 1. Switch Settings

Switch	Function	Default	Options
S1	PD_CATHODE	AVCC	NC
S2	RSSI_OUT	10 kΩ + 0.0 µF	NC
S3	SQUELCH	GND	VCC
S4	THRADJ	100 kΩ	1 kΩ
S5	BW_SEL	GND	VCC
S6	LOS_INV	GND	VCC

DIGITAL PICTURE OF ADN2892 EVALUATION BOARD

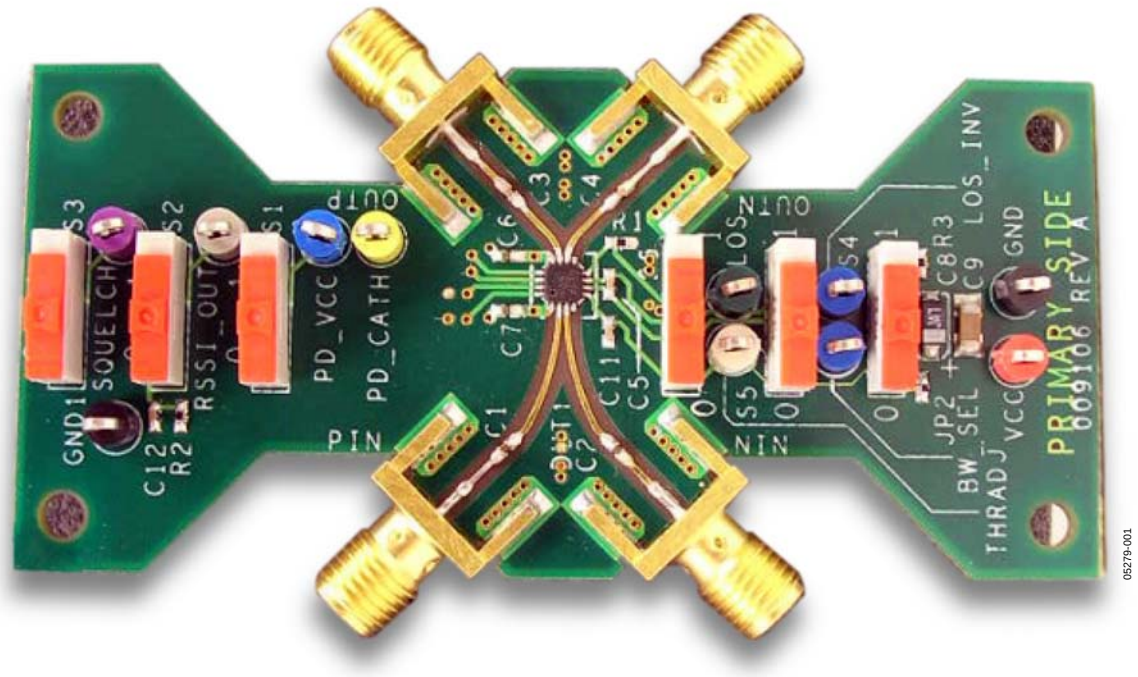

Figure 1. Factory Default Switch Settings of the ADN2892 Evaluation Board

QUICK START

Getting started with the ADN2892 evaluation board is a five step process. Refer to Figure 1 when completing these steps.

1. Set Switch S1 through Switch S6 to the factory default settings. Note that Switch S1 and Switch S2 are set for the RSSI function and Switch S4 sets the optional LOS threshold resistor (the default setting is 100 kΩ). Switch S3 disables the squelch function by connecting to ground. Switches S5 and S6 are set to ground to disable the BW_SEL and LOS_INV functions.
2. Apply 3.3 V of power to test points VCC (red) and GND (black). The test points are located at the right-most side of the board.
3. Using a pair of matched-length 50 Ω cables, connect PIN and NIN (two SMA connectors located at the bottom of the board) to a pattern generator to get a PRBS signal.
4. Using a pair of matched-length 50 Ω cables, connect OUTP and OUTN (two SMA connectors located at the top of the board) to an oscilloscope.
5. Apply a PRBS data pattern signal at a data rate ranging from 155 Mbps to 4.25 Gbps to the ADN2892. A differential signal with amplitude of greater than100 mV p-p is a good signal for an initial test. The ADN2892 presents its output at the OUTP and OUTN SMA connectors.

ADN2892 EVALUATION BOARD FEATURES

Power Supply

The ADN2892 evaluation board requires a 3.3 V, ±10% nominal power supply. Connect this supply to the board through the VCC (red) and GND (black) test points.

PIN/NIN Inputs

The ADN2892 receives a differential or single-ended signal through the SMA connectors, PIN and NIN. When applying a single-ended signal, terminate one of the differential input SMA connectors with a 50 Ω terminator.

With ac signal coupling, the ADN2892 supports not only CML, but also LVDS, LVPECL, and LVCMOS. Ceramic Capacitor C1 and Capacitor C2 provide the DC blocking to the signal input. To match the 50 Ω transmission line, the ADN2892 features on-chip, 50 Ω single-ended termination resistors for its input pads.

Data Outputs

The OUTP and OUTN outputs are CML outputs. Through 0.1 µF ceramic capacitors, the CML output signal is ac coupled to the SMA connectors, OUTP and OUTN.

Loss of Signal Detector

The ADN2892 features an on-chip LOS detector. The LOS signal asserts when the input signal level drops below a user-programmed threshold voltage. The threshold is set by selecting a resistor value between the THRADJ pin and GND. On the ADN2892 evaluation board, Switch S4 can select resistors between a 100 kΩ (the factory default setting position) or a 1 kΩ (when switched to upper-most position). If an input signal level drops below the preset threshold, the LOS output is set to Logic 1. The LOS test point (green) connects to the LOS output pad.

RSSI

The ADN2892 has an on-chip RSSI circuit to indicate a received optical average power. Biased on a photodiode, (refer to the functional block diagram in the ADN2892 data sheet), the ADN2892 RSSI circuit senses the current supplied to the photodiode and outputs a current proportional to the average amount of the photodiode current with a ratio of 1:1. A resistor placed from RSSI_OUT to GND converts the output current to a voltage referenced to GND. This on-chip circuit eliminates the need for external RSSI circuitry to get an SFF-8472-compliant optical receiver.

To evaluate the ADN2892 RSSI circuit, Switch S1 must be at the factory default setting position shown in Figure 1. This setting provides the power supply to the ADN2892 PD_VCC pin and to the on-chip RSSI circuitry.

The PD_CATHODE pin connects to a PD cathode and provides a bias current supply. The yellow test point on the evaluation board provides the bias voltage to the photodiode. The current provided from the PD_CATHODE pin is mirrored to the RSSI_OUT pin.

Set Switch S2 to the factory default setting position shown in Figure 1, the voltage is available at the RSSI_OUT test point. In this configuration, the RSSI_OUT current is converted to a voltage via a 10 kΩ resistor.

When Switch S2 is set to the upper position, the output current is available at the RSSI_OUT test point (gray).

Squelch Mode

Driving the squelch input pad to Logic 1 disables the limiting amplifier outputs. Therefore, for normal operation, set Switch S3 to the factory default setting position (Logic 0) as shown in Figure 1. Otherwise, set Switch S3 to the upper position (Logic 1) to disable the ADN2892 outputs.

BW_SEL Mode

Driving the BW_SEL input to Logic 0 enables the internal 1.5 GHz low-pass filter. Set Switch 5 to the factory default setting position (Logic 0) to enable the on-chip low-pass filter. Otherwise, set Switch S5 to the upper position (Logic 1) for full bandwidth (3.8 GHz) operation.

LOS_INV Mode

LOS_INV is an input pin with a 100 kΩ on-chip pull-down resistor. Set Switch S6 to the factory default setting position (Logic 0) for normal LOS operation. Otherwise, set Switch S6 to the upper position (Logic 1) to enable the LOS_INV mode. The function matrix of LOS_INV input and LOS output is shown in Table 2.

Table 2. LOS_INV Input and Output

LOS_INV Level	LOS Level	Function
Low	High	Loss of Input Signal
	Low	Input Signal Exists
High	High	Input Signal Exists
	Low	Loss of Input Signal

Output Eye Measurements

Figure 2 shows the ADN2892 differential output with a jitter-free, 10 mV p-p differential, 4.25 Gbps, $2^{23} - 1$ PRBS pattern input signal.

Figure 3 shows the ADN2892 differential output with a jitter-free, 2 V p-p differential, 2.488 Gb/s, $2^{23} - 1$ PRBS pattern input signal.

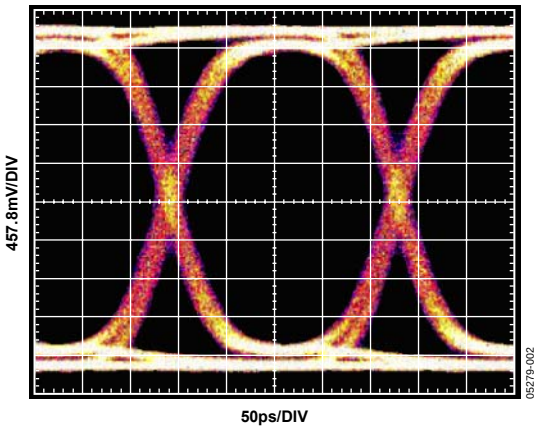

Figure 2. ADN2892 Output with 10 mV p-p Differential Input

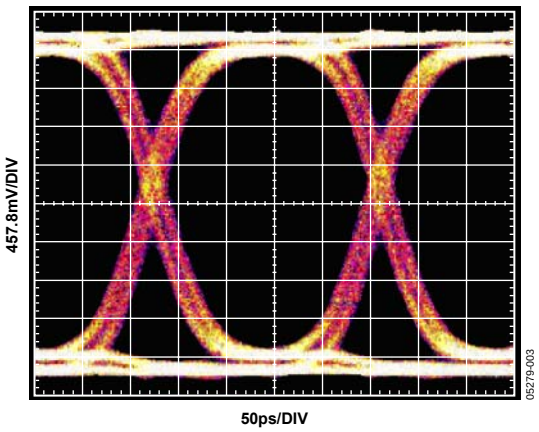

Figure 3. ADN2892 Output with 2 V p-p Differential Input

ADN2892 EVALUATION BOARD SCHEMATIC

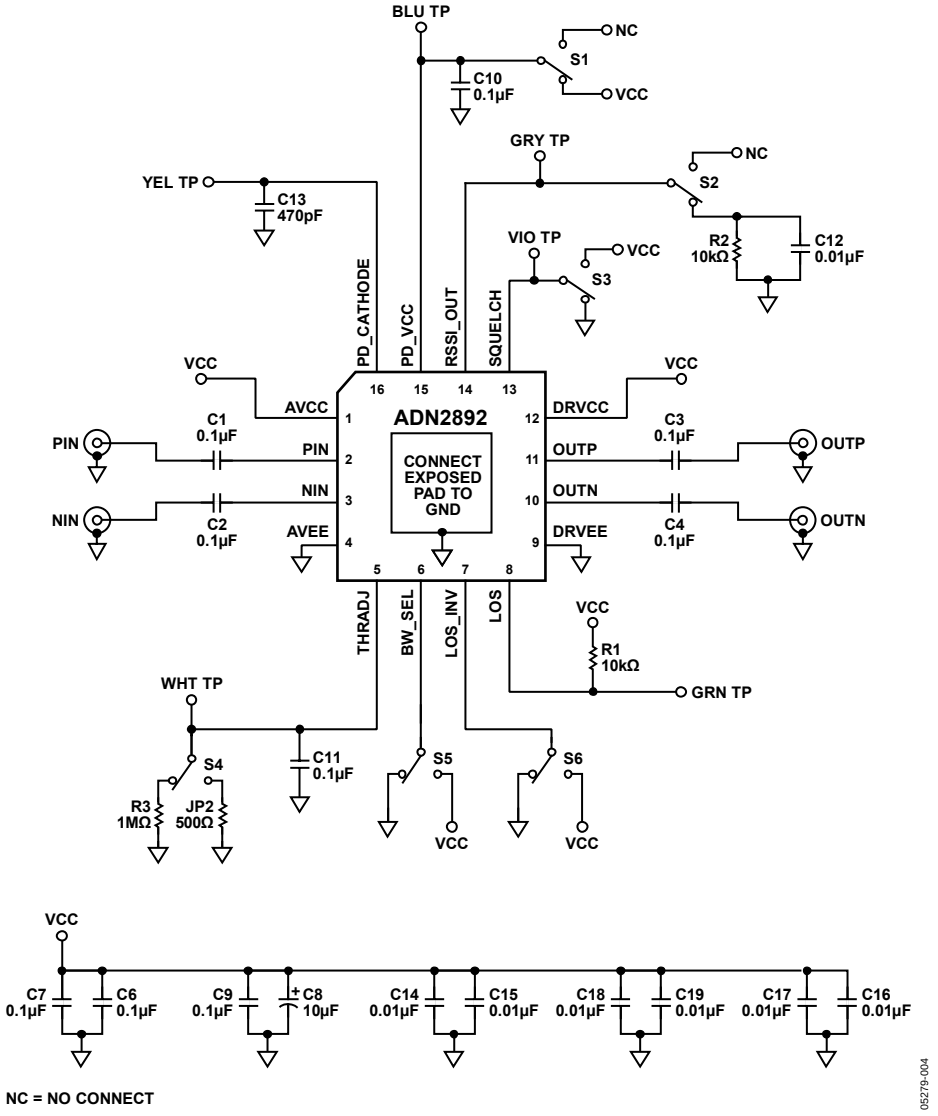

Figure 4. ADN2892 Evaluation Board Schematic

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