ADP1043A Evaluation Software Reference Guide

Preliminary Technical Data

EVAL-ADP1043A-GUI-RG

GENERAL DESCRIPTION

This user guide gives describes the various controls and indicators of the ADP1043A Evaluation Software. It gives the details of what each button on the GUI does, in terms of the register that is being updated, along with a brief description.

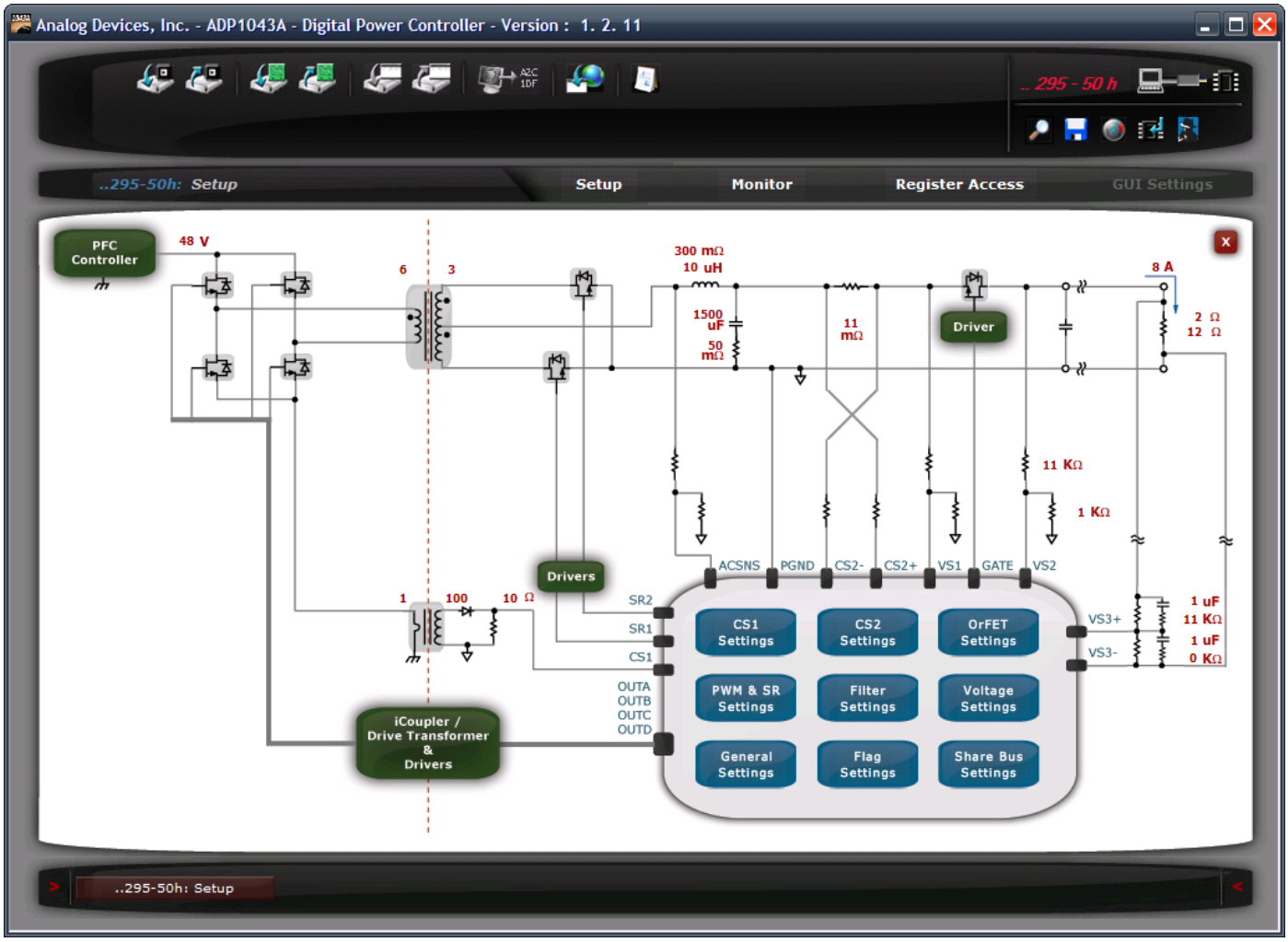

Figure 1. GUI Main Interface Window

Rev. A

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REVISION HISTORY

06/09—Rev. 1

09/09—Rev. 2

GUI CONTROLS

LINK

Figure 2.

Table 1. Referring to Figure 2

No.	Name	REG	Bits	R/W	Description
1	"USB to I2C interface" Number				This number shows the last three digits of the "USB to I2C interface" connected to ADP1043A. This number is also physically printed on the "USB to I2C Interface"
2	ADP1043A Address				This number shows the address of ADP1043A the GUI is connected to.
3	Communication link				This animated indicator shows if the GUI is communicating with ADP1043A
4	Scan				The GUI scans for all the ADP1043A connected to the computer. This helps in connecting and disconnecting devices once the GUI is already running.
5	Save/Load Options				This control opens the Tools window
6	Dashboard				This control opens the Dashboard window
7	Update EEPROM	0x5E 0x7B	[7:0]	W	This control writes the contents of the registers to the EEPROM of ADP1043A This is done by writing 0h twitce to register 0x5E, followed by writing 0h to 0x7B, wait for 40ms and followed by writing 1h to 0x5E
8	Spy				This control opens the Spy window

STRUCTURAL NAVIGATION

Figure 3.

Table 2. Referring to Figure 3

No.	Name	REG	Bits	R/W	Description
1	Device – Window Info				This indicator shows the device address and the window name of the window which is currently open
2	Structural Navigation				If you have only one device connected to the GUI, then clicking on the buttons opens the respective windows. If you have multiple devices connected, then clicking on the buttons opens the window for the device selected in the "Link" section shown above in Figure 2

WINDOWS NAVIGATION

Figure 4.

Table 3. Referring to Figure 4

No.	Name	REG	Bits	R/W	Description
1	Arrows				The arrows move the tabs in the respective directions
2	Tabs				The tabs open the window whose name and device address is displayed on it

TOOLS

Figure 5.

Table 4. Referring to Figure 5

No.	Name	REG	Bits	R/W	Description
1	Save Register Settings				This control saves the contents of the register map of the device selected in the "Link" section shown above in Figure 2, to a ".43r" file
2	Load register Settings				This control loads the contents of the register map to the device selected in the "Link" section shown above in Figure 2, from a ".43r" file
3	Save Board Settings				This control saves the information about the extrenal components required by the GUI to a ".43b" file
4	Load Board Settings				This control loads the information about the extrenal components required by the GUI from a ".43b" file
5	Update GUI				This control connects to" www.analog.com" and redirects you to the page which has the latest version of the GUI
6	Reference Guide				This control opens the GUI Reference Guide

DASHBOARD

Figure 6.

Table 5. Referring to Figure 6.

No.	Name	REG	Bits	R/W	Description
1	PS ON	0x2C	[5]	W	This control turns ON or OFF the PSON control signal when Software PSON is selected.
2	VS1	0x15	[15:4]	R	This value displays the voltage measured at the VS1 pin and scaled using the R1 and R2 values entered by the user.
3	VS3	0x17	[15:4]	R	This value displays the voltage measured at the VS3 pin and scaled using the R1 and R2 values entered by the user.
4	CS2	0x18	[15:4]	R	This value displays the output current. The CS2 ADC gives a value corresponding to the voltage drop across the CS2 pins, using the Rsense resistance value, the software calculates the output current and is scaled using the CS2 Nominal Voltage Setting
5	Power Supply	0x00	[7]	R	Red = Power supply is off. All PWM outputs are disabled. This bit stays high until a PS ON is performed.
6	Sync Rectifiers	0x00	[3]	R	Red = Sync rects are disabled. This flag is enabled when any of these three cases is true: • SR1 and SR2 are disabled by the user. • The load current has fallen below the threshold in Register 0x3C. • A flag that was configured to disable the sync rects has been set.
7	OrFET	0x00	[6]	R	Red = OrFET control signal at the GATE pin (Pin 16) is off.

SETUP

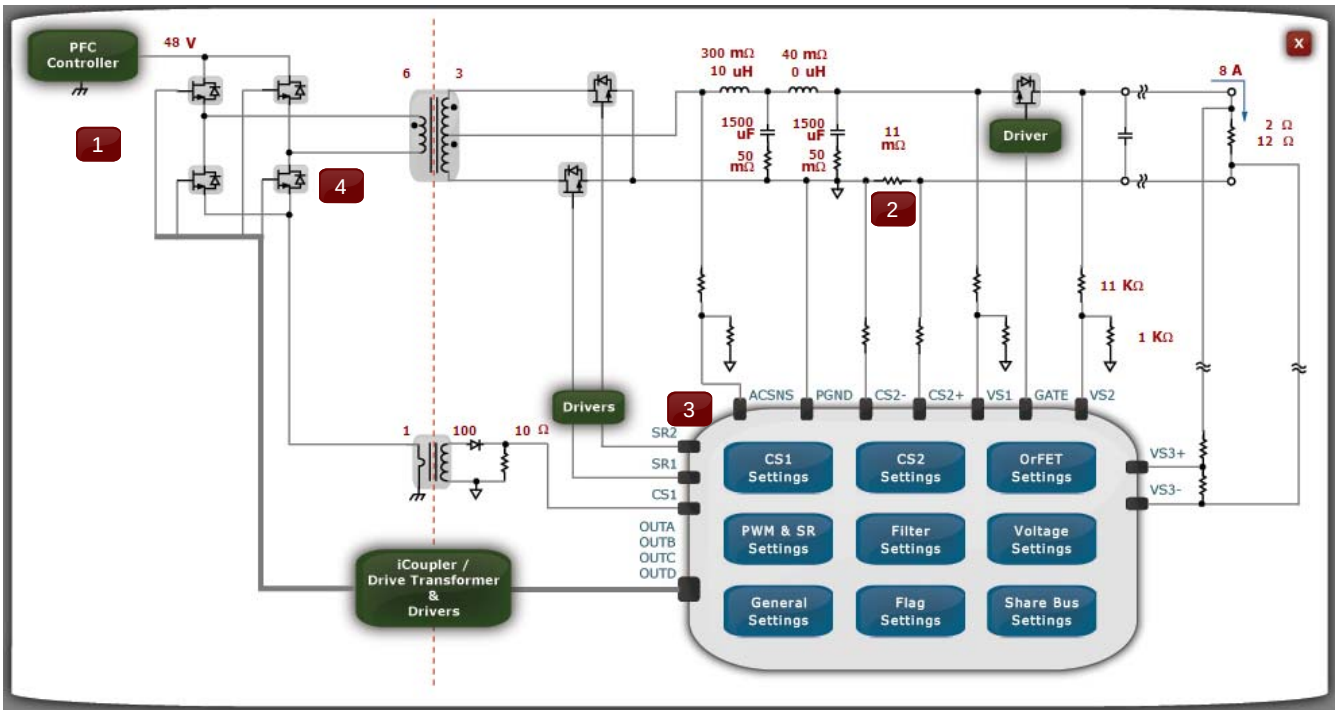

Figure 7.

Table 6. Referring to Figure 7

No.	Name	REG	Bits	R/W	Description
1	External Components				These external components values are entered by the user, which helps the GUI in calculating scale factors, full loop phase and gain response of the system. The user can also select various other options like topology for display purposes
2	High-Side Current Sensing	0x24	[7]	W	The user can select between High-Side or Low-Side Current Sensing by clicking on this control
3	ADP1043A Setup Blocks				The grey block represents ADP1043A and the blue blocks represent the various setup blocks of the ADP1043A. These blue blocks can be clicked to open the corresponding window for settings
4	Resonant Mode	0x40	[7:0]	W	The user can select between Resonant Mode or other topologies by clicking on this control

VOLTAGE SETTINGS

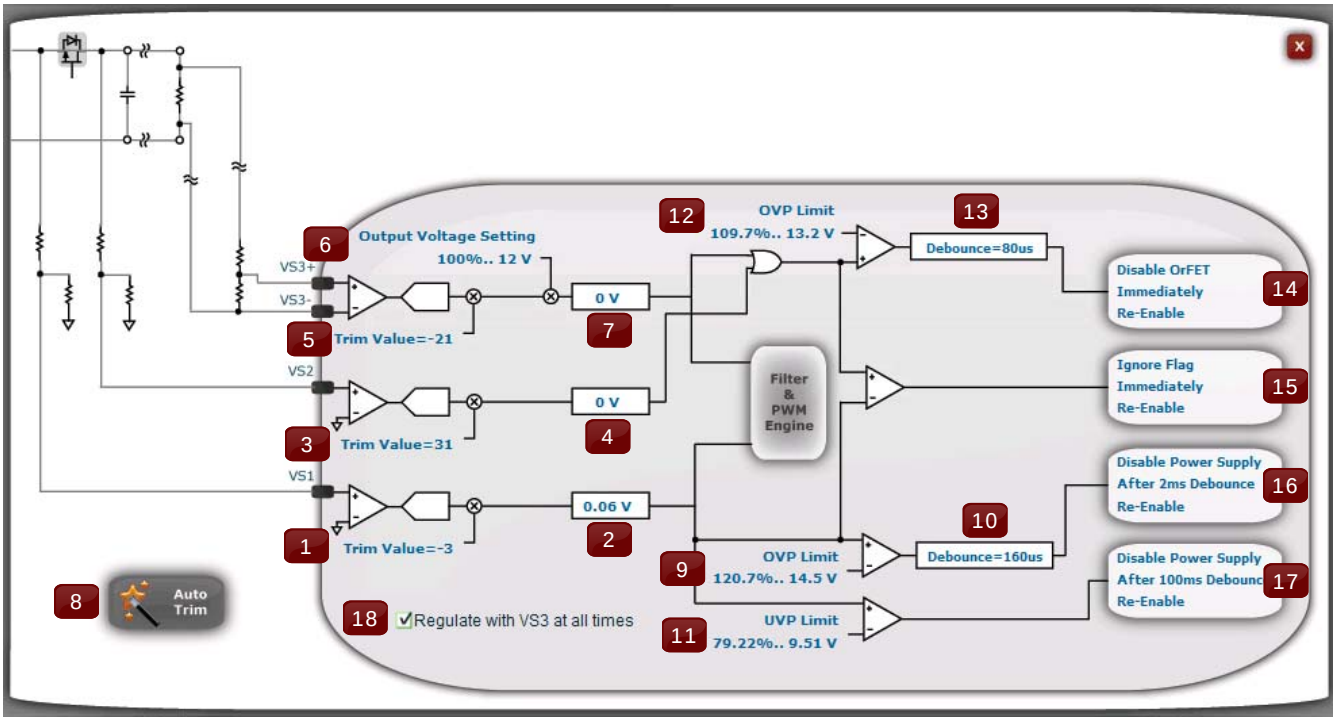

Figure 8.

Table 7. Referring to Figure 8.

No.	Name	REG	Bits	R/W	Description
1	VS1 Trim Value	0x38	[7:0]	W	This sets the amount of gain trim that is applied to the VS1 ADC reading. This control trims the voltage at the VS1 pin for external resistor tolerances. This control is trimmed until the VS1 Value indicator 2 displays the desired nominal voltage
2	VS1 Value	0x15	[15:4]	R	This value displays the voltage measured at the VS1 pin and scaled using the resistor values entered by the user in the Setup Window.
3	VS2 Trim Value	0x39	[7:0]	W	This sets the amount of gain trim that is applied to the VS2 ADC reading. This control trims the voltage at the VS2 pin for external resistor tolerances. This control is trimmed until the VS2 Value indicator 4 displays the desired nominal voltage
4	VS2 Value	0x16	[15:4]	R	This value displays the voltage measured at the VS2 pin and scaled using the resistor values entered by the user in the Setup Window.
5	VS3 Trim Value	0x3A	[7:0]	W	This sets the amount of gain trim that is applied to the VS3 ADC reading. This control trims the voltage at the VS3 pin for external resistor tolerances. This control is trimmed until the VS3 Value indicator 7 displays the desired nominal voltage. The Output Voltage Setting 6 Should be set to 100% while trimming VS3
6	Output Voltage Setting	0x31	[7:0]	W	This control is used to change the output voltage. It is programmable from 0% to 155% of nominal voltage.

Table 8. Referring to Figure 8.

No.	Name	REG	Bits	R/W	Description
7	VS3 Value	0x17	[15:4]	R	This value displays the voltage measured at the VS3 pin and scaled using the resistor values entered by the user in the Setup Window.
8	Auto Trim VS1, VS2 and VS3				Follow the three steps mentioned in the "Voltage Trim Procedure", to trim VS3. Then click on this button to Auto-Trim VS1 and VS2
9	VS1 OVP Setting	0x32	[7:3]	W	Local overvoltage limit. This range is programmable from 107.7% to 145.3% of the nominal VS1 voltage. 0x00 corresponds to 108.5%. Each LSB results in an increase of 1.21%.
10	VS1 OV Debounce	0x32	[1:0]	W	Delay before setting the OVP Flag
11	VS1 UVP Setting	0x34	[6:0]	W	This control sets the UVP limit. The range is programmable from 0% to 155% of the nominal VS1 voltage. Each LSB increases the voltage by 155% / 128 = 1.21%
12	VS3 OVP Setting	0x33	[7:3]	W	Local overvoltage limit. This range is programmable from 107.7% to 145.3% of the nominal VS3 voltage. 0x00 corresponds to 107.7%. Each LSB results in an increase of 1.21%.
13	VS3 OV Debounce	0x33	[1:0]	W	Delay before setting the OVP Flag
14	Load OVP (VS2 or VS3) Action	0x09	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
15	Line Impedance Action	0x0C	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
16	Local OVP (VS1) Action	0x0A	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
17	Local UVP (VS1) Action	0x0B	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
18	Regulate with VS3 at all times	0x33	[2]	W	Set the regulating point to VS3 at all times. (If not set, then the ADP1043A uses the VS1 voltage as the regulating point during soft-start)

ORFET SETTINGS

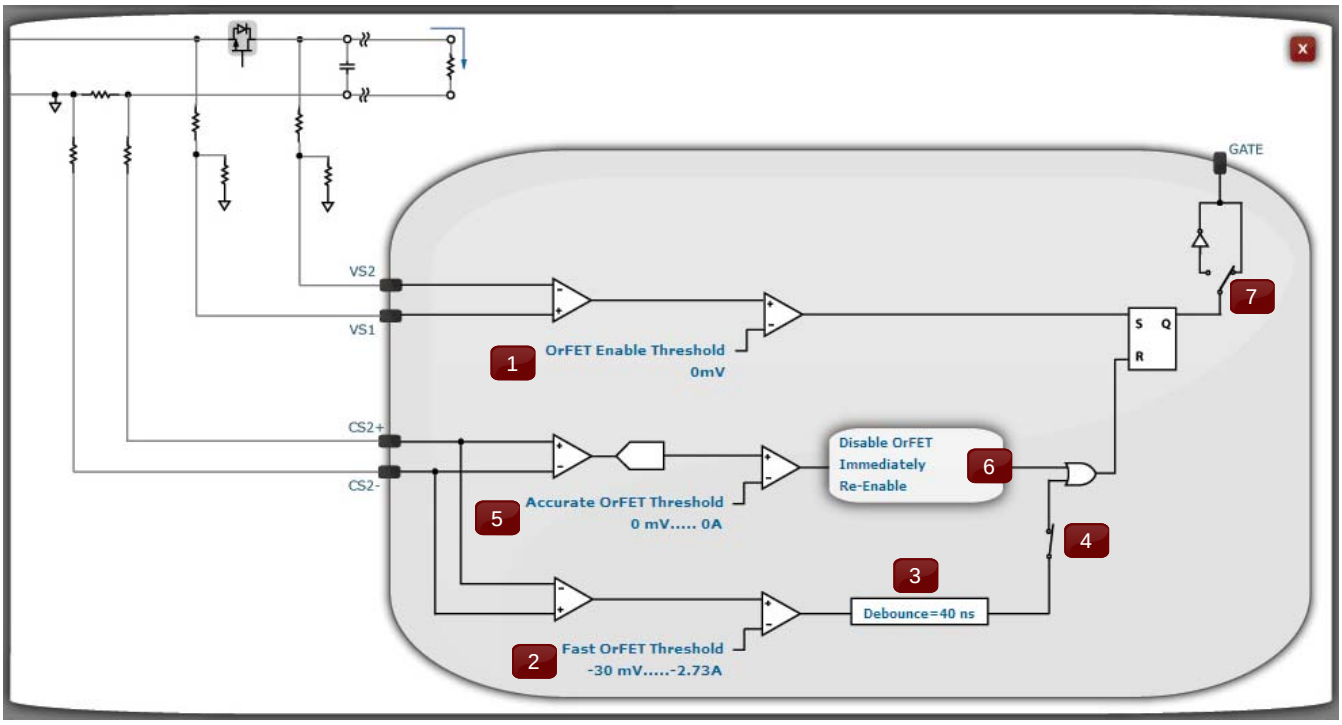

Figure 9.

Table 9. Referring to Figure 9.

No.	Name	REG	Bits	R/W	Description
1	OrFET Enable Threshold	0x30	[5:4]	W	This control programs the voltage difference between VS1 and VS2 before the OrFET is enabled.
2	Fast OrFET Threshold	0x30	[3:2]	W	This control programs the threshold voltage difference between CS2+ and CS2– at which the OrFET is disabled.
3	Debounce	0x30	[1]	W	This control determines the debounce on the fast OrFET control before it disables the OrFET.
4	Fast OrFET Enabled	0x30	[0]	W	This switch enables or disable Fast OrFET
5	Accurate OrFET Threshold	0x30	[7:6]	W	This control programs the voltage difference between CS2+ and CS2– at which the Reverse Voltage flag is set.
6	Reverse Voltage (Accurate OrFET Threshold) Action	0x0C	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.

Table 10. Referring to Figure 9

No.	Name	REG	Bits	R/W	Description
7	Gate Polarity	0x2D	[1]	W	This switch sets the polarity of the OrFET Gate control pin

CS1 SETTINGS

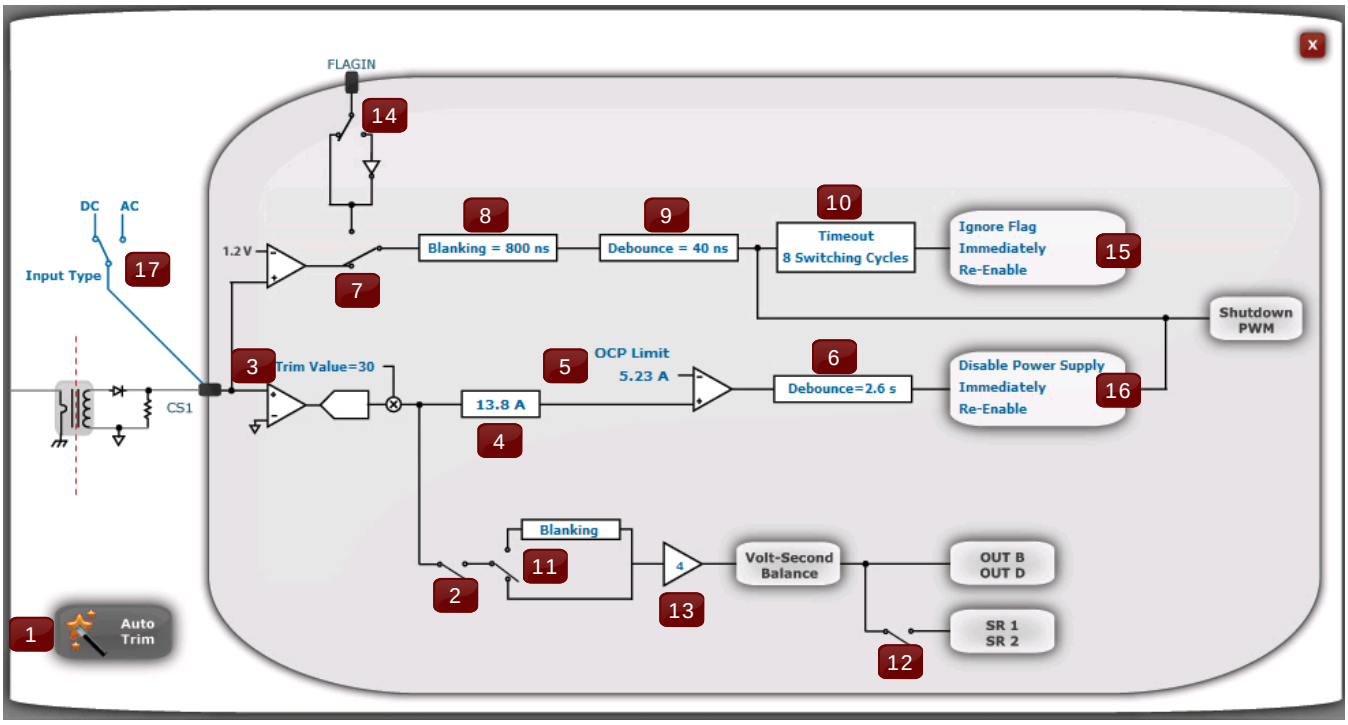

Figure 10.

Table 11. Referring to Figure 10

No.	Name	REG	Bits	R/W	Description
1	Auto Trim				This control is used to start the CS1 automatic trimming routine
2	Enabled	0x27	[5]	W	Enabling this checkbox enables current balance for the main transformer (used for full-bridge configurations). This value introduces extra modulation on the OUTB and OUTD modulating waveforms to give current balance in both branches of the full bridge.
3	Trim Value	0x21	[7:0]	W	This control trims the voltage at the CS1 pin for external resistor and transformer tolerances. This control is trimmed until the CS1 Value indicator 10 displays the desired current.
4	CS1 Value	0x13	[15:4]	R	This value displays the current measured on the primary side. The CS1 ADC gives a value corresponding to the voltage on the CS1 pin, using the resistance value, the software calculates the current at that pin and then scales it using the N1:N2 ratio
5	CS1 Accurate OCP Limit	0x22	[4:0]	W	This control programs the CS1 accurate OCP threshold. The digital word that is output from the CS1 ADC is compared with this threshold setting. If the CS1 ADC reading (Register 0x18) is greater than the OCP threshold set here, then the CS1 OCP flag is set.
6	Accurate OCP OFF Delay	0x0E	[4:2]	R	This control displays the debounce time before the OCP CS2 flag is set.

Table 12. Referring to Figure 10

No.	Name	REG	Bits	R/W	Description
7	Fast OCP Bypass	0x27	[4]	W	Disabling this switch means that the FLAGIN pin is used for CS1 OCP instead of the CS1 pin. Enabling it means that the Fast OCP comparator is used.
8	Blanking	0x22	[7:5]	W	This control determines the blanking time for CS1 before fast OCP is enabled. This time is measured from the start of a switching cycle. It is synchronized with the rising edge of OUTB and OUTD. If regulating using OUTAUX, it is synchronized with the rising edge of OUTAUX.
9	Debounce	0x27	[7:6]	R	This control displays the CS1 debounce value. This is the minimum time that the CS1 signal must be constantly above the fast OCP limit before it shuts down the PWMs. Once this happens, all PWM's are disabled for the remainder of the switching cycle.
10	Timeout	0x27	[1:0]	W	If the CS1 Fast OCP comparator is set, all PWM's are immediately disabled for the remainder of the switching cycle. The PWM's resume as normal at the beginning of the next switching cycle. This sets the number of consecutive switching cycles where the comparator is set before the CS1 FAST OCP flag is set.
11	Leading Edge Blanking	0x27	[2]	R/W	Setting this switch to "Blanking" means that the current spike at the beginning of each CS1 reading is ignored by the VS Balance circuit
12	VS Balance on SR PWMs	0x52	[1]	R/W	Enabling this switch means that the VSBalance circuit will also modulate SR1 and SR2, along with OUTB and OUTD. When set, it is the rising edge of SR1 and SR2 that the VSBalance modulation is applied to.
13	Gain	0x28	[1:0]	R/W	If the CS1 Fast OCP comparator is set, all PWM's are immediately disabled for the remainder of the switching cycle. The PWM's resume as normal at the beginning of the next switching cycle. This sets the number of consecutive switching cycles where the comparator is set before the CS1 FAST OCP flag is set.
14	Flag-In Polarity	0x2D	[2]	W	This switch sets the polarity of the FlagIN input pin
15	CS1 Fast OCP Action	0x08	[5:4]	W	This control sets the action that the ADP1043A performs once this flag is set.
	Timing	0x08 0x27	[7] [7:6]	W	This sets the debounce between the flag being set and the action.
	Resolve Issue		[6]	W	This sets whether to re-enable or remain disabled after the flag is set.
16	CS1 Accurate OCP Action	0x08	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing	0x08 0x0E	[3] [4:2]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
17	CS1 Input Type				This switch lets you specify the type of signal the CS1 pin is seeing. This value is used then used to accurately calculate CS1 value

CS2 SETTINGS

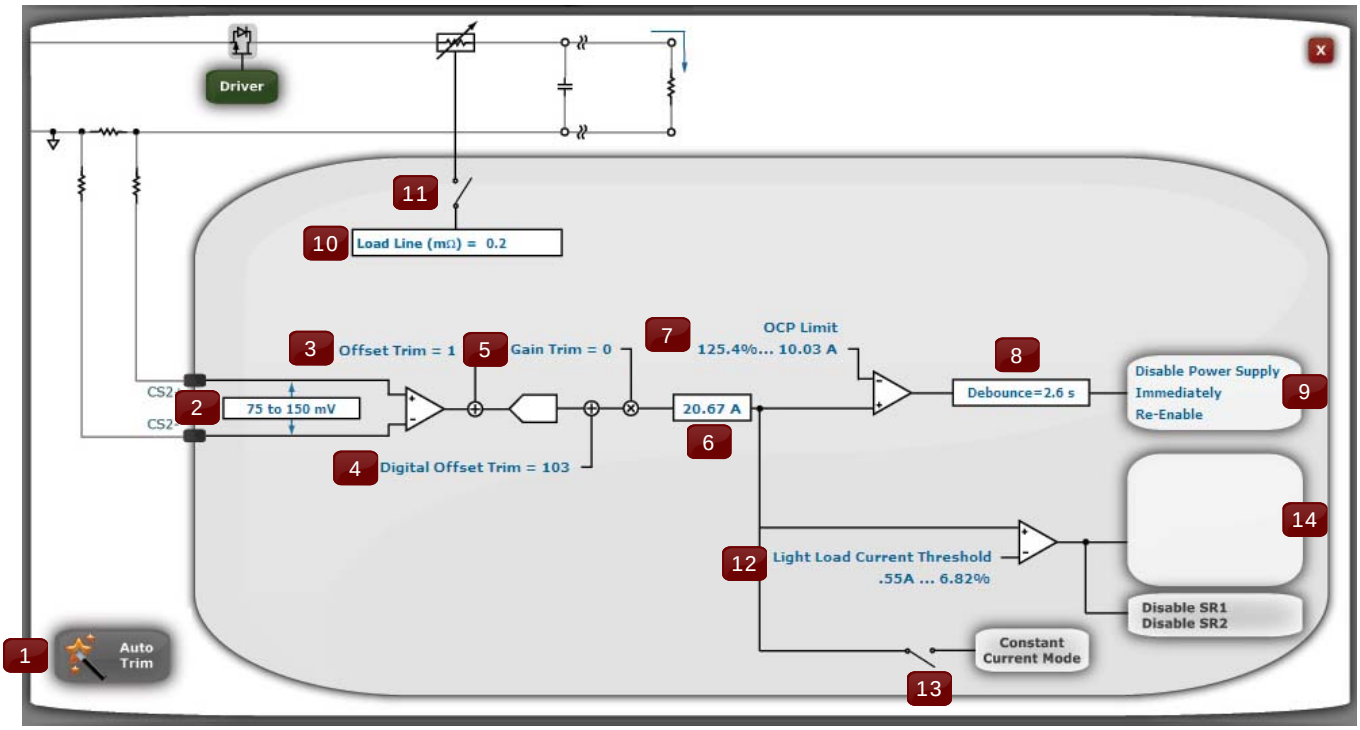

Figure 11.

Table 13. Referring to Figure 11.

No.	Name	REG	Bits	R/W	Description
1	Auto Trim				This control is used to start the CS1 automatic trimming routine
2	CS2 Nominal Voltage	0x23	[7:6]	W	This control sets the nominal full-load voltage drop across the sense resistor
3	Offset Trim	0x24	[6:0]	W	This control calibrates the secondary side (CS2) current sense common-mode error. It calibrates for errors in the resistor divider network.
4	Digital Offset Trim	0x25	[7:0]	W	This control is used to calibrate the CS2 value that is read in Register 0x18
5	Gain Trim	0x23	[5:0]	W	This control calibrates the secondary side (CS2) current sense gain. It calibrates for errors in the sense resistor.
6	CS2 Value	0x18	[15:4]	R	This value displays the output current. The CS2 ADC gives a value corresponding to the voltage drop across the CS2 pins, using the Rsense resistance value, the software calculates the output current and is scaled using the CS2 Nominal Voltage Setting
7	CS2 Accurate OCP Limit	0x26	[7:0]	W	This control programs the CS2 OCP threshold. The digital word that is output from the CS2 ADC is compared with this threshold setting. If the CS2 ADC reading (Register 0x18) is greater than the OCP threshold set here, then the CS2 OCP flag is set. This value should be programmed only after the CS2 offset, gain, and digital trims have been performed.

Table 14. Referring to Figure 11.

No.	Name	REG	Bits	R/W	Description
8					

	Accurate OCP OFF Delay	0x0E	[4:2]	R	This control displays the debounce before the OCP CS2 flag is set.
9	CS2 Accurate OCP Action	0x09	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing	0x09 0x0E	[7] [4:2]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
10	Load Line Setting	0x36	[2:0]	W	This control sets the impedance for the Load Line Setting
11	Load Line Enable	0x36	[3]	W	This switch enables or disables the load line. This sets how much the output voltage decreases from nominal at full load. For example, a 12V system, programmed with an 8% load-line means that the output voltage will vary from 12V at no load to 11.04V at 100% load.
12	Light Load Current Threshold	0x3B	[2:0]	W	This control sets the load current limit on the CS2 ADC below which the Sync Rectifier (SR1 and SR2) outputs are disabled. This value also determines the point at which the power supply goes into DCM mode. Below this limit, the DCM filter registers are used. Above this limit, the CCM filter registers are used. This value is programmable from 0 to 46mV of the CS2 ADC . There is an 8mV hysteresis on this signal.
13	Constant Current Mode	0x27	[3]	W	This switch is used to enable constant current mode
14	Disable OUT"X"	0x3B	[7:3]	W	Enabling this checkbox means that the corresponding output will also be disabled if the load current drops below the Light Load Current threshold.

REGISTER ACCESS

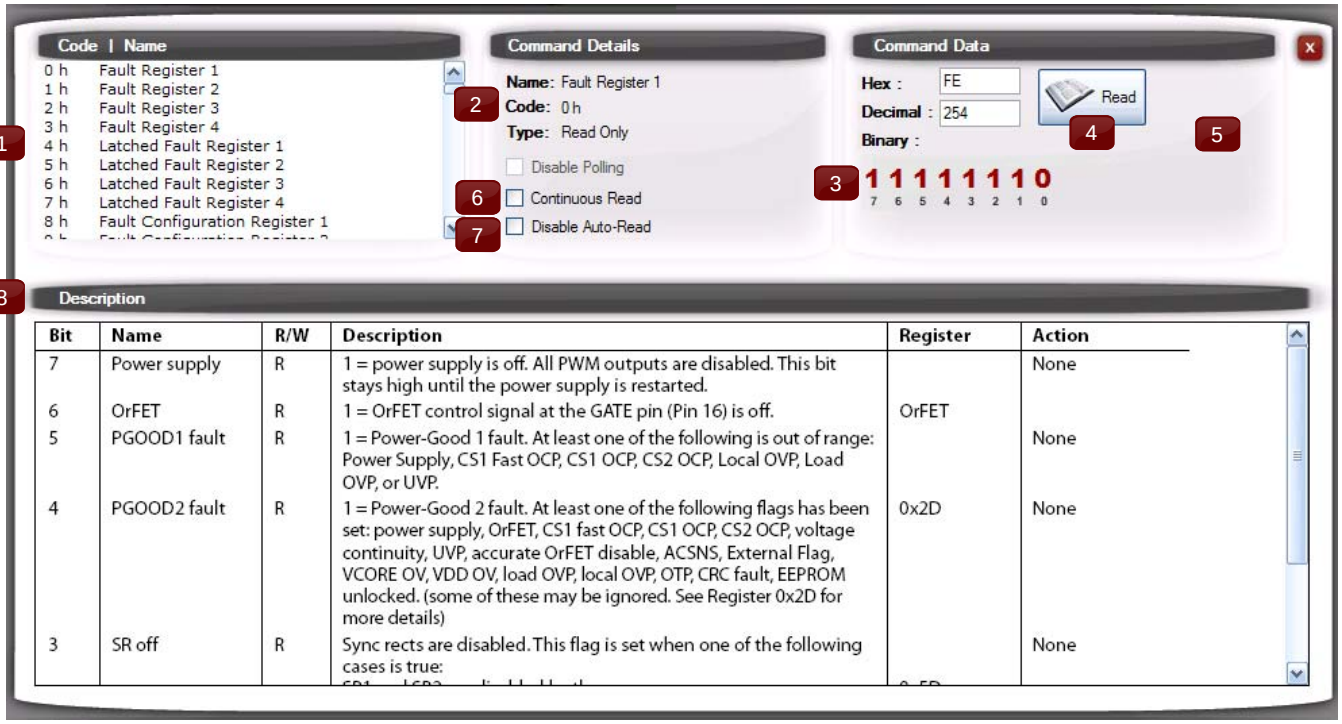

Figure 12.

Table 15. Referring to Figure 12.

No.	Name	REG	Bits	R/W	Description
1	Register Map	0x00 – 0x7E			This control displays the complete ADP1043A register map, Selecting any particular register will display the data contained in that register, and will allow this register to be read and written to.
2	Register Details				These set of indicators display the selected register's *(selected in* 1 *)* Command Name, Code and its value in hexadecimal and decimal formats.
3	Bit Display				This control / indicator displays the current value of the selected register, and can be modified by clicking on the individual bits.
4	Read				This control reads the value of the register selected by control 1
5	Write				This control writes the value to the register selected by control 1
6	Continuous Read				If this checkbox is enabled then the GUI will continuously read the value of the register selected in control 1
7	Disable Automatic Read-Back				The GUI automatically does a read operation after a write operation to verify if the write operation was successful. Enabling this checkbox disables this automatic read-back feature.
8	Description				This indicator displays the description of the selected register

TOPOLOGY PWM AND SR SETUP

GENERAL

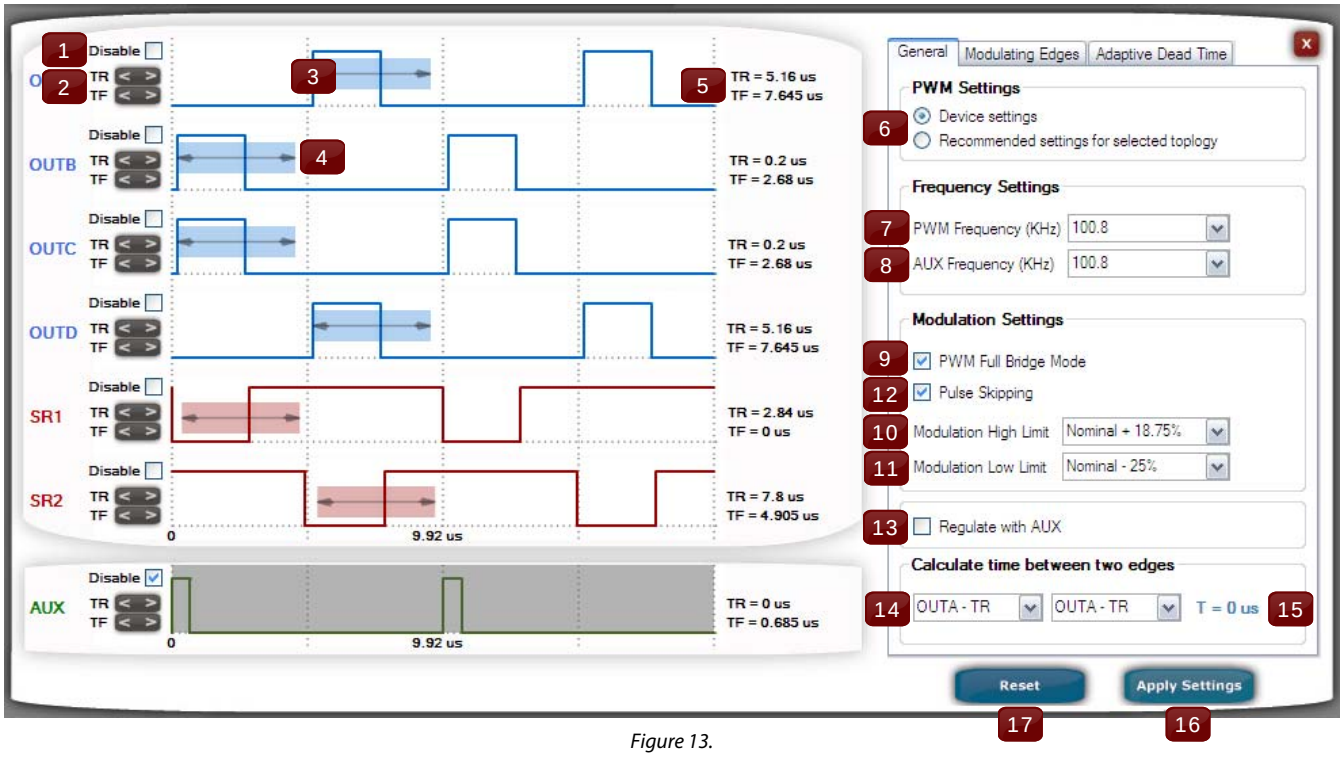

Figure 13.

Table 16. Referring to Figure 13.

No.	Name	REG	Bits	R/W	Description
1	Disable "XXXXX"	0x5D	[7:1]		Enabling this checkbox disables the corresponding output
2	T"X" < >				This Control increases or decreases the corresponding edge timing in 5ns steps
3	PWM Edges	0x41 0x43 0x45 0x47 0x49 0x4B 0x4D 0x4F 0x51 0x53 0x55 0x57 0x59 0x5B	[7:0]	W	Both the rising and falling PWM edges can be clicked on and dragged to move to the desired position to set the positive and negative edge timings

Table 17. Referring to Figure 13.

No.	Name	REG	Bits	R/W	Description
4	Modulation Limits Box				These boxes display the modulation limits for that edge. These are set using controls 9 10 11. Changing the limits will be displayed here.
5	Timings				These indicators display the positive and negative edge timings set by controls 2 3
6	PWM Settings				This control lets a user select between the settings stored in the part, or ADI recommended settings for the selected topology
7	PWM Frequency	0x40	[5:0]	W	This control sets the switching frequency of OUTA, OUTB, OUTC, OUTD, SR1, SR2.
8	AUX PWM Frequency	0x3F	[5:0]	W	This control sets the switching frequency of the OUTAUX signal
9	PWM Full-Bridge Mode Enabled	0x2E	[7]	W	Enable this control when operating in full-bridge mode. This mode distributes the modulation equally between two PWMs instead of one. It affects the modulation high limit and the modulation low limit settings.
10	Modulation High Limit	0x2E	[6:4]	W	This control sets the maximum allowed modulation that will be applied to a PWM. The value is a percentage of the switching period. Changes here will be displayed in 4
11	Modulation Low Limit	0x2E	[1:0]	W	This control sets the minimum allowed modulation that will be applied to a PWM. If the modulation calculated is to be lower than this limit, pulse skipping 12 can be enabled. The value is a percentage of the switching period. Changes here will be displayed in 4
12	Pulse Skipping Enabled	0x2E	[2]	W	Enabling this checkbox enables pulse skipping mode. If the ADP1043A requires a duty cycle lower than the Modulation Low Limit, pulse skipping will be enabled.
13	Regulate with OUTAUX	0x5C	[1]	W	If this checkbox is enabled then control loop PWM modulation is regulated by OUTAUX. The CS1 blanking signal is synchronized with OUTAUX If this checkbox is disabled then control loop PWM modulation is regulated by OUTA, OUTB, OUTC, OUTD, SR1 and SR2.
14	Timings				Select any two edges using these controls. The difference between these edges is calculated in 15
15	Time Display				This indicator displays the requested difference in times between the edges selected by controllers 14
16	Apply Settings				This control programs all the PWM settings to the part and then writes to bit 0 of register 0x5D. This bit latches in all registers from Address 0x40 to Address 0x5D. This is to prevent the PWM timing from being temporarily incorrect, if changing PWM timing while the power supply is on.
17	Reset				This button loads the settings programmed in the ADP1043A connected to the software

MODULATING EDGES

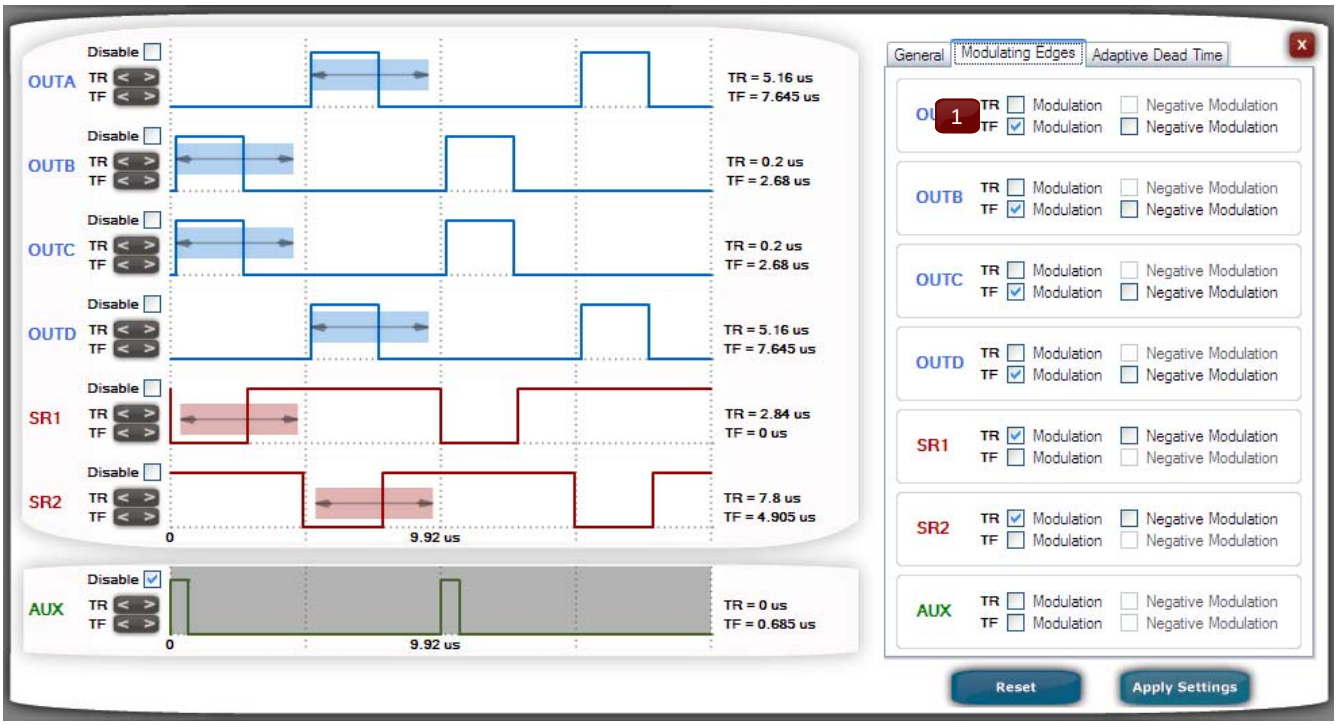

Figure 14.

Table 18. Referring to Figure 14.

No.	Name	REG	Bits	R/W	Description
1	Modulation on T "X" Edge	0x42 0x44 0x46 0x48 0x4A 0x4C 0x4E 0x50 0x52 0x54 0x56 0x58 0x5A 0x5C	[3]	W	Enabling this checkbox enables modulation on the corresponding edge

ADAPTIVE DEAD TIME

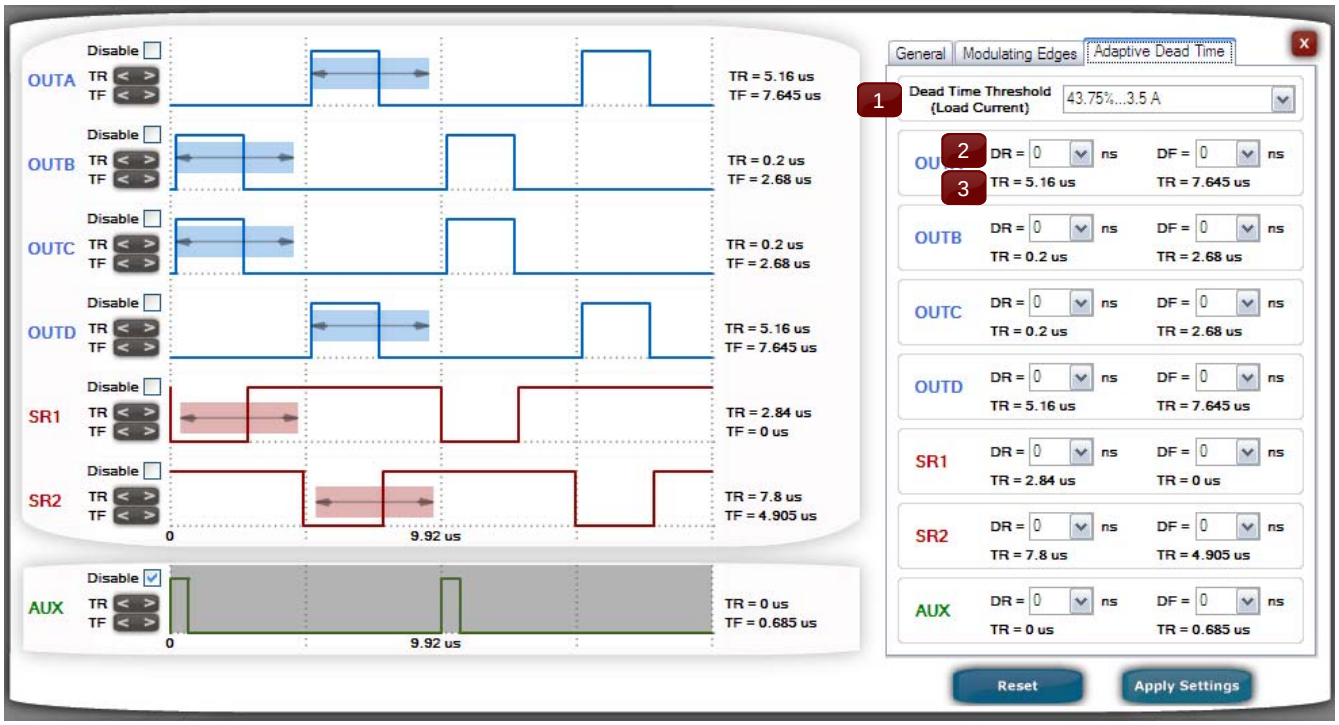

Figure 15.

Table 19. Referring to Figure 15.

No.	Name	REG	Bits	R/W	Description
1	Dead Time Threshold	0x68	[2:0]	W	This value determines the adaptive dead time threshold. Below this load current, the offsets from Register 0x69 to Register 0x6F will be introduced.
2	D "X" (ns)	0x69 0x6A 0x6B 0x6C 0x6D 0x6E 0x6F	[7:0]	W	This control sets the offset from the nominal timing for the corresponding edge and output
3	T "X"				This indicator displays then new time for the edge after adding or subtracting the offset to the nominal time

RESONANT MODE

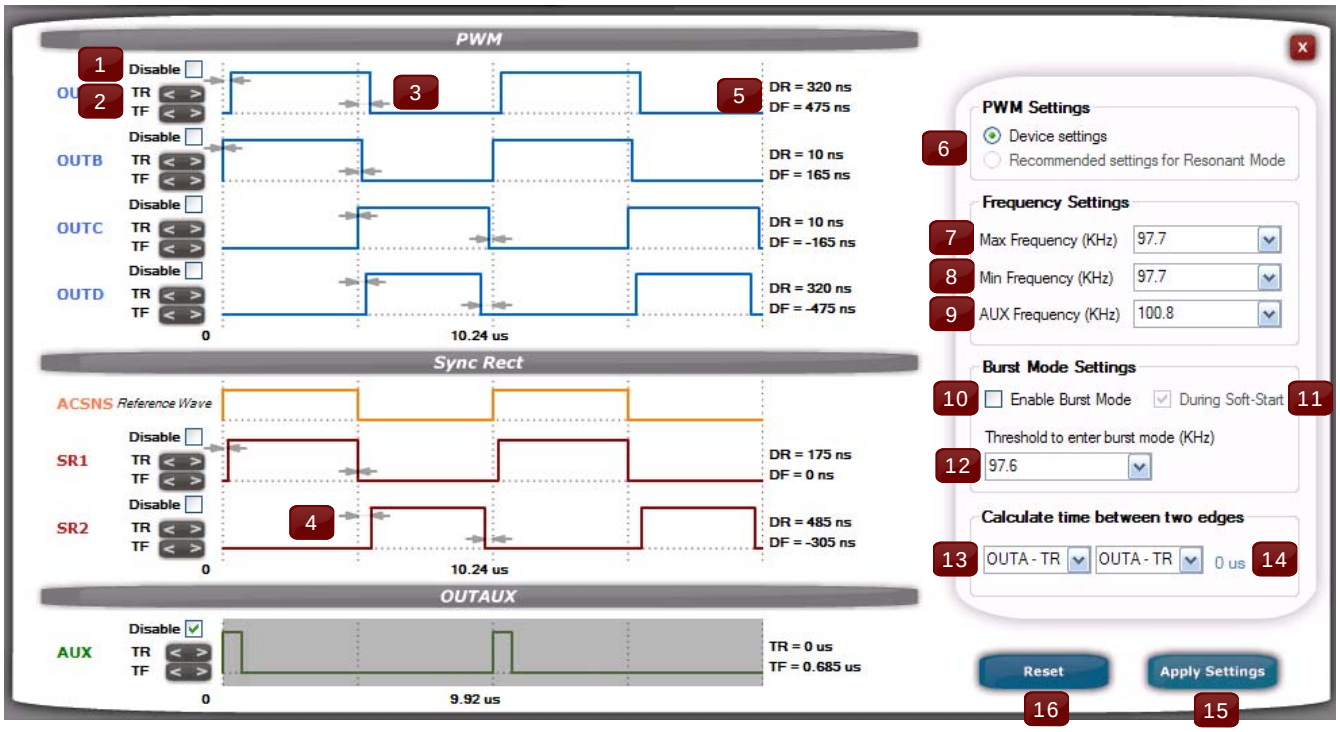

Figure 16.

Table 20. Referring to Figure 16.

No.	Name	REG	Bits	R/W	Description
1	Disable "XXXXX"	0x5D	[7:1]		Enabling this checkbox disables the corresponding output
2	T"X" < >				This Control increases or decreases the corresponding edge timing in 5ns steps
3	PWM Edges	0x41 0x43 0x45 0x47 0x49 0x4B 0x4D 0x4F 0x51 0x53 0x55 0x57 0x59 0x5B	[7:0]	W	Both the rising and falling PWM edges can be clicked on and dragged to move to the desired position to set the positive and negative edge timings

Table 21. Referring to Figure 13.

No.	Name	REG	Bits	R/W	Description
4	Arrows				These arrows display the time between the nominal value and the location where the edge is set
5	Timings				These indicators display the positive and negative edge timings set by controls 2 3
6	PWM Settings				This control lets a user select between the settings stored in the part, or ADI recommended settings for the selected topology
7	MAX Frequency	0x46 0x48	[7:0] [7:4]	W	This control sets the maximum switching frequency of OUTA, OUTB, OUTC, OUTD, SR1, SR2.
8	MIN Frequency	0x42 0x44	[7:0] [7:4]	W	This control sets the minimum switching frequency of OUTA, OUTB, OUTC, OUTD, SR1, SR2.
9	AUX PWM Frequency	0x3F	[5:0]	W	This control sets the switching frequency of the OUTAUX signal
10	Enable Burst Mode	0x4A	[6]	W	These bits enable burst mode when the desired switching frequency for regulation is higher than the threshold set in 12
11	During Soft-Start	0x4A	[7]	W	These bits enable burst mode when the desired switching frequency for regulation is higher than the threshold set in 12 during soft-start
12	Threshold to enter Burst Mode	0x4A	[5:0]	W	This control sets the frequency at which the part enter burst mode
13	Timings				Select any two edges using these controls. The difference between these edges is calculated in 15
14	Time Display				This indicator displays the requested difference in times between the edges selected by controllers 14
15	Apply Settings				This control programs all the PWM settings to the part and then writes to bit 0 of register 0x5D. This bit latches in all registers from Address 0x40 to Address 0x5D. This is to prevent the PWM timing from being temporarily incorrect, if changing PWM timing while the power supply is on.
16	Reset				This button loads the settings programmed in the ADP1043A connected to the software

FILTER SETTINGS

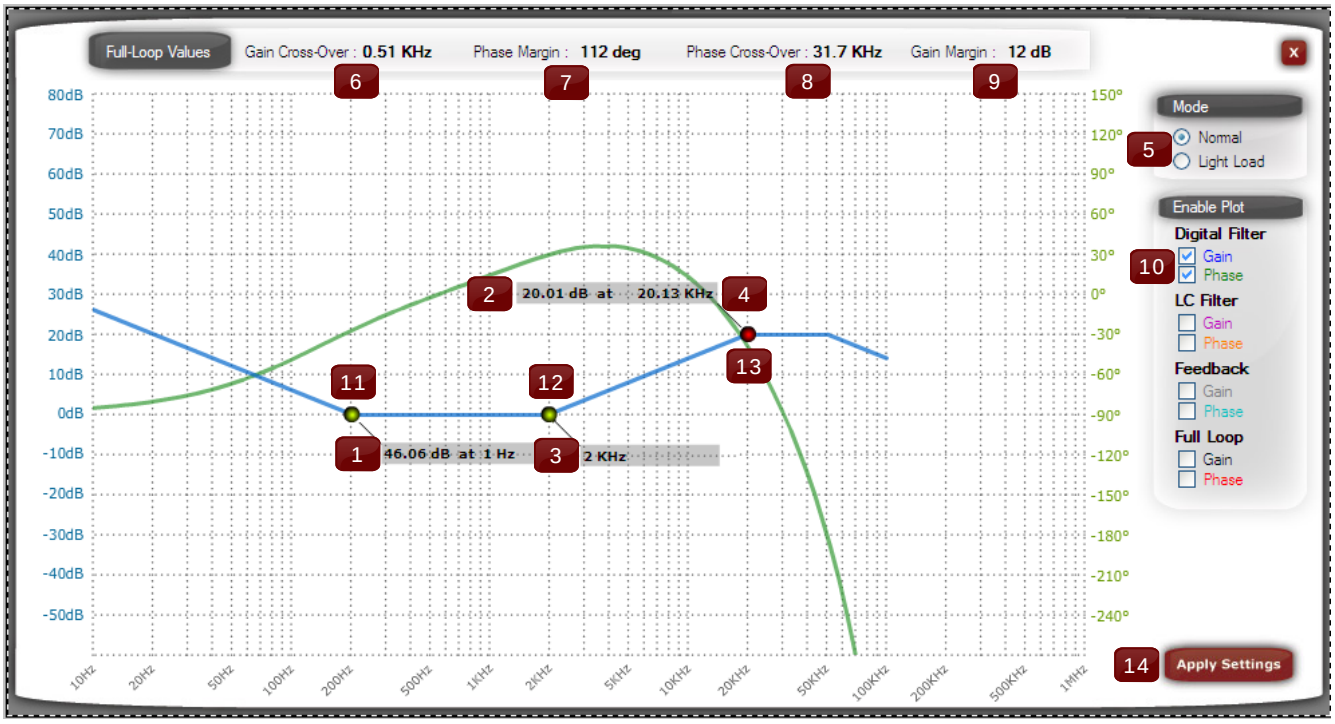

Figure 17.

Table 22. Referring to Figure 17.

No.	Name	REG	Bits	R/W	Description
1	Low Frequency Gain	0x60 0x64	[5:0]	R	This indicator displays the low frequency gain of the loop response. Programmable over a20 dB range. It has a resolution of 0.3dB. (0x60 is for Normal Mode and 0x64 is for Light-Load Mode)
2	High Frequency Gain	0x63 0x67	[5:0]	R	This indicator displays the high frequency gain of the loop response. (0x63 is for Normal Mode and 0x67 is for Light-Load Mode)
3	Zero Frequency	0x61 0x65	[5:0]	R	This indicator displays the position of the final zero. (0x61 is for Normal Mode and 0x65 is for Light-Load Mode)
4	Pole Frequency	0x62 0x66	[5:0]	W	This indicator displays the position of the final pole. (0x62 is for Normal Mode and 0x66 is for Light-Load Mode)
5	Settings Radio Buttons				These radio buttons selcet between the Light Load Mode Settings and Normal Mode Settings
6	Loop Filter Gain Cross-over Frequency				This indicator displays the full loop filter Gain Cross-over Frequency
7	Loop Filter Phase Margin				This indicator displays the full loop phase margin for the power supply
8	Loop Filter Phase Cross-over Frequency				This indicator displays the full loop filter phase Cross-over Frequency
9	Loop Filter Gain Margin				This indicator displays the full loop gain margin for the power supply

Table 23. Referring to Figure 17.

No.	Name	REG	Bits	R/W	Description
10	Enable Plot				If the checkbox is enabled then the corresponding plot is plotted on the graph
11	Green Dot 1	0x60 0x64	[5:0]	R	The green dot can be moved left or right, and this in turn sets the low frequency gain of the loop response. Programmable over a20 dB range. It has a resolution of 0.3dB. (0x60 is for Normal Mode and 0x64 is for Light-Load Mode)
12	Green Dot	0x61 0x65	[5:0]	R	The green dot can me moved left or right and is used to set the Zero Frequency (0x61 is for Normal Mode and 0x65 is for Light-Load Mode)
13	Red Dot	0x63 0x67 0x62 0x66	[5:0]	R	The red dot can be moved left, right, up or down, which sets the high frequency gain of the loop response. (0x63 is for Normal Mode and 0x67 is for Light-Load Mode). It is also used to set the pole frequency(0x62 is for Normal Mode and 0x66 is for Light-Load Mode)
14	Apply Settings				This control programs all the above values to the corresponding registers and bits .

SHARE BUS SETTINGS

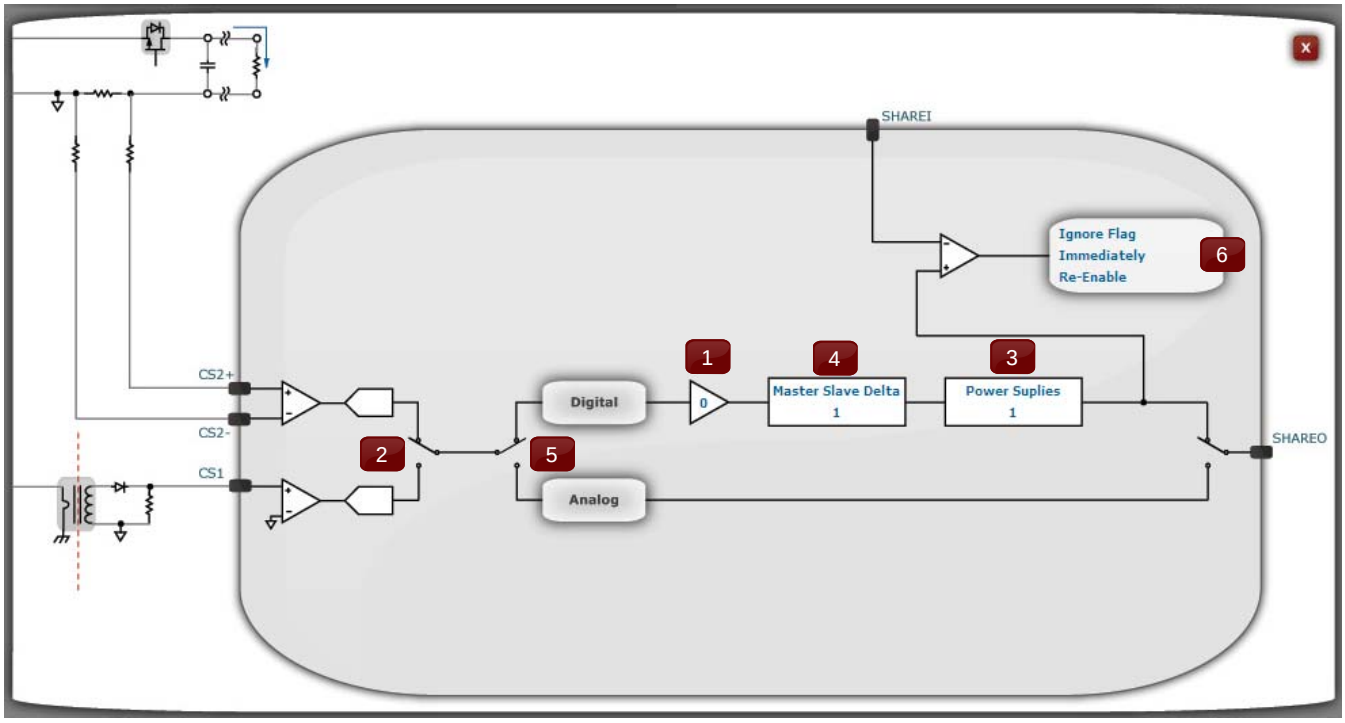

Figure 18.

Table 24. Referring to Figure 18.

No.	Name	REG	Bits	R/W	Description
1	Share Bus Bandwidth	0x29	[2:0]	W	This control sets the share bus bandwidth
2	Current Sensing options for Current Sharing	0x29	[3]	W	This switch selects between CS1 and CS2 sensing, the selected ADC is used for performing current sharing.
3	Power Supplies	0x2A	[7:4]	W	This determines how much a Master reduces his output voltage to maintain current sharing.
4	Current Share Difference between master and slave	0x2A	[3:0]	W	This determines how close a Slave tries to match the current of the Master device. The higher the setting, the larger the distance that satisfies the current sharing criteria
5	Current Sensing Type	0x29	[4]	W	Setting this switch to analog will result in the Current Sense ADC reading coming directly out on the ShareO pin. This bitstream can be used for analog current sharing. Setting this switch to digital will result in the Digital Share Bus signal coming out on the ShareO pin. This can be used for digital current sharing.
6	Share Bus Action	0x0D	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.

GENERAL SETTINGS

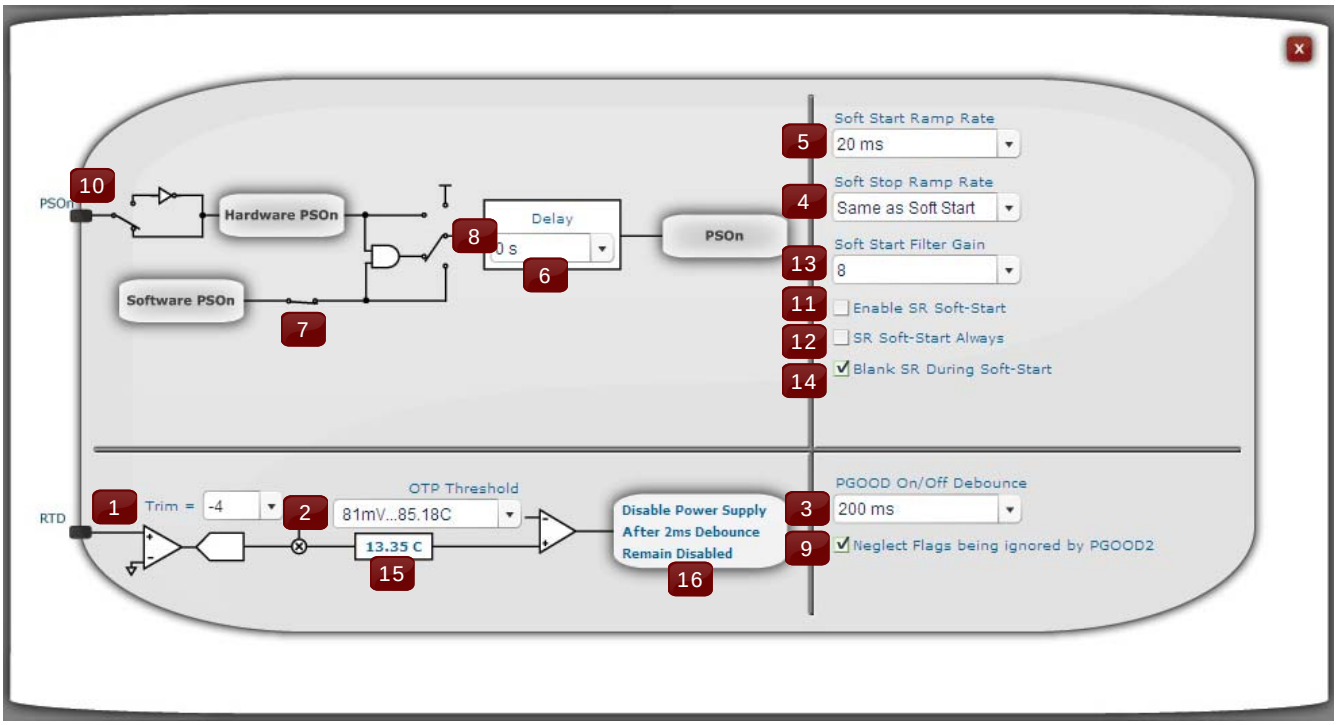

Figure 19.

Table 25. Referring to Figure 19.

No.	Name	REG	Bits	R/W	Description
1	Trim	0x2B	[4:0]	W	This control calibrates the RTD ADC gain. It calibrates for errors in the ADC. This trim allows ±12% trim to be realized.
2	OTP Threshold	0x2F	[7:0]	W	This is the value that is compared to the RTD ADC reading. If the RTD ADC reading is lower than the threshold set here, then the OTP flag is set. (The reason that the flag is set below the threshold is that using an NTC causes the reading to decrease as the temperature increases). Each LSB corresponds typically to an increased OTP threshold of 3 mV. Note that the RTD ADC range is 0 V to 1.58V, and that the OTP threshold is 0 V to 765 mV. There is a hysteresis of 12mV on the OTP flag.
3	PGOOD ON/OFF Debounce	0x2D	[7:4]	W	At startup, there is a delay before PGOOD1 is enabled. PGOOD1 is not enabled until a period of time after the following signals are all within normal limits: ACSNS, OCP CS1, OCP CS2, VS1 OVP,VS2 OVP, and UVP. When PSON is disabled, there is a delay before PGOOD1 is disabled. This delay is programmed using this control.
4	Soft Stop	0x2C	[2]	W	This control is used to enable or disable the Soft-Stop feature
5	Soft Start Ramp Rate	0x2C	[1:0]	W	This control is used to set the rise time of the Soft-Start ramp
6	PS_ON Delay Time	0x2C	[4:3]	W	This control sets the time from when the PS_ON signal is set to when the soft-start begins.

Table 26. Referring to Figure 19.

No.	Name	REG	Bits	R/W	Description
7	PS ON	0x2C	[5]	W	This control turns ON or OFF the PSON control signal when Software PSON is selected.
8	PSON Type	0x2C	[7:6]	W	This control selects between the different Software and Hardware PSON options.
9	Neglect Flags being ignored by PGOOD2	0x2D	[3]	W	0 = Any flag can set the PGOOD2 pin 1 = Any flag that is not Ignored can set the PGood2 pin.
10	PSON Polarity	0x2D	[0]	W	This control sets the polarity of the PSON input pin: If Inverted then low = on
11	Enable SR Soft-Start	0x54	[0]	W	Setting this means that the SR signals will have a soft-start function
12	SR Soft-Start Always	0x54	[1]	W	Checked = SR signals will soft-start every time they are enabled. Unchecked = SR Signals will soft-start only the first time that they are enabled.
13	Soft-Start Filter Setting	0x5F	[1:0]	W	This control determines the bandwidth of the low pass digital filter that is used during soft-start
14	Blank SR During Soft Start	0x0F	[7]	W	Setting this checkbox means that SR is ignored until the end of the soft-start ramp time.
15	Temperature	0x1A	[15:4]	R	This value displays the temperature in degrees Celsius, which is converted from the voltage measured at the RTD pin.
16	OTP Action	0x0B	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.

FLAG SETTINGS

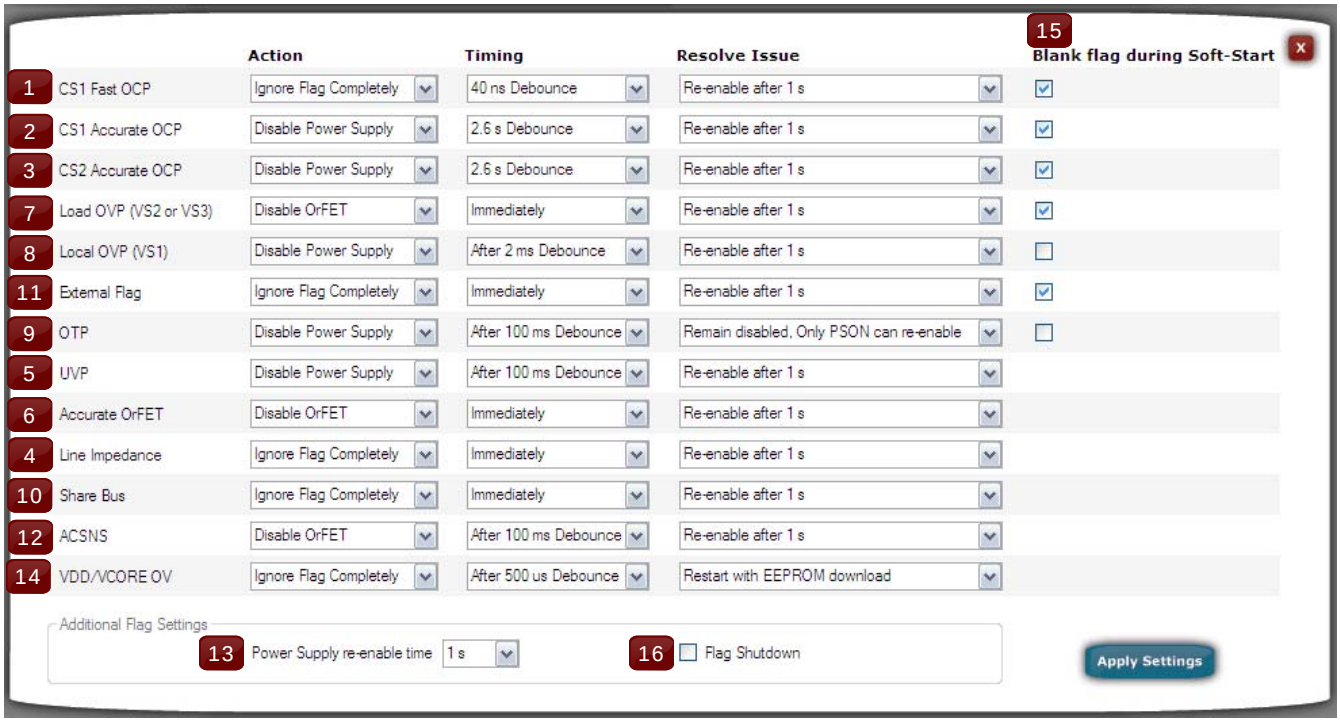

Figure 20.

Table 27. Referring to Figure 20.

No.	Name	REG	Bits	R/W	Description
1	**CS1 Fast OCP**				
	Action	0x08	[5:4]	W	This control sets the action that the ADP1043A performs once this flag is set.
	Timing	0x08 0x27	[7] [7:6]	W	This sets the debounce between the flag being set and the action.
	Resolve Issue		[6]	W	This sets whether to re-enable or remain disabled after the flag is set.
2	**CS1 Accurate OCP**				
	Action	0x08	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing	0x08 0x0E	[3] [4:2]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
3	**CS2 Accurate OCP**				
	Action	0x09	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Timing	0x09 0x0E	[7] [4:2]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.

Table 28. Referring to Figure 20.

No.	Name	REG	Bits	R/W	Description
4	**Line impedance**	0x0C	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
5	**UVP**	0x0B	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
6	**Reverse Voltage (Accurate OrFET Threshold)**	0x0C	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
7	**Load OVP (VS2 or VS3)**	0x09	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
8	**Local OVP (VS1)**	0x0A	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
9	**OTP**	0x0B	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.

Table 29. Referring to Figure 20.

No.	Name	REG	Bits	R/W	Description
10	**Share Bus**	0x0D	[5:4]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[7]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
11	**External Flag Input (FLAGIN)**	0x0A	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
12	**ACSNS**	0x0D	[1:0]	W	This control sets the action that the ADP1043A needs to take once the flag is set.
	Action				
	Timing		[3]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[2]	W	This control selects whether to re-enable ADP1043A or remain disabled after the flag is set.
13	Power Supply Re-Enable Time	0x0E	[1:0]	W	This control sets the Power Supply re-enable time
14	VDD / VCORE OV	0x0E	[7]	W	Setting this bit means that the VDD OV and VCORE OV Flags will be ignored
	Timing		[5]	W	This control sets a debounce between the flag being set and the action that the ADP1043A needs to take.
	Resolve Issue		[6]	W	Setting this bit to 1 means that if the part shuts down, it will download EEPROM contents again before restarting. Setting this bit to 0 means that the part shuts down. It does not download EEPROM.
15	Blank Flag During Soft Start	0x0F	[6:0]	W	Setting this checkbox means that corresponding flag is ignored until the end of the soft-start ramp time.
16	Flag Shutdown	0x34	[7]	W	This bit is only valid when the OUTAUX is used for regulation. Checked: When any flag decides to shutdown the power supply, OUTAUX PWM is immediately shutdown, and all other PWM's are shutdown at the end of the switching cycle. Un-Checked: When any flag decides to shutdown the power supply, OUTAUX PWM is immediately shutdown, and all other PWM's are also immediately shutdown.

MONITOR

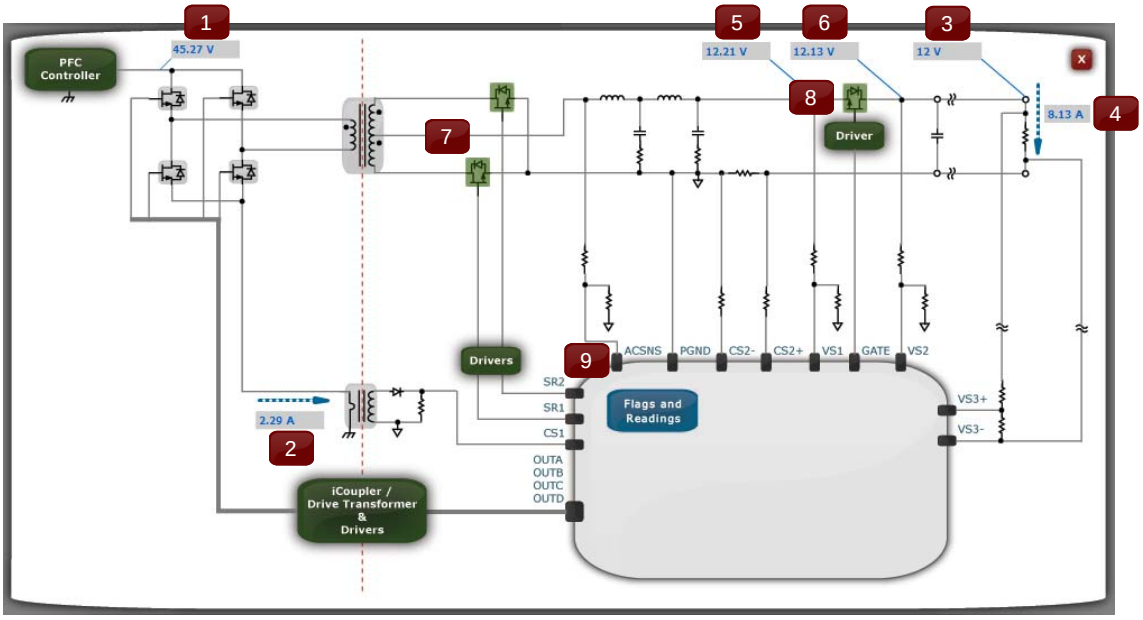

Figure 21.

Table 30. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
1	I/P Voltage				This indicator displays the input voltage calculated by the GUI using the duty cycle, VS3 and the N1:N2 values
2	I/P Current	0x13	[15:4]	R	This value displays the current measured on the primary side. The CS1 ADC gives a value corresponding to the voltage on the CS1 pin, using the Rcs1 resistance value, the software calculates the current at that pin and then scales it using the N1:N2current transformer ratio
3	O/P Voltage	0x17	[15:4]	R	This value displays the voltage measured at the VS3 pin and scaled using the 1 and R2 values entered by the user.
4	O/P Current	0x18	[15:4]	R	This value displays the output current. The CS2 ADC gives a value corresponding to the voltage drop across the CS2 pins, using the Rsense resistance value, the software calculates the output current and is scaled using the CS2 Nominal Voltage Setting
5	VS1	0x15	[15:4]	R	This value displays the voltage measured at the VS1 pin and scaled using the R1 and R2 values entered by the user.
6	VS2	0x16	[15:4]	R	This value displays the voltage measured at the VS2 pin and scaled using the R1 and R2 values entered by the user.
7	SR OFF	0x00	[3]	R	Red = Sync rects are disabled. This flag is enabled when any of these three cases is true: • SR1 and SR2 are disabled by the user. • The load current has fallen below the threshold in Register 0x3C. • A flag that was configured to disable the sync rects has been set.

Table 31. Referring to Figure 21.

No.	Name	REG	Bits	R/W	Description
8	OrFET	0x00	[6]	R	Red = OrFET control signal at the GATE pin (Pin 16) is off.
9	ADP1043A Monitor Blocks				The grey block represents ADP1043A and the blue blocks represent the various monitor blocks of the ADP1043A. These blue blocks can be clicked to open the corresponding window for monitor

FLAGS AND POWER MONITORING

Figure 22.

Table 32. Referring to Figure 22.

No.	Name	REG	Bits	R/W	Description
1	Power Supply	0x00	[7]	R	Red = Power supply is off. All PWM outputs are disabled. This bit stays high until a PS ON is performed.
	OrFET	0x00	[6]	R	Red = OrFET control signal at the GATE pin (Pin 16) is off.
	PGOOD1 Fault	0x00	[5]	R	Red = Power-good 1 fault. At least one of the following is out of range: ACSNS, OCP CS1, OCP CS2, VS1 OVP, VS2 OVP, or UVP.
	PGOOD2 Fault	0x00	[4]	R	Red = Power-good 2 fault. Any of these flag has been set: Power Supply, OrFET, Fast OCP CS1, OCP CS1, OCP CS2, Voltage Continuity, UVP, Accurate OrFET Disable, V_{DD}UV, V_{CORE} OV, V_{DD} OV, Load OVP, Local OVP, OTP, CRC Fault, EEPROM Unlocked
	SR OFF	0x00	[3]	R	Red = Sync rects are disabled. This flag is enabled when any of these three cases is true: • SR1 and SR2 are disabled by the user. • The load current has fallen below the threshold in Register 0x3C. • A flag that was configured to disable the sync rects has been set.
	Fast OCP (CS1)	0x00	[2]	R	Red = Fast OCP current is above its Over Current Protection limit. This is a 1.2V threshold on the CS1 pin. Fast OCP is a comparator
	OCP CS1	0x00	[1]	R	Red = CS1 current is above its Accurate Over Current Protection limit
	OCP CS2	0x00	[0]	R	Red = CS2 current is above its Accurate Over Current Protection limit

Table 33. Referring to Figure 22.

No.	Name	REG	Bits	R/W	Description
2	Voltage Continuity	0x01	[7]	R	Red = Voltage differential between VS1, VS2, VS3 pins is outside limits. Either (VS1 − VS2) > 100 mV or (VS2 − VS3) > 100 mV.
	UVP	0x01	[6]	R	Red = VS1 is below its undervoltage limit.
	Accurate OrFET Disable	0x01	[5]	R	Red = Reverse voltage across CS2 pins is above limit. This is the Accurate OrFET Reverse Voltage.
	VDD UV	0x01	[4]	R	Red = V_{DD} is below limit.
	VCORE OV	0x01	[3]	R	Red = 2.5 V V_{CORE} is above limit.
	VDD OV	0x01	[2]	R	Red = V_{DD} is above limit. The I2C interface stays functional, but a PS_ON toggle is required to restart the power supply.
	Load OVP	0x01	[1]	R	Red = VS2 or VS3 is above its overvoltage limit.
	Local OVP	0x01	[0]	R	Red = VS1 is above its overvoltage limit.
3	OTP	0x02	[7]	R	Red = Temperature is above OTP limit.
	Reserved	0x02	[6]	R	Reserved
	Share Bus	0x02	[5]	R	Red = Current share is outside regulation limit.
	Constant Current	0x02	[4]	R	Red = Power supply is operating in constant current mode.
	Reserved	0x02	[3]	R	Reserved.
	Line Impedance	0x02	[2]	R	Red = Line impedance between VS2 and VS3 is above limit.
	Soft-Start Filter	0x02	[1]	R	Red = The Soft-Start Filter is in use
	External Flag	0x02	[0]	R	Red = The external flag pin (FLAGIN) is set.
4	Reserved	0x03	[7]	R	Reserved.
	Modulation	0x03	[6]	R	Red = Modulation is at either minimum or maximum limit.
	Address	0x03	[5]	R	Red = The ADDRESS resistor is not correct.
	Light Load Mode	0x03	[4]	R	Red = The system is in Light Load mode.
	Reserved	0x03	[3]	R	Reserved.
	ACSNS	0x03	[2]	R	Red = The ac sense timing or amplitude is not correct. The AC Sense comparator has not tripped for one switching cycle.
	CRC Fault	0x03	[1]	R	Red = The EEPROM contents downloaded are incorrect
	EEPROM Unlocked	0x03	[0]	R	Red = The EEPROM is unlocked.

Table 34. Referring to Figure 22.

No.	Name	REG	Bits	R/W	Description
5	I/P Voltage				This indicator displays the input voltage calculated by the GUI using the duty cycle, VS3 and the N1:N2 values
6	I/P Current	0x13	[15:4]	R	This value displays the current measured on the primary side. The CS1 ADC gives a value corresponding to the voltage on the CS1 pin, using the Rcs1 resistance value, the software calculates the current at that pin and then scales it using the N1:N2current transformer ratio
7	I/P Power				This indicator displays the input power which is calculated using I/P Voltage 1 and I/P Current 2
8	O/P Voltage	0x17	[15:4]	R	This value displays the voltage measured at the VS3 pin and scaled using the R1 and R2 values entered by the user.
9	O/P Current	0x18	[15:4]	R	This value displays the output current. The CS2 ADC gives a value corresponding to the voltage drop across the CS2 pins, using the Rsense resistance value, the software calculates the output current and is scaled using the CS2 Nominal Voltage Setting
10	O/P Power				This indicator displays the input power which is calculated using O/P Voltage and O/P Current 2
11	VS1	0x15	[15:4]	R	This value displays the voltage measured at the VS1 pin and scaled using the R1 and R2 values entered by the user.
12	VS2	0x16	[15:4]	R	This value displays the voltage measured at the VS2 pin and scaled using the R1 and R2 values entered by the user.
13	Temperature	0x1A	[15:4]	R	This value displays the temperature in degrees Celsius, which is converted from the voltage measured at the RTD pin.
14	Share Bus	0x1D	[7:0]	R	This indicator displays share bus voltage information. If the power supply is the master, this register will output zero.
15	Modulation Value	0x1E	[7:0]	R	This indicator displays the amount of modulation from 0% to 100% that is being placed on the modulating edges.
16	Slave / Master	0x1D	[7:0]	R	This indicator displays if the ADP1043A is in the Master Mode or Slave Mode.
17	Grey Lines				These grey lines represent the various threshold levels for the indicator it is on.
18	Get First Flag	0x10	[3:0]	R	This button gets the flag that was set first. Restarting the power supply resets this value. Pressing this button also resets the value.
19	1st	0x10	[3:0]	R	This indicator represents the first flag that was set.