ADP1046A LLC resonant converter with Synchronous Rectification

12V/600W

PRD1486

FEATURES

600W LLC resonant topology
Input voltage range: 360 V dc to 420 V dc
Output voltage: 12 V dc
Nominal output current: 50 A
7 PWM outputs including Auxiliary PWM
Burst mode control in soft-start state and light load mode
OrFET control
On-board tests for housekeeping functions
Graphical user interface (GUI) software
I2C serial interface to PC
Calibration and trimming

CAUTION

This evaluation board uses high voltages and currents. Extreme caution must be taken especially on the primary side, to ensure safety for the user. It is strongly advised to power down the evaluation board when not in use. A current limited power supply is recommended as input as no fuse is present on the board.

ADP1046A EVALUATION BOARD OVERVIEW

This evaluation board features the ADP1046A in a switching power supply application. With the evaluation board and software, the ADP1046A can be interfaced to any PC running Windows 2000/XP/Vista/NT/7 via the computer's USB port. The software allows control and monitoring of the ADP1046A internal registers. The board is set up for the ADP1046A to act as an isolated switching power supply with a rated load of 12V/50A from an input voltage ranging from a 360VDC to 420VDC.

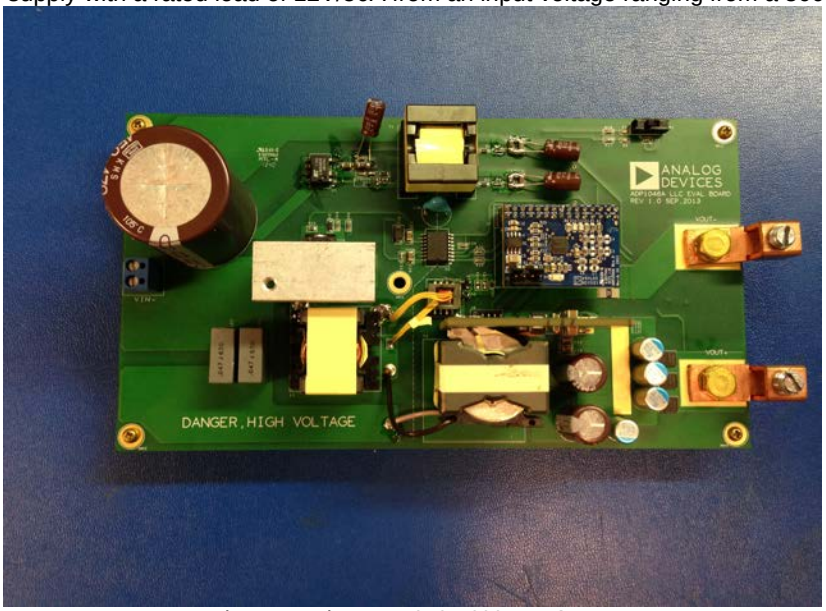

Figure 1 – The ADP1046A 600W LLC EVB

Rev. 1.0
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Tel: 781.329.4700 **www.analog.com**
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REVISION HISTORY

03/08/2014—Revision 1.0: SPM

BLOCK DIAGRAM

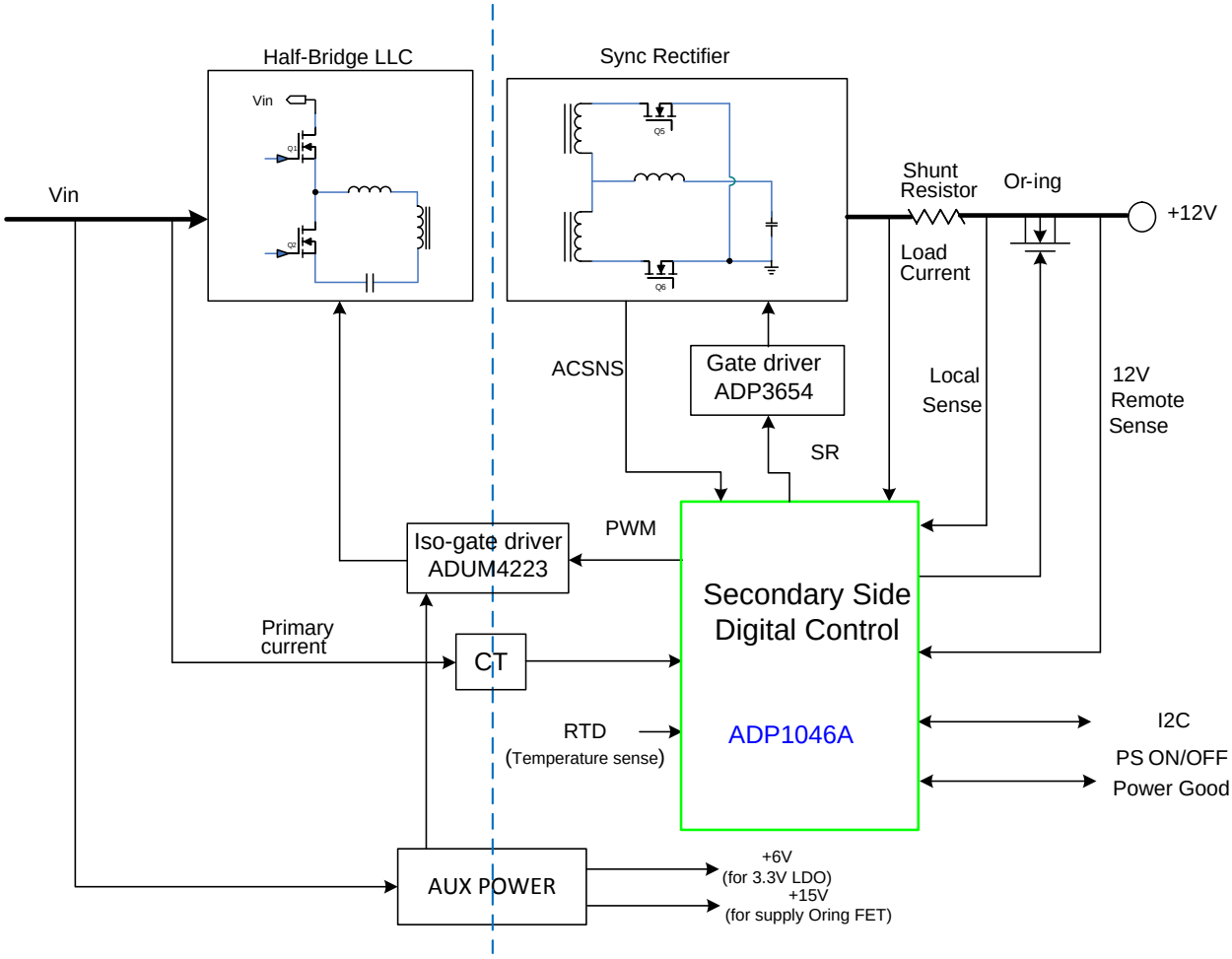

Figure.2 – The LLC EVB Block Diagram

BOARD SPECIFICATIONS

Specification	*MIN*	*TYP*	*MAX*	*Units*	*Notes*
V_{IN}	360	400	420	V	
V_{OUT}		12		V	
I_{OUT}	0.0	50	62.5	A	Need 11 CFM cooling
Overload current (OCP limit)			62.5	A	OCP delay time 10ms
Efficiency @ 50% loading		96.3%		%	Vin= 400V Iout=25A
Switching frequency	49	82	403.2	KHz	
Output Voltage Ripple		170		mV	At 50A load

Table 1 - Target Specifications

TOPOLOGY AND CIRCUIT DESCRIPTION

This application note consists of the ADP1046A in an isolated DC/DC switching power supply that is LLC resonant topology with synchronous rectification. The circuit is designed to provide a rated output load of 12V/50A from a nominal input voltage of 400VDC. The ADP1046A can provide functions such as the output voltage regulation, output over voltage protection, input and output current protection, primary cycle by cycle protection, and over temperature protection. Figure 2 shows the block diagram about the built reference design board. The auxiliary power supply starts up at 50VDC and provides power to the ADP1046A through a 3.3V LDO, the iCoupler isolation gate drivers, and the synchronous rectifier drivers.

The auxiliary power supply uses transformer (T1) and IC (U1) to generate a 12V rail on the primary side to power the iCoupler isolation devices (MOSFET drivers), a 15V rail on the secondary side to supply the OrFET and a 6V rail on the secondary side to power the *ADP3654 that is the gate driver IC for driving synchronous rectifier* and the ADP1046A using the 3.3V LDO. This auxiliary supply starts up when Vin higher than 50VDC.

The primary side consists of the input terminals (J5, J6), switches (Q5, Q6), the current sense transformer (T2) and the main transformer (T3) which include one resonant choke Lm. There are also resonant inductor (L1) and resonant capacitor (C26, C27) that the LLC resonant converter can be operated in zero voltage switching (ZVS) at all load conditions. The ADP1046A is situated on the secondary side and is powered via the auxiliary power supply or the USB connector via the LDO. The gate signal for the primary switches is generated by the ADP1046A through the iCouplers and fed into the MOSFET drivers (U2).

The secondary (isolated) side of the transformer consists of a center- tapped winding. The synchronous rectifier driver (U3) provides the drive signals for the switches (Q2~Q4, Q6~Q8) in SR board. The output inductor (L1) and output capacitor (C9~C19) act as a low pass filter for the output voltage. The output voltage is fed back to the ADP1046A using a voltage divider and has a nominal voltage of 1V which is differentially sensed. Output current measured using a sense resistor (R10~R13) which is also differentially sensed. To protect the synchronous rectifiers from exceeding the peak reverse voltage an RCD clamp is implemented (D2, D5, R3, R6, C1, C2).

The primary current is sensed through the CS1 pin with a small RC time constant (R24, C23) that act as a low pass filter to remove the high frequency noise on the signal. An additional RC can be placed, but the internal Σ-Δ ADC naturally averages the signal. The position of the current transformer is placed in series with the resonant inductor to avoid saturation. The full wave rectifier is used in secondary side in Half-Bridge LLC topology.

The SR gate signal is made by self-excited method. The secondary winding sense voltage (SR mosfet Vds) is divided and fed to ACSNS pin to produce the SR gate signals. The Oring FET control is also implemented in this reference board for the current sharing application.

Capacitor (C34) is a YCAP that reduces common mode noise from the transformer.

The 4 pin I2C communication connector also presents in the ADP1046A daughter card. This allows the PC software to communicate with the IC through the USB port of the PC. The user can easily change register settings on the ADP1046A, and monitor the status registers. It is recommended that the USB dongle be connected directly to the PC, not via external hub.

Switch (SW1) acts as a hardware PS_OFF switch. The polarity is configured using the GUI to be active high.

CONNECTORS

The following table lists the connectors on the board:

Connector	Evaluation Board Function
J5	DC Input positive terminal
J6	DC Input negative terminal
J1	Output voltage positive terminal
J2	Output voltage negative terminal
J3	Socket for ADP1046A daughter card
J1	I2C connector on the ADP1046A daughter card

Table 2 - Board connectors

The pin outs of the USB dongle are given below:

Figure 3 – I2C connector (pin1 on left)

Pin (left to right)	Function
1	5V
2	SCL
3	SDA
4	Ground

Table 3 - I2C connector pin out descriptions

SETTING FILES AND EEPROM

The ADP1046A communicates with the GUI software using the I2C bus.

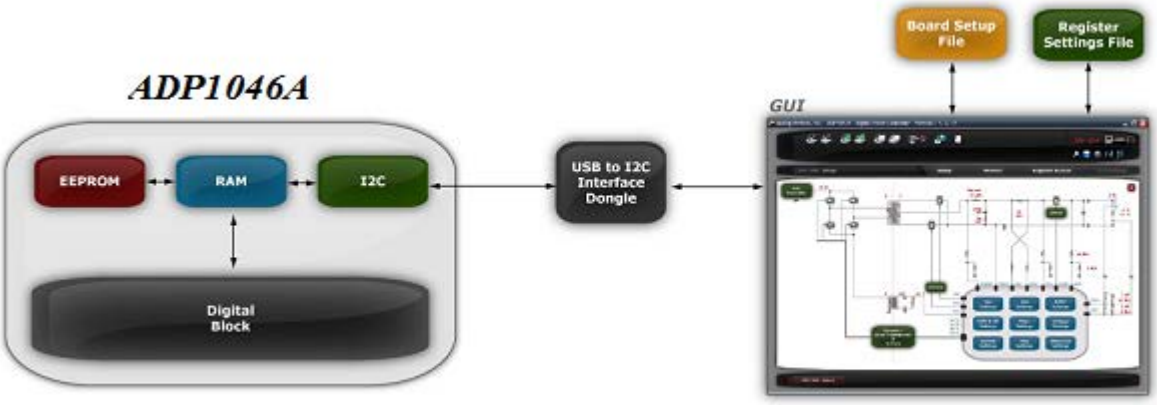

Figure 3 - ADP1046A and GUI interaction

The register settings (having extension .46r) and the board settings (having extension .46b) are two files that are associated with the ADP1046A software. The register settings file is contains information such as the over voltage and over current limits, softstart timing, PWM settings etc. that govern the functionality of the part. The ADP1046A stores all its settings in the EEPROM.

The EEPROM on the ADP1046A does not contain any information about the board, such as current sense resistor, output inductor and capacitor values. This information is stored in board setup file (extension .46b) and is necessary for the GUI to display the correct information in the 'Monitor' tab as well as 'Filter Settings' window. The entire status of the power supply such as the ORFET and synchronous rectifiers enable/disable, primary current, output voltage and current can be thus digitally monitored and controlled using software only. Always make sure that the correct board file has been loaded for the board currently in use.

Each ADP1046A chip has trim registers for the temperature, input current and the output voltage and current, and ACSNS. These can be configured during production and are not overwritten whenever a new register settings file is loaded. This is done in order to retain the trimming of all the ADCs for that corresponding environmental and circuit condition (component tolerances, thermal drift, etc.). A guided wizard called the 'Auto Trim' is started which trims the above mentioned quantities so that the measurement value matches the valued displayed in the GUI to allow ease of control through software.

BOARD EVALUATION

EQUIPMENT

- DC Power Supply (360-460V, 600W): Chroma
- Electronic Load (80V/600W): Chroma 6314
- Oscilloscope with differential probes: Lecroy 610Zi
- PC with ADP1046A GUI installed
- Precision Digital Voltmeters (Agilent 34410A) for measuring DC current and voltage

SETUP

NOTE: DO NOT CONNECT THE USB CABLE TO THE EVALUATION BOARD UNTIL THE SOFTWARE HAS FINISHED INSTALLING

1. Install the ADP1046A software by inserting the installation CD. The software setup will start automatically and a guided process will install the software as well as the USB drivers for communication of the GUI with the IC using the USB dongle.
2. Insert the daughter card in connector J3
3. Ensure that the PS_ON switch (SW1 on schematic) is turned to the OFF position. It is located on the bottom right half of the board.
4. Connect one end of USB dongle to the board and the other end to the board to the USB port on the PC using the “USB to I2C interface” dongle.
5. The software should report that the ADP1046A has been located on the board. Click “Finish” to proceed to the Main Software Interface Window. The serial number reported on the side of the checkbox indicates the USB dongle serial number. The windows also displays the device I2C address.

Figure 4 - ADP1046A address of 50h in the GUI

6. If the software does not detect the part it enters into simulation mode. Ensure that the connecter is connected to the daughter card. Click on ‘Scan for ADP1046A now’ icon (magnifying glass) located on the top right hand corner of the screen.

Figure 5 - “Scan for ADP1046A Now’ icon

7. Click on the “Load Board Settings” icon (fourth button from the left) and select the ADP1046A_FBPS_600W_xxxx**.46b** file. This file contains all the board information including values of shunt and voltage dividers. Note: All board setting files have an extension of .46b.

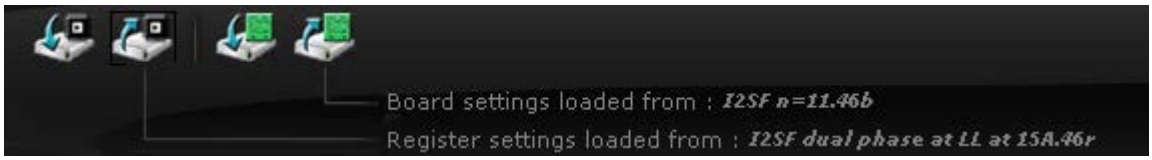

Figure 6 - Different icons on dashboard for loading and saving .46r and .46b files

8. The IC on the board comes preprogrammed and this step is optional. The original register configuration is stored in the ADP1046A_FBPS_600W_xxxx**.46r** register file (Note: All register files have an extension of .46r). The file can be loaded using the second icon from the left in Figure 7.

9. Connect a DC power source (400VDC nominal, current limit to ~2A) and an electronic load at the output set to 1 Ampere.

10. Ensure that the differential probes are used and the ground of the probes are isolated if oscilloscope measurements are made on the primary side of the transformer.

11. Click on the Dashboard settings (3rd icon in Figure and turn on the software PS_ON)

12. The board should now up and running, and ready for evaluation. The output should now read 12 VDC.

13. Click on the ‘MONITOR’ tab and then on the Flags and readings icon. This window provides a snapshot of the entire state of the PSU in a single user friendly window.

BOARD SETTINGS

The following screenshot displays the board settings.

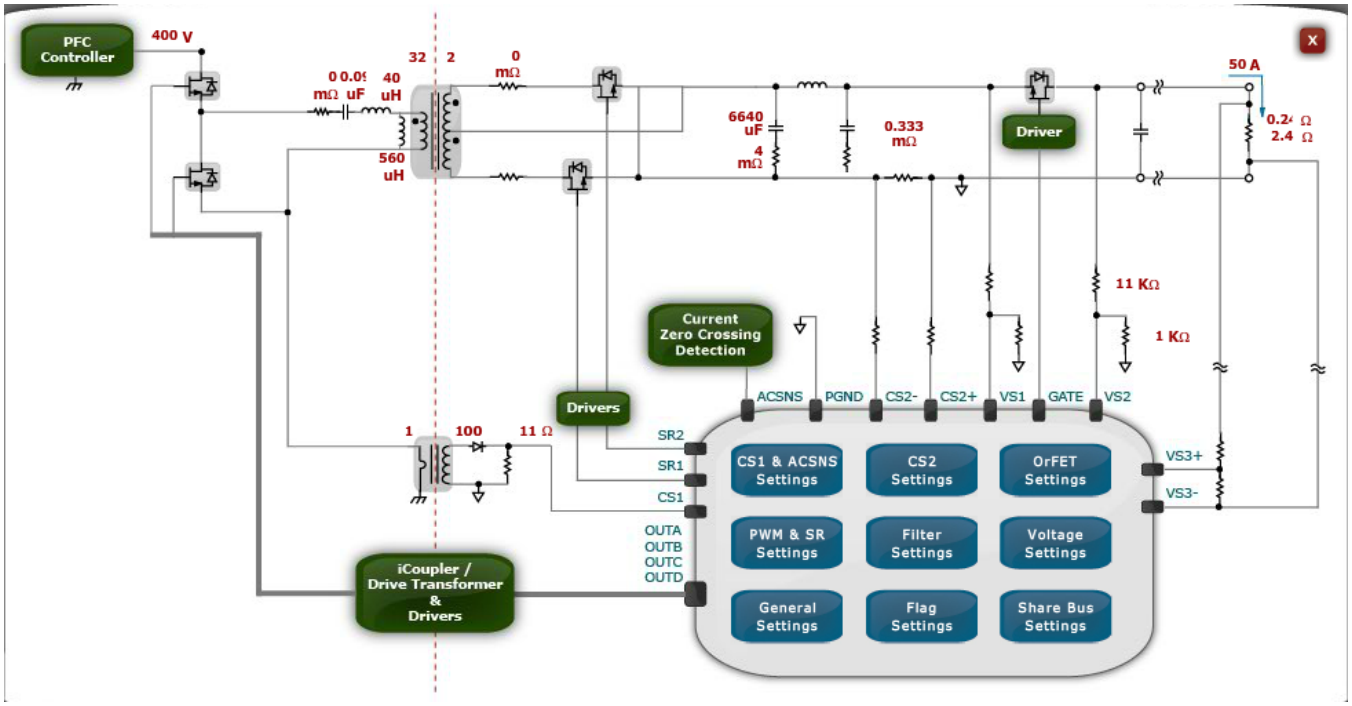

Figure 7 - Main Setup window of ADP1046A GUI

THEORY OF OPERATION DURING STARTUP

The following steps briefly describe the startup procedure of the ADP1046A and the power supply and the operation of the state machine for the preprogrammed set of registers that are included in the design kit.

1. The on board auxiliary power starts up at approximately 50VDC. This provides a drive voltage on the isolated side to an LDO (3.3V) that powers up the ADP1046A. After VDD (3.3V) is applied to the ADP1046A it takes approximately 20-50µs for VCORE to reach 2.5V. The digital core is now activated and the contents of the registers are downloaded in the EEPROM. The ADP1046A is now ready for operation.
2. PS_ON is applied. The power supply begins the programmed softstart ramp of 20ms (programmable).
3. Since the 'softstart from pre-charge' setting is active the output voltage is sensed before the softstart ramp begins. Depending upon the output voltage level of the effective softstart ramp is reduced by the proportional amount.
4. The PSU now is running in steady state. PGOOD1 turns on after the programmed debounce.
5. If a fault is activated during the soft-start or steady state, the corresponding flag will be set and the programmed action will be taken such as disable PSU and re-enable after 1 sec or 'Disable SR and OrFET, Disable OUTAUX' etc.

FLAGS SETTINGS CONFIGURATIONS

Basically when a flag is triggered, the ADP1046A state machine waits for a programmable debounce time before taking any action. The response to each flag can be programmed individually. The flags can be programmed in a single window by selecting the FLAG SETTINGS icon in the MONITOR tab in the GUI. This monitor window shows all the fault flags (if any) and the readings in one page. The 'Get First Flag' button determines the first flag that was set in case of a fault event.

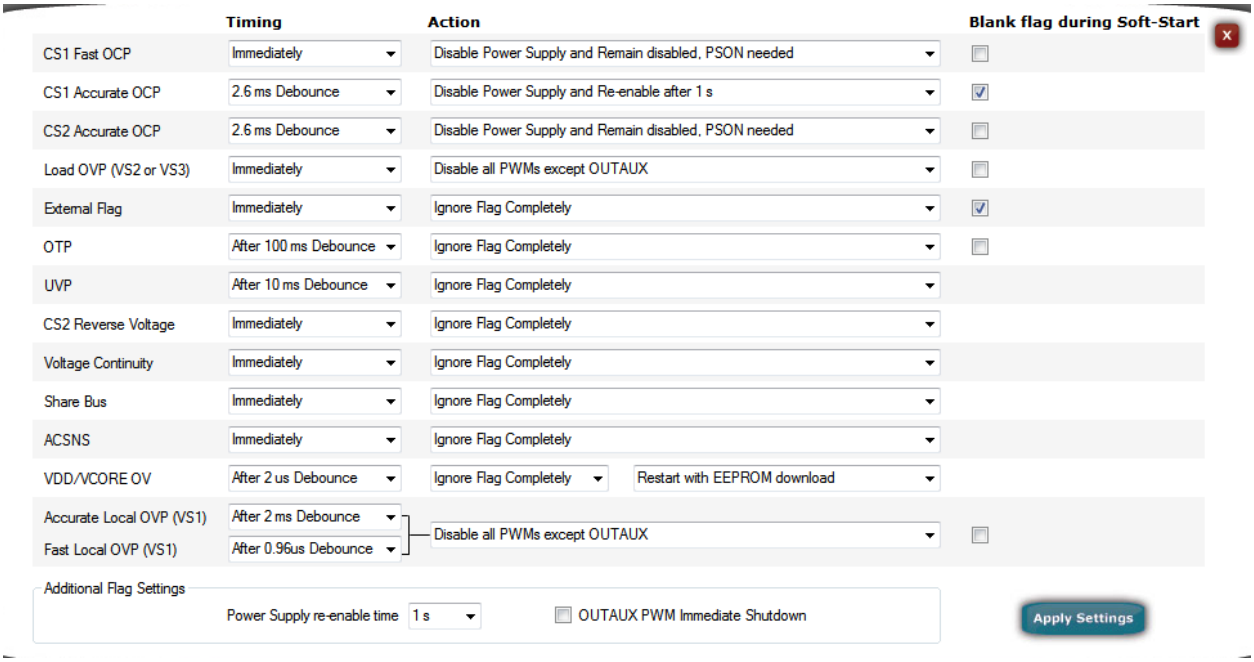

Figure 8 - Fault Configurations

PWM SETTINGS

The ADP1046A has a fully programmable PWM setup that controls 7 PWMs. Due to this flexibility the IC can function in several different topologies such as any isolated buck derived topology, push pull, flyback and also has the control law for resonant converters.

Each PWM edge can be moved in 10ns steps to achieve the appropriate deadtime needed and the maximum modulation limit sets the maximum duty cycle.

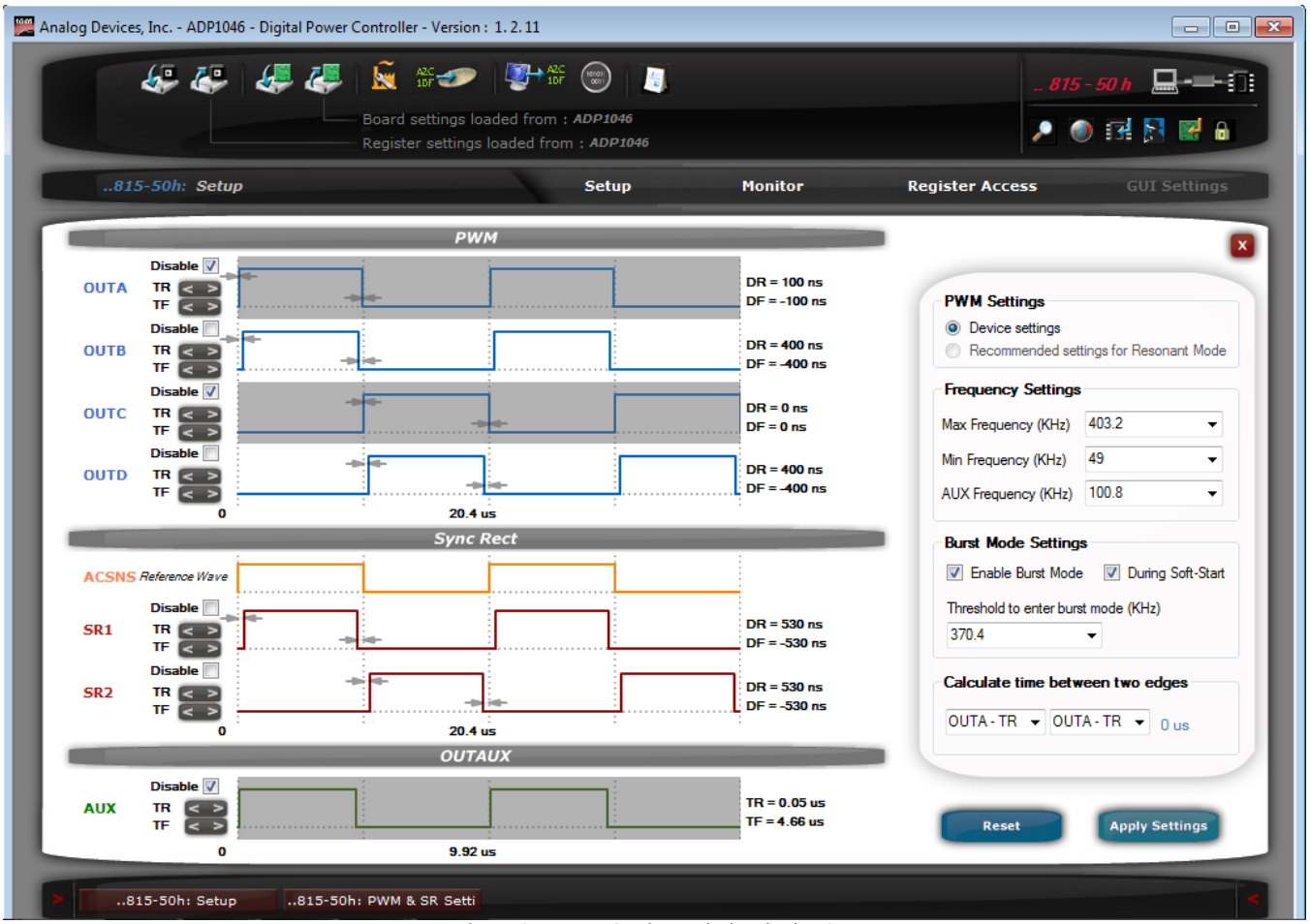

Figure 9 – PWM Settings window in the GUI

PWM	Switching element being controlled
OUTB,OUTD	Primary switch PWM configured for Half-Bridge LLC resonant topology
SR1-SR2	Synchronous rectifier PWMs
OUTAUX	N/A

Table 4 –PWMs and their corresponding switching element

BOARD EVALUATION AND TEST DATA

STARTUP

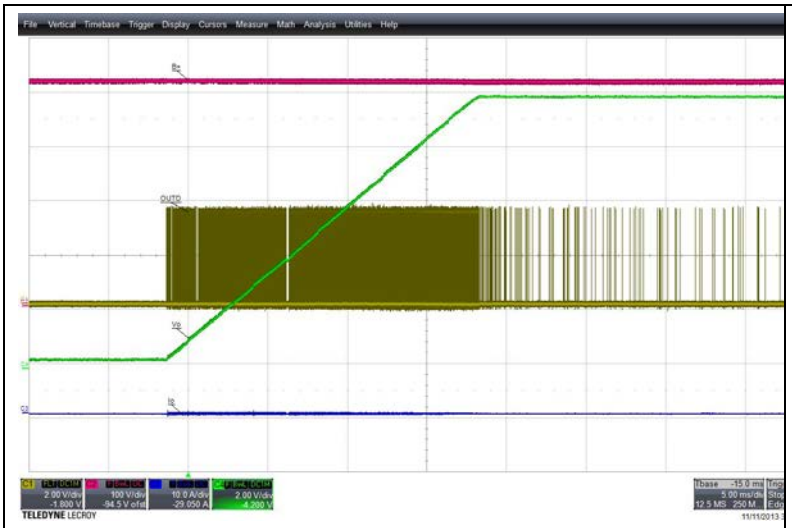

Figure 10 - Startup at 400VDC, 0W load(software PSON)
Green trace: Output voltage, 2V/div, 5ms/div
Yellow trace: PWM signal 2V/div, 5ms/div
Blue trace Load current, 10A/div, 5ms/div
Red trace: Input voltage, 100V/div, 5ms/div

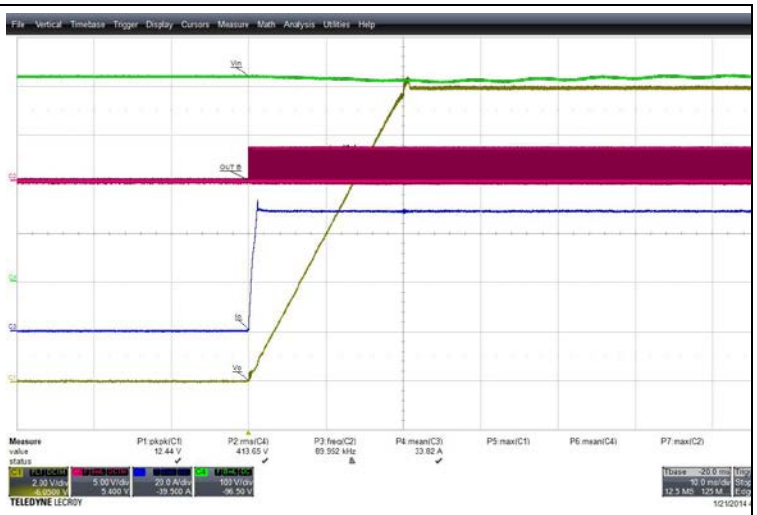

Figure 11 - Startup at 400VDC, 600W load(software PSON)
Green trace: Input voltage, 100V/div, 5ms/div
Yellow trace: Output voltage, 2V/div, 5ms/div
Blue trace Load current, 10A/div, 5ms/div
Red trace: PWM signal 2V/div, 5ms/div

OVERCURRENT PROTECTION

Figure 12 - 65A load(Action to shutdown after ~10ms)
Green trace: Output voltage, 2V/div, 5ms/div
Blue trace: Load current, 20A/div, 5ms/div

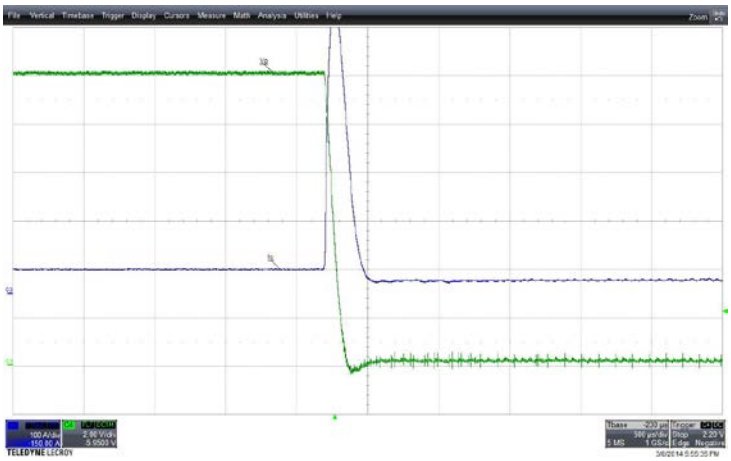

Figure 13 –Over current protection, 600Wto output shorted,
Green trace: Output voltage, 2V/div, 500us/div
Blue trace: Load current, 100A/div, 500us/div

LLC CONVERTER & SR PWM TIMING

Figure 14 –The PWM timing of LLC converter and SR @ Io=20A
Yellow Trace: OUTB
Red Trace: OUTD
Blue Trace: ACSNS
Green Trace: SR1

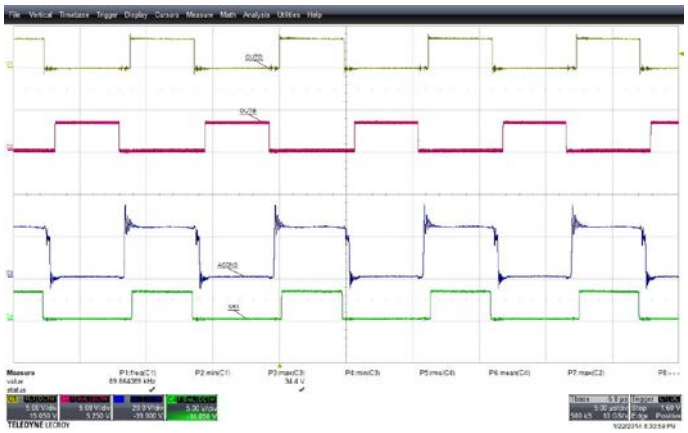

Figure 15 –The PWM timing of LLC converter and SR @ Io=50A
Yellow Trace: OUTB
Red Trace: OUTD
Blue Trace: ACSNS
Green Trace: SR1

SYNCHRONOUS RECTIFIER STRESS

Figure 16 – Synchronous rectifier MOSFET Peak reverse voltage at 600W load, 400VDC, 50V/div, 2us/div

OUTPUT VOLTAGE RIPPLE

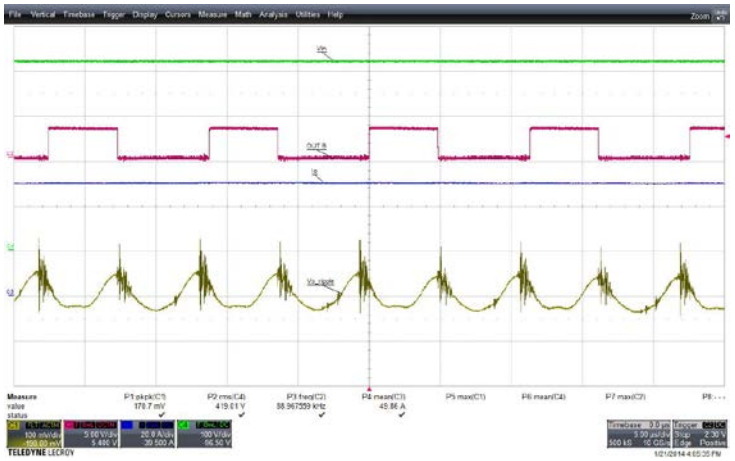

Figure 17 – Output voltage AC coupled 400VDC, 50A, 100mV/div, 5us/div..

TRANSIENT VOLTAGE AT 400VDC (NOMINAL INPUT VOLTAGE)

LOAD STEP OF 0-50%

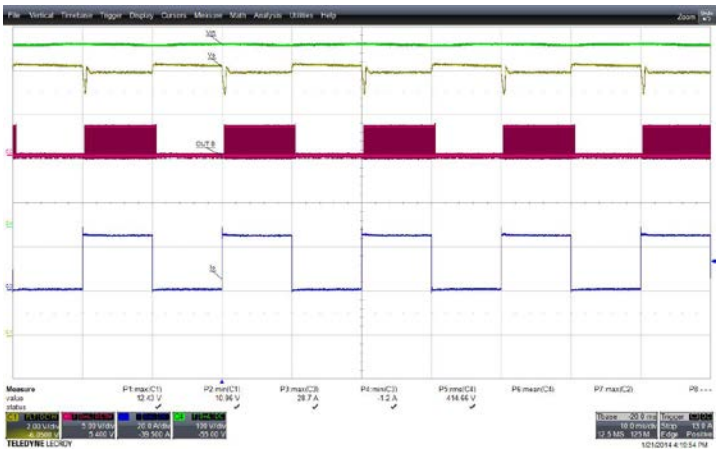

Figure 18 – Output voltage transient, 10ms/div
Yellow trace: output voltage, 2V/div 2A/div
Red Trace: OUTB (LLC gate signal)
Blue Trace: output current, 20A/div
Green trace :input voltage , 100V/div

LOAD STEP OF 50-100%

Figure 19 – Output voltage transient, 10ms/div
Yellow trace: output voltage, 2V/div 2A/div
Red Trace: OUTB (LLC gate signal)
Blue Trace: output current, 20A/div
Green trace :input voltage , 100V/div

ZVS WAVEFORMS FOR Q6

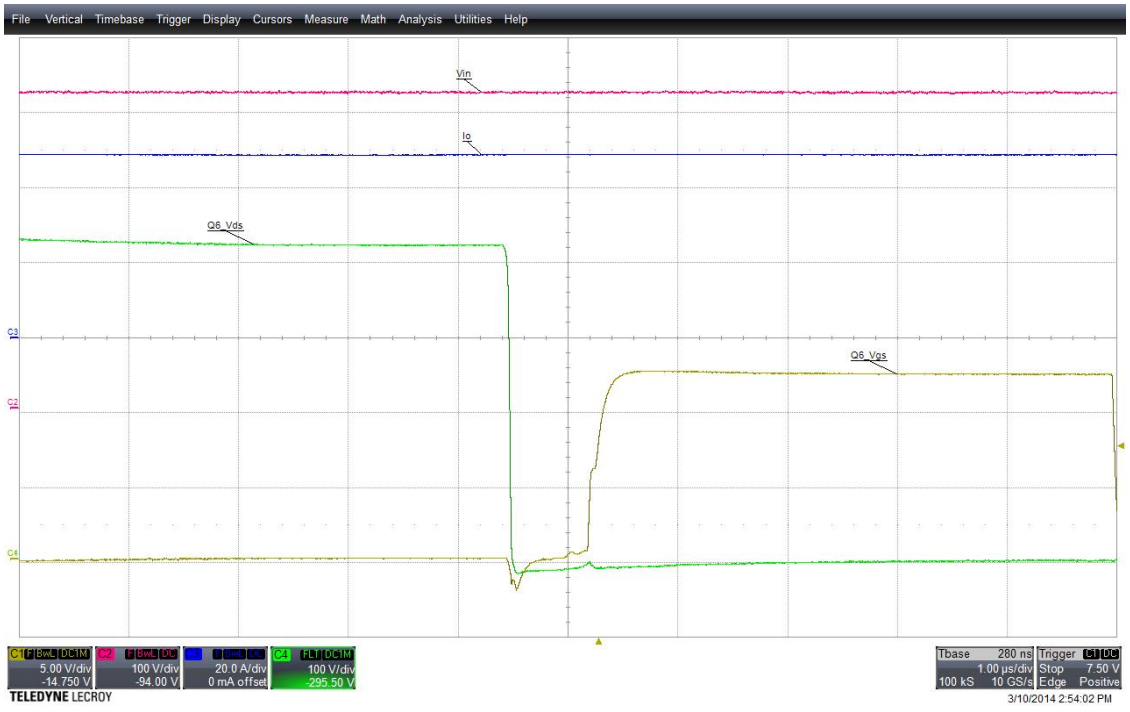

Figure 20–Resonant transition at 600W, 1us/div
Green trace: Q6 Vds
Yellow trace: Q6 Vgs
Blue Trace: Io, 10A/div
Red trace :input voltage , 100V/div

CLOSED LOOP FREQUENCY RESPONSE

A network analyzer (AP300) was used to test the bode plots of the system. A continuous noise signal of 150mV was injected across the entire frequency range across a 15Ω resistor in series with the output voltage divider using an isolation transformer. The operating condition was 400VDC input and a load condition of 600W with a soaking time of 45 minutes.

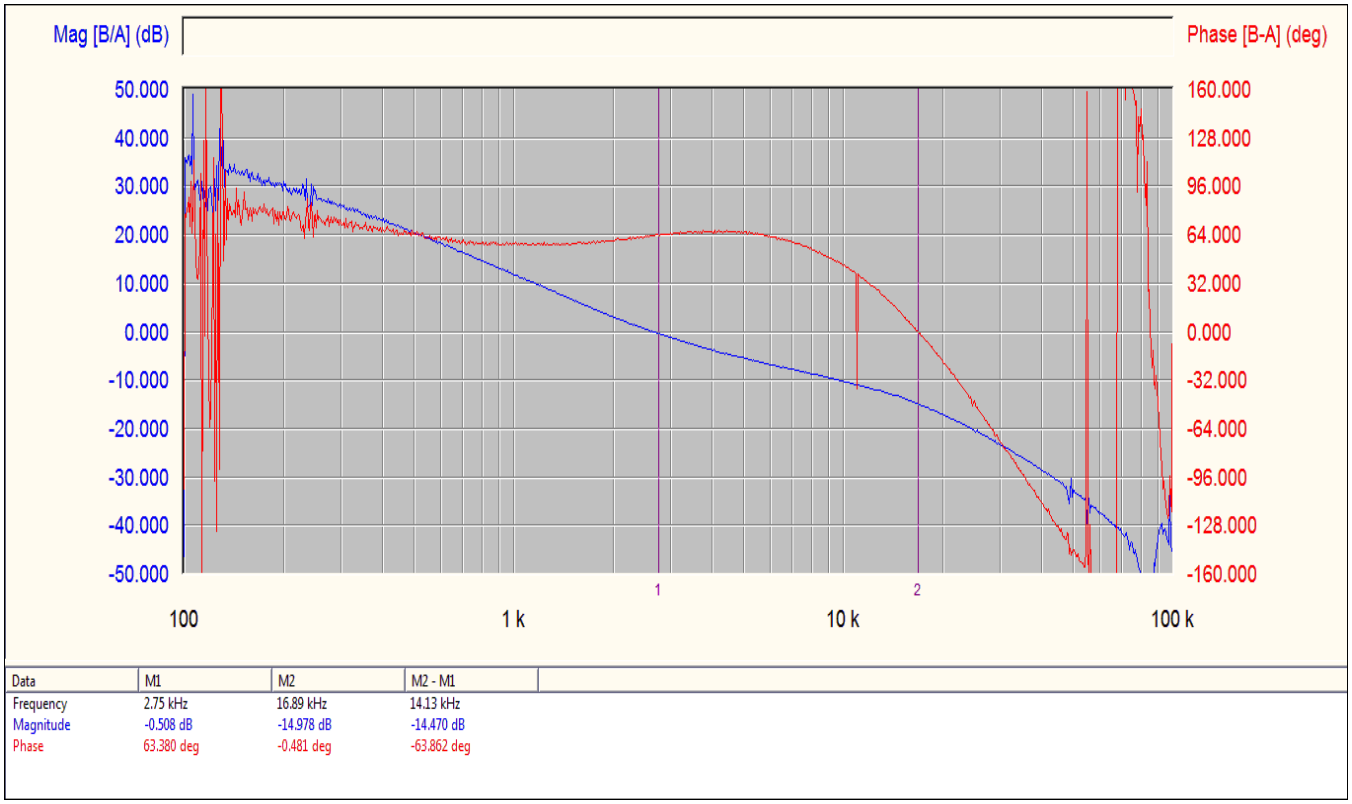

Figure 21 – Bode Plots, 400VDC input, 50A load,
Blue trace: Gain in dB
Red trace: Phase in degrees
Crossover frequency= 2.75KHz
Phase margin= 63.38°

EFFICIENCY

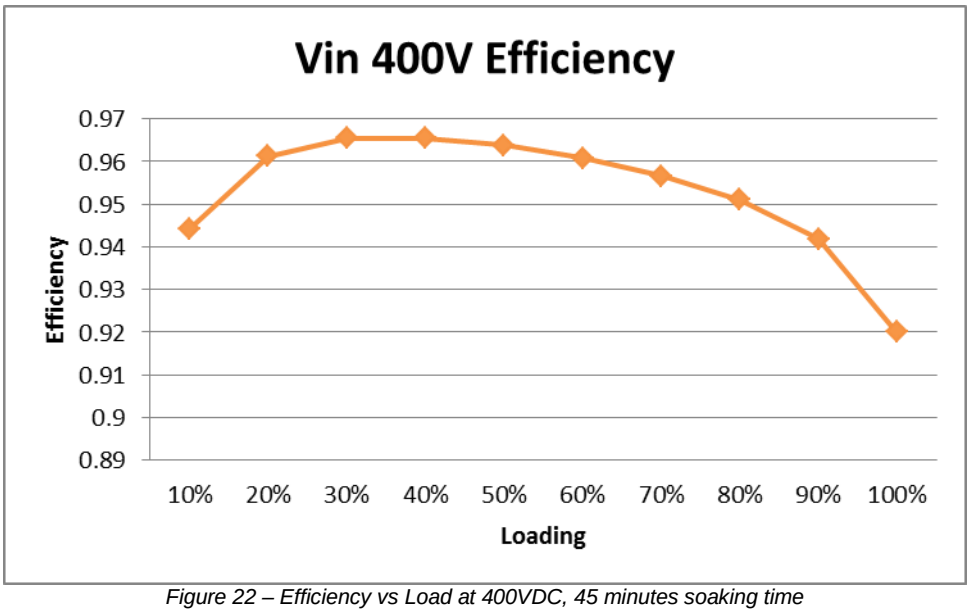

Figure 22 – Efficiency vs Load at 400VDC, 45 minutes soaking time

TRANSFORMER SPECIFICATION

PARAMETER	*MIN*	*TYP*	*MAX*	*UNITS*	*NOTES*
Core and Bobbin					PQ3230, Magnetics Inc R Material or equivalent
Primary inductance		590		µH	Pins 2 to pin 4

Table 5 - Transformer specifications

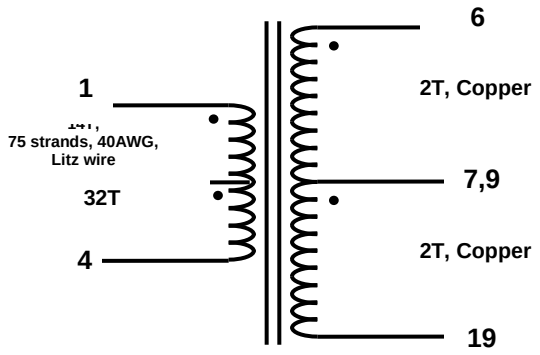

Figure 23 - Transformer electrical diagram

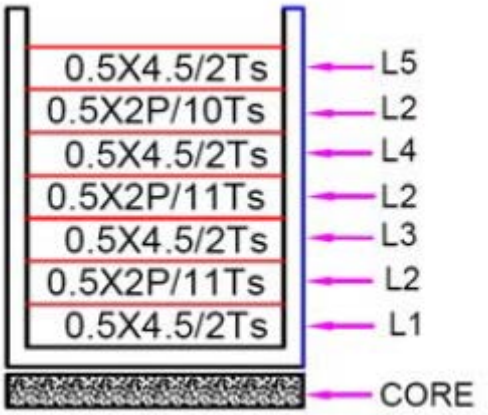

Figure 24 - Transformer construction diagram

APPENDIX I –SCHEMATICS (MAIN, AUX POWER, SR BOARD AND DAUGHTER CARD)

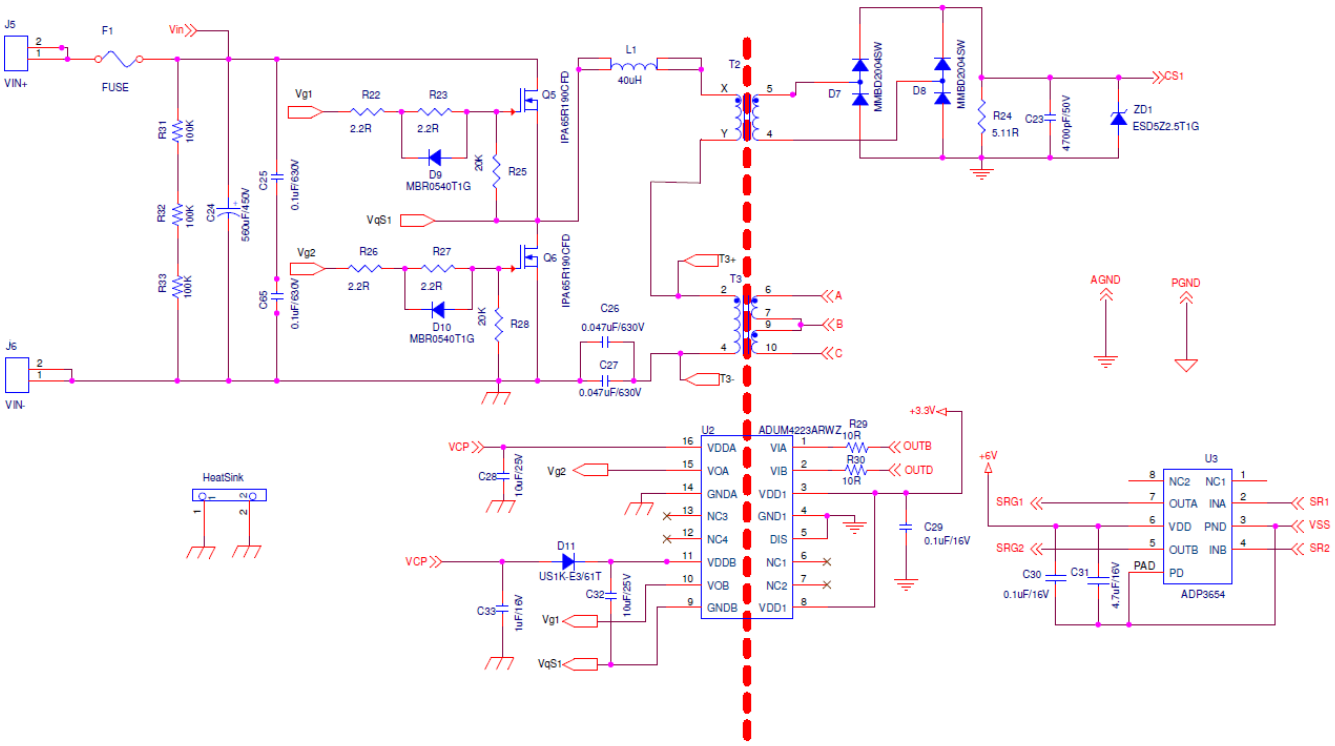

Figure 25 – Schematic – Half Bridge LLC

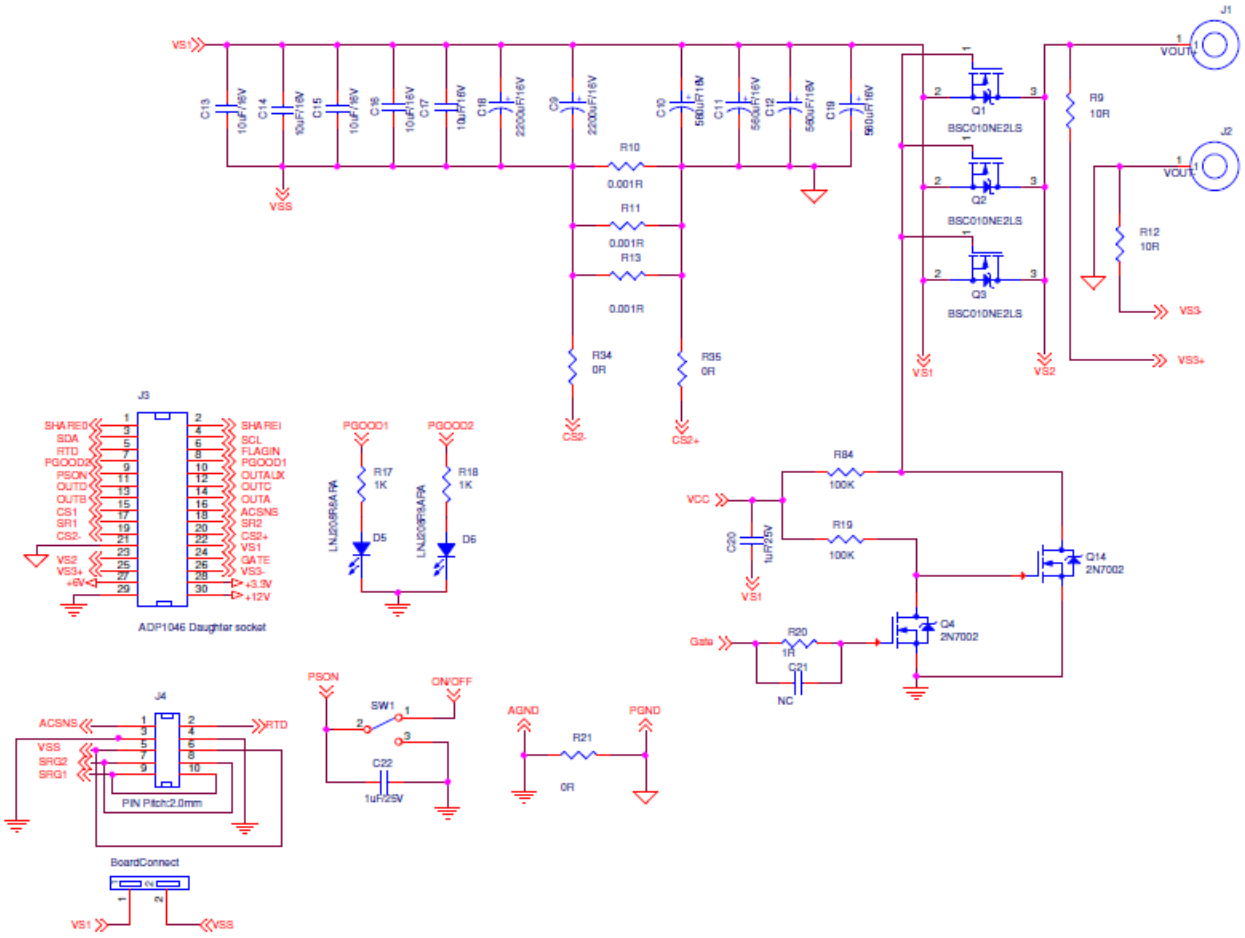

Figure 26 – Schematic – Current sense & Oring FET

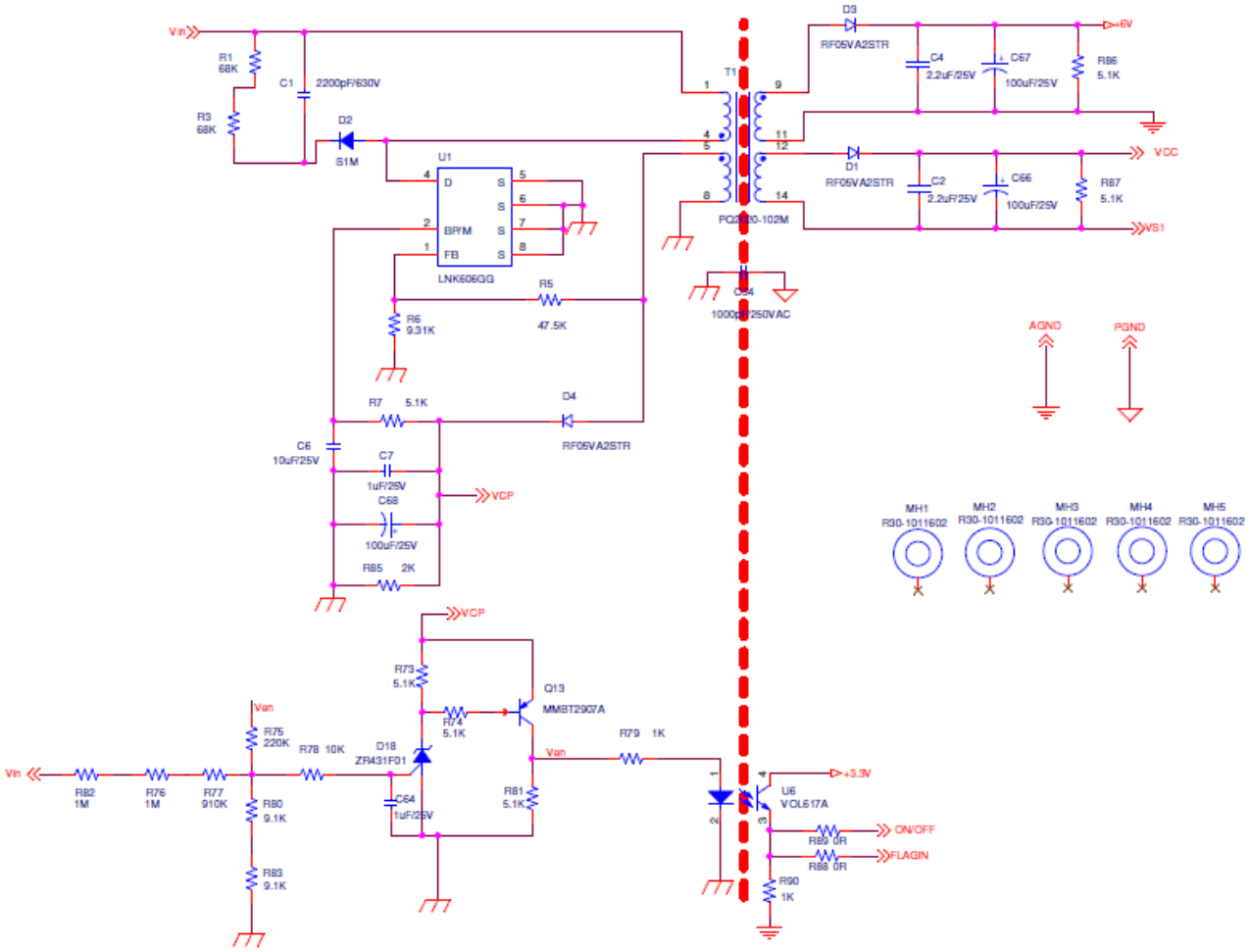

Figure 27 – Schematic – AUX power

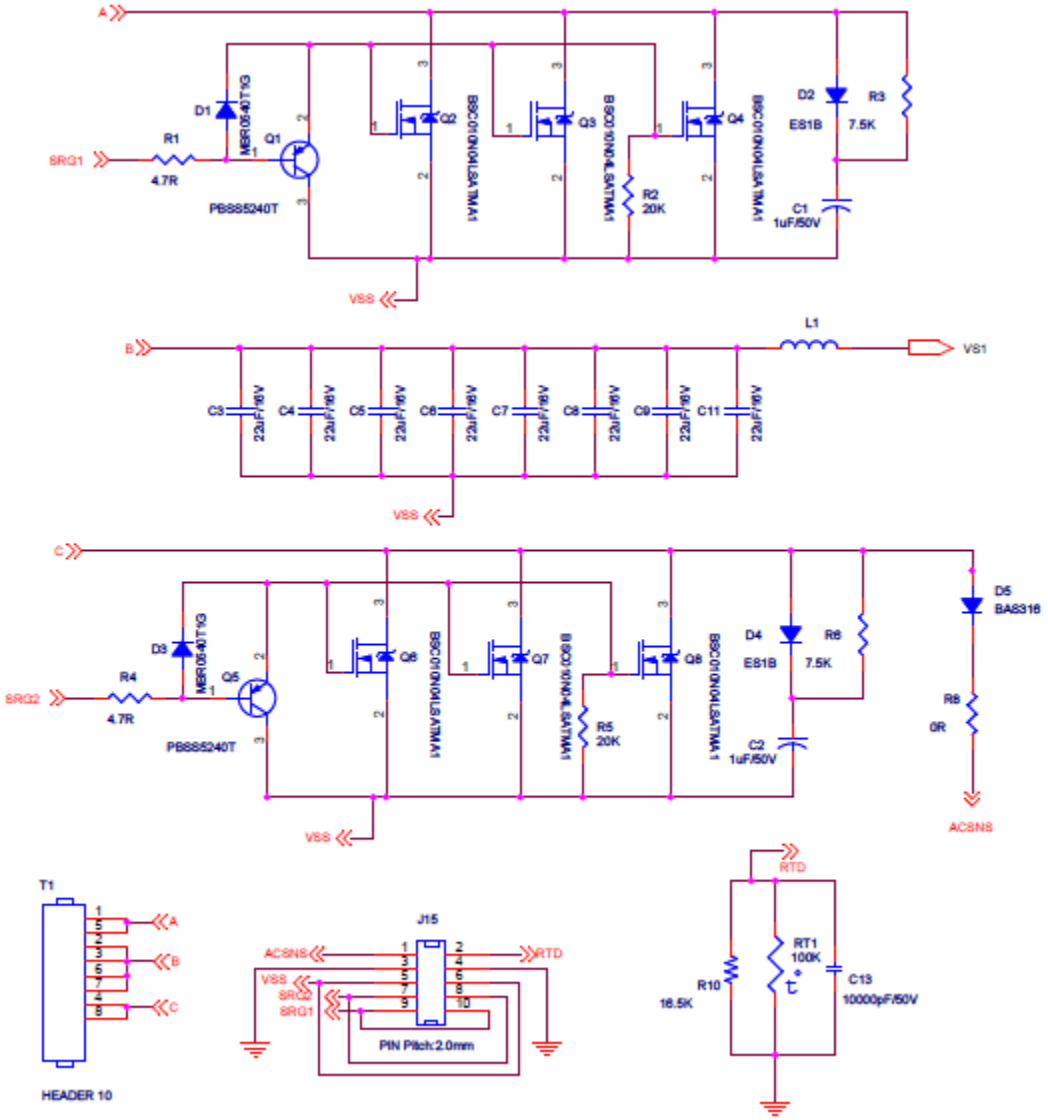

Figure 28 – Schematic – SR & Thermal sense

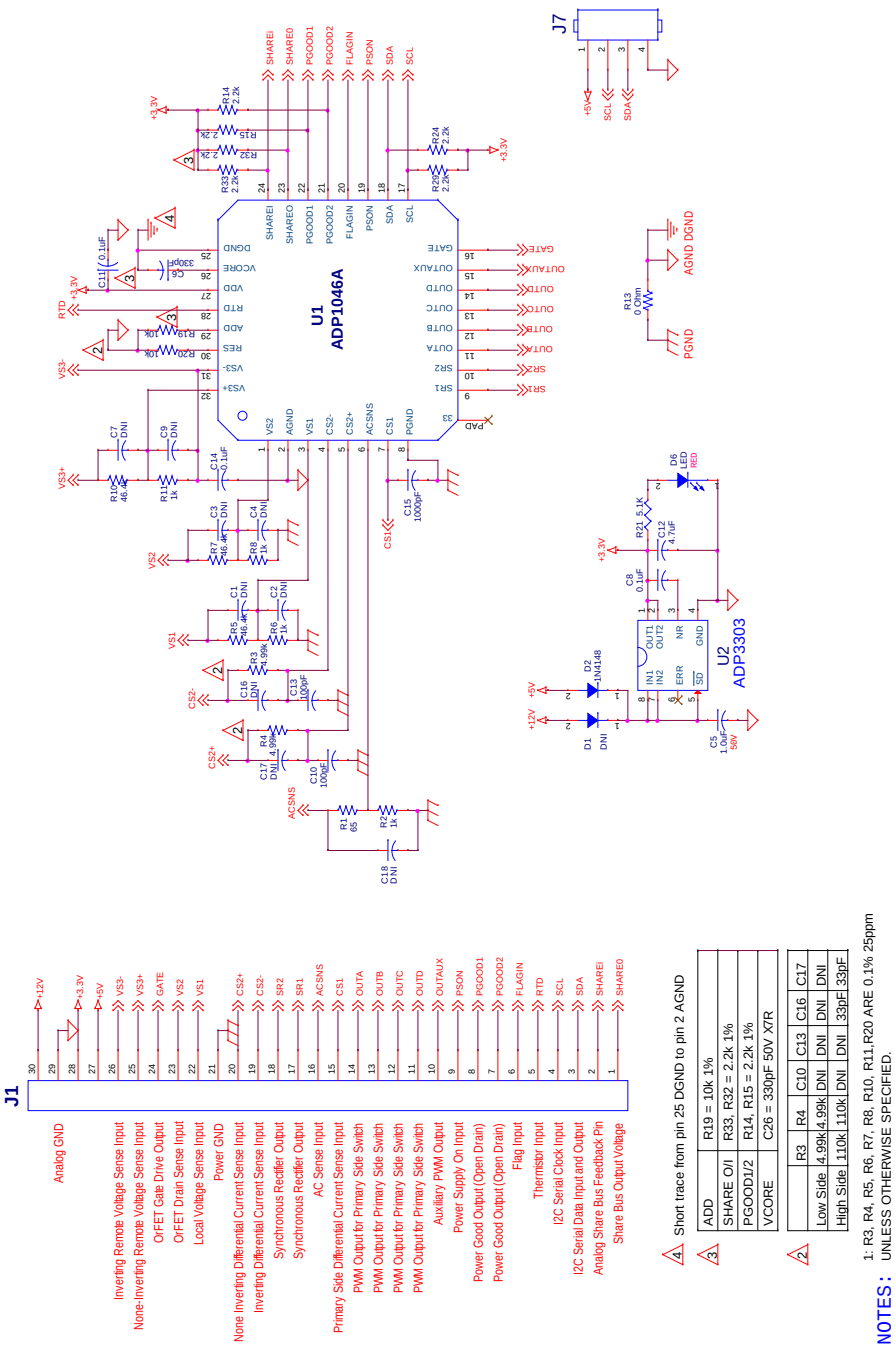

Figure 29 – Schematic – ADP1046A daughter card

APPENDIX IV – LAYOUT

Main Board

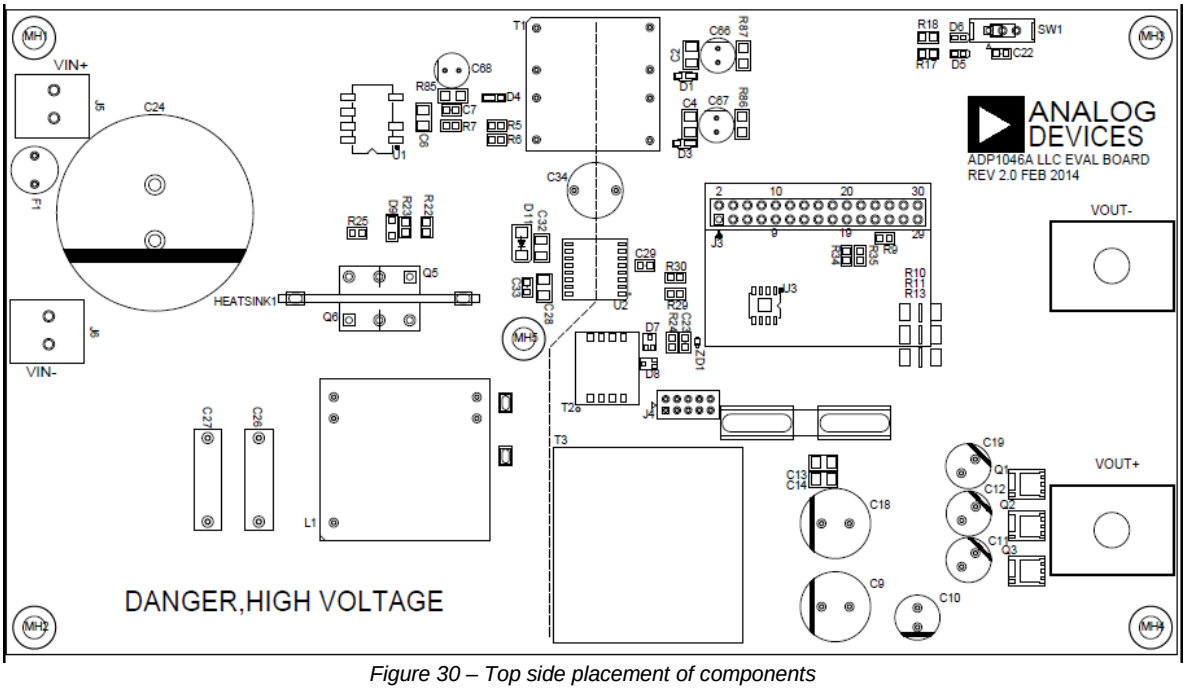

Figure 30 – Top side placement of components

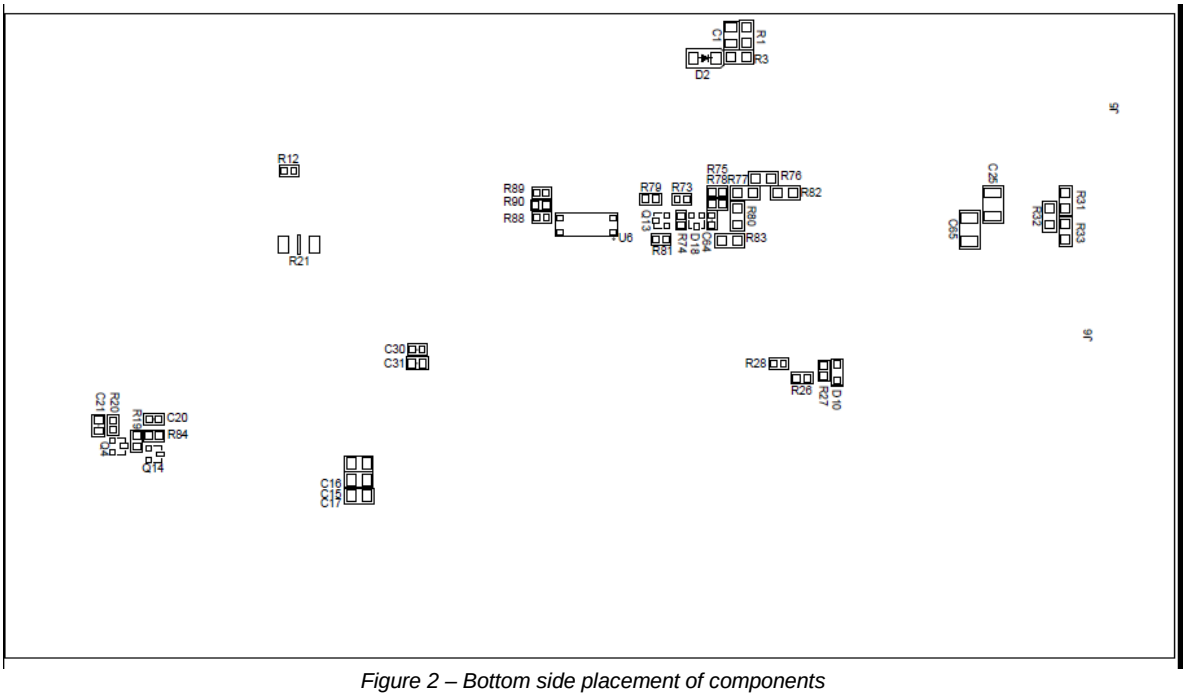

Figure 2 – Bottom side placement of components

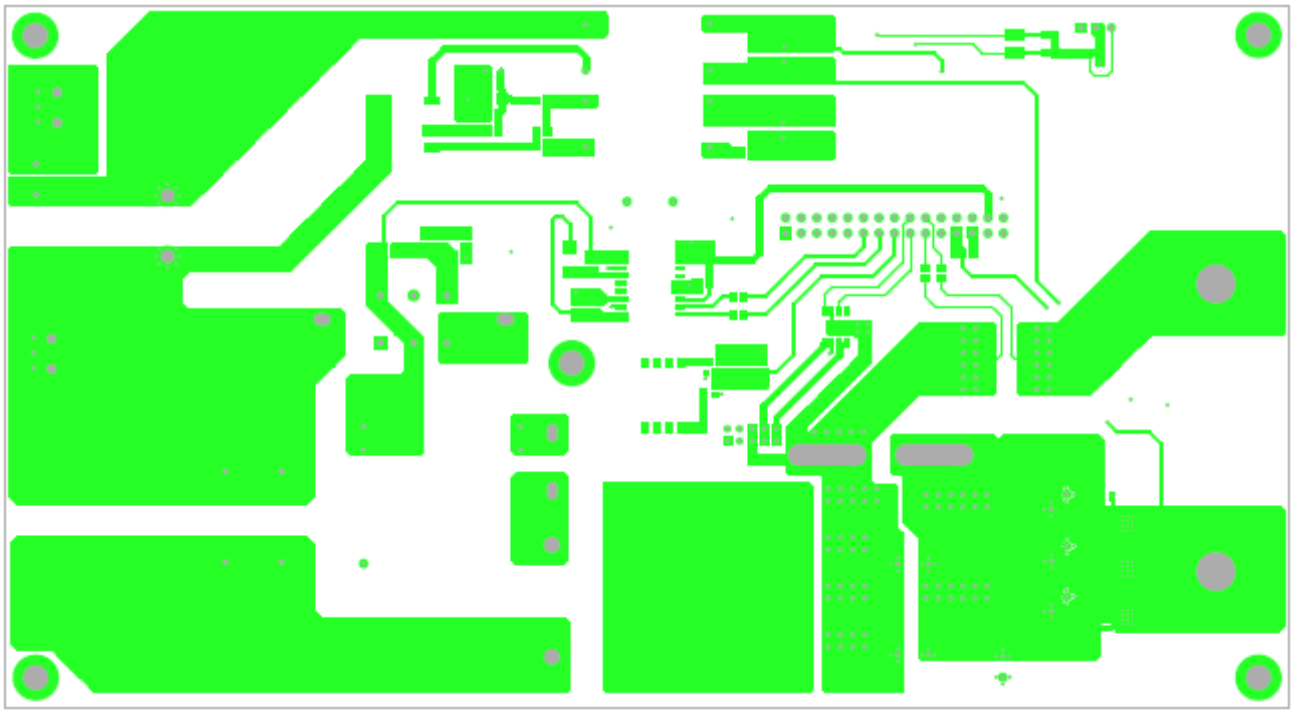

Figure 32 – Layout Layer 1

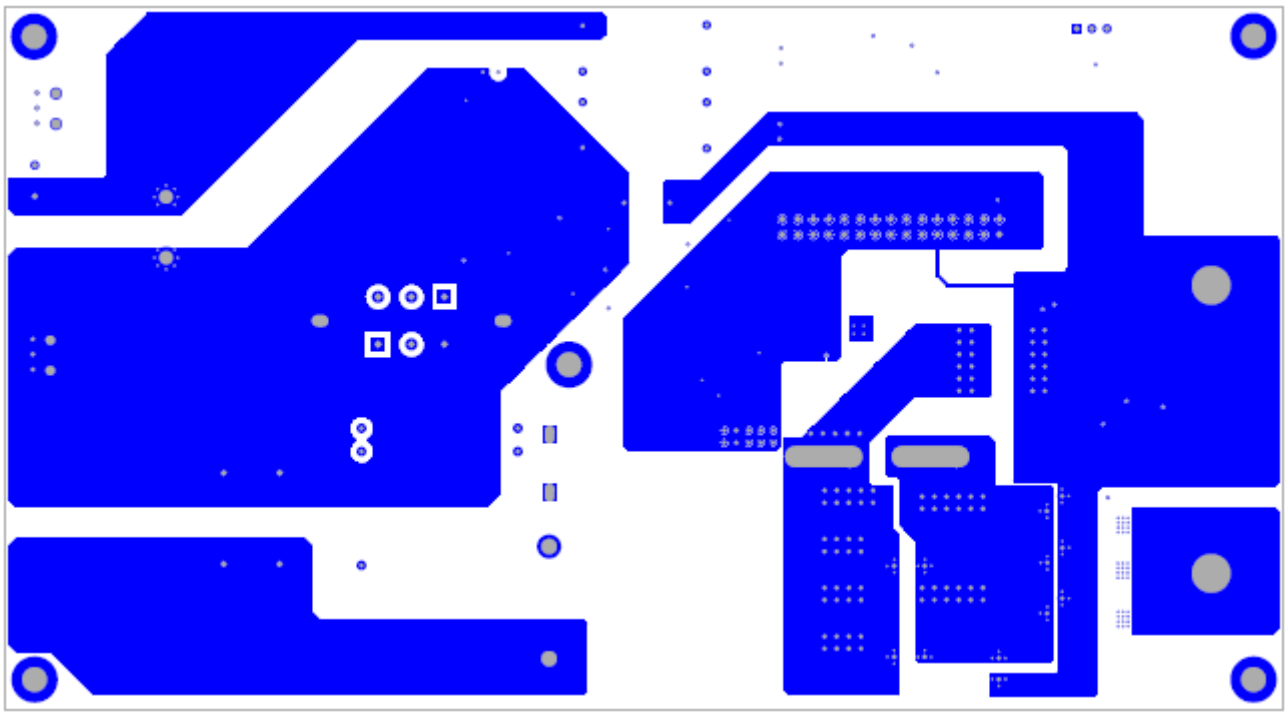

Figure 33 – Layout Layer 2

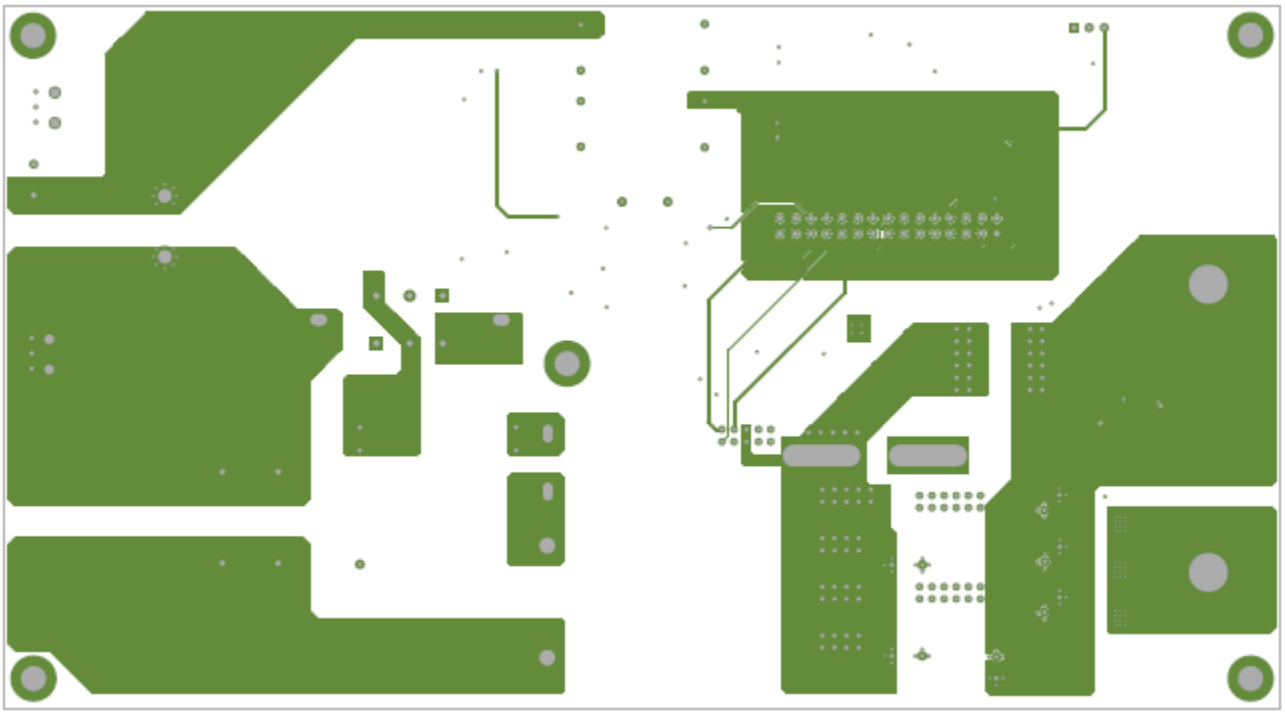

Figure 34 – Layout Layer 3

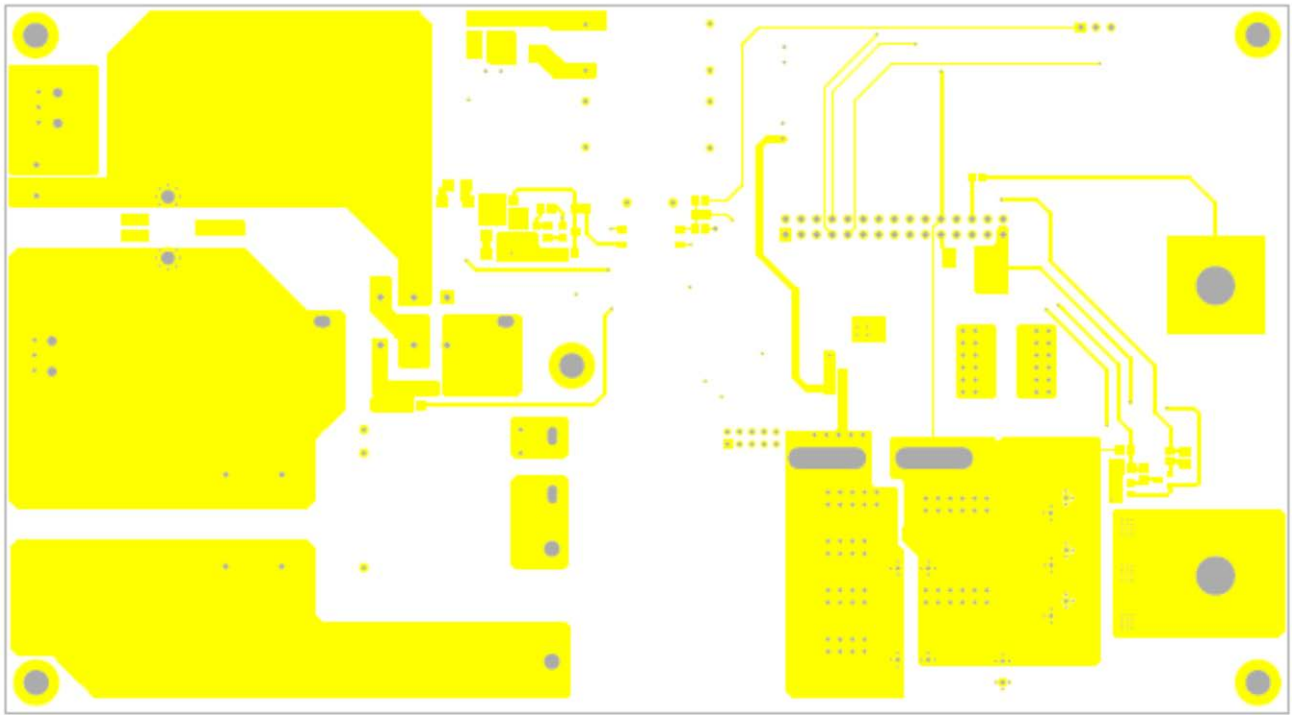

Figure 35 – Layout Layer 4

SR Board

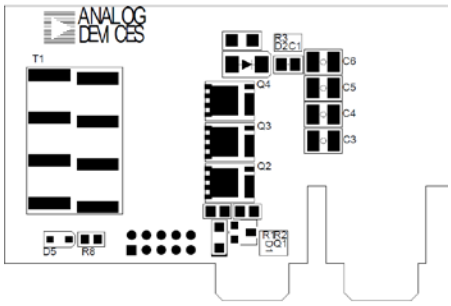

Figure 36 – Top side placement of components

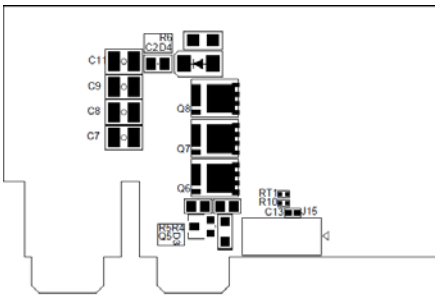

Figure 37 – Bottom side placement of components

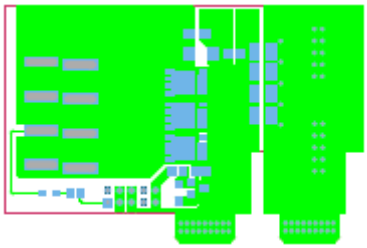

Figure 38 – Layout Layer 1

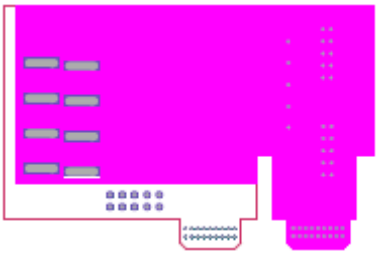

Figure 39 – Layout Layer 2

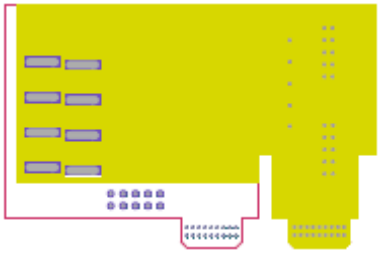

Figure 40 – Layout Layer 3

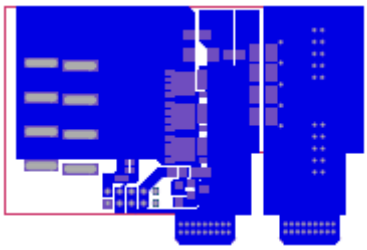

Figure 41 – Layout Layer 4

NOTES

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