AN-1336
APPLICATION NOTE

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Adaptive Dead Time in Full Bridge Phase Shifted Topology Using ADP1055

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INTRODUCTION

The growing demand for compact size in the power supply industry is forcing the size of power supply units (PSUs) to decrease. Apart from the power level itself, the size of the power supply is determined by the following two factors: the switching frequency and efficiency. The switching frequency determines the size of the magnetic components, which are the transformer and the inductor, while the efficiency determines the size of the switches (typically metal-oxide semiconductor field effect transistors [MOSFET]) and board size, which can be bulky.

The current industry standard for offline power supplies is in the 100 kHz to 200 kHz range. It is possible to increase the switching frequencies, however, there is a practical limit to this because as switching frequency increases, so do the switching losses. The use of bigger switching elements is typically not an option due to their cost constraints. In addition, the first three harmonics of switching frequency (f_{SW}) lie inside the electromagnetic interference (EMI) spectrum for the Comité Internationale Spécial des Perturbations Radioelectrotechnique (CISPR) or EN55022, which are hard to eradicate with the use of bulky EMI line filters that additionally add cost and size.

Using soft switching avoids these cost and size issues. Added efficiency, an overall quieter system (lower EMI), and smaller heat sinks are added bonuses. Soft switching eliminates the switching losses, which is the product of the voltage and current through a switch during the turn-on process. In power supply topologies with hard switching, the switching losses can be considerably high, especially when input voltages are large (385 V, which is typically the output of a power factor correction [PFC] front end).

Several topologies eliminate this loss such as active clamp and resonant mode topology. Another popular topology is full bridge phase shifted topology, which is more popular because the full bridge on the primary side is well suited for higher power as well as better utilization of the transformer core. With a digital controller such as the ADP1055, the hardware remains the same; however, with a slight modification in the pulse-width modulation (PWM) scheme, zero voltage switching (ZVS) is achieved.

This application note details the setup of the PWMs in the full bridge phase shifted topology and explores the adaptive dead time (ADT) feature of the IC that enables ZVS at light loads (see Figure 1).

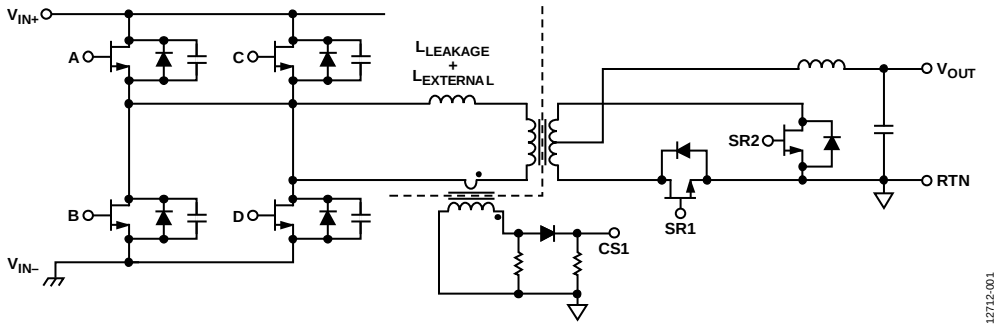

Figure 1. Full Bridge Phase Shifted Topology

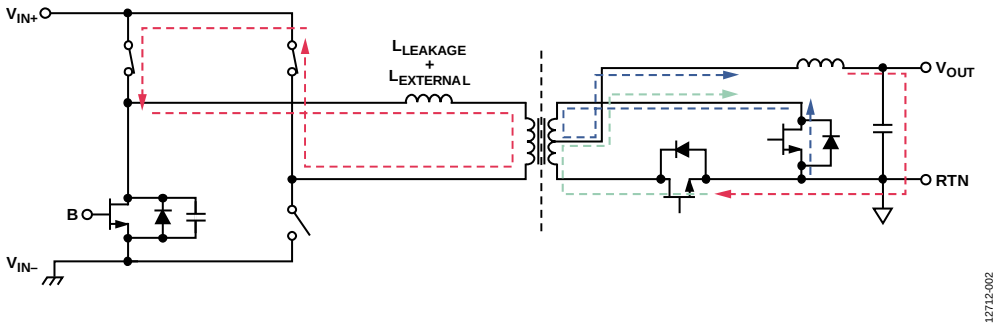

Figure 2. Active to Passive Stage That Shows ZVS of QC

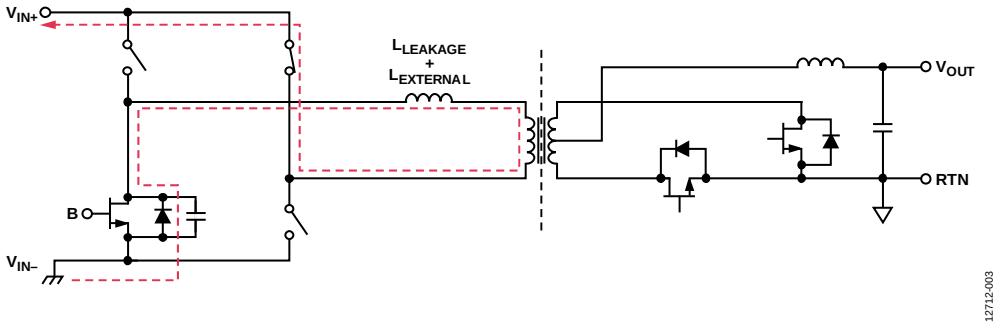

Figure 3. Passive to Active Stage That Shows ZVS of QB

ZVS EXPLANATION

Given a switching node that consists of an inductor, switch, and diode, when the MOSFET switch turns off the parasitic output, the parasitic capacitance (C_{OSS}) is charged because it is connected to the input voltage. During the next switching cycle, this energy is wasted because it is dumped into the FET. It also increases the turn-on switching losses equal to

$$P_{SW} = C_{OSS} \times V^2 \times f_{SW}$$

where:
P_{SW} is the switching loss.
V is the voltage across the switch.
f_{SW} is the switching frequency.

In the full bridge phase shifted topology, ZVS is achieved by discharging C_{OSS} using either the reflected current during the freewheeling portion of the inductor (active to passive stage) or the energy stored in the leakage plus the additional external inductor circulating the energy in C_{OSS} (passive to active stage), shown in Figure 2 and Figure 3. The respective FET turns on whenever the parasitic body diode conducts, at which point, the FET has a negligible voltage across it (one diode drop of 0.7 V compared to the nominal input voltage, typically 385 V).

The active to passive and passive to active transitions, and the typical PWM timing diagrams, are shown in Figure 2 and Figure 3.

PWM SETUP USING ADP1055

The ADP1055 is a digital controller with six PWMs. Each PWM can be independently set with relation to each other, and a combined modulation high limit (maximum duty cycle) can be set to all PWMs. There is also an independent set of PWMs for the synchronous rectifiers.

As shown in Figure 4, the extent of overlap of the OUTA and OUTD pair and the OUTB and OUTC pair provides an effective duty cycle for power transfer. The duty cycle is the logical AND of OUTA and OUTD for one leg of the H bridge. As the load decreases, each pair of PWMs move 180° out of phase with each other.

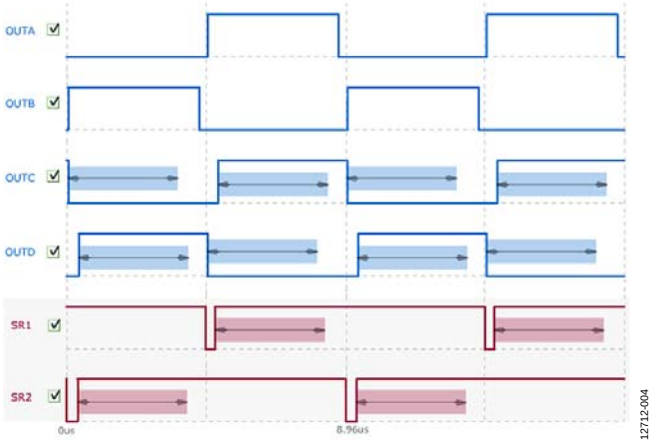

Figure 4. Typical PWM Setup for Full Bridge Phase Shifted Topology

Modulation for both the rising (t_{RISE}) and falling (t_{FALL}) edges is applied on OUTC and OUTD. The position of each edge (rising or falling) is programmed to ensure when there is no load that the PWM pairs are 180° out of phase with each other to prevent shoot-through. As the load increases, the t_{RISE} and t_{FALL} of OUTC and OUTD are phase shifted and move to the right.

ADAPTIVE DEAD TIME

The dead times for the fixed edges of OUTA and OUTB must be set up on the test bench. The modulated edges must be verified by design of the resonant tank frequency which is a function of leakage ($L_{LEAKAGE}$) plus the external inductor ($L_{EXTERNAL}$), transformer primary capacitance, switch parasitic capacitance, external capacitance in parallel with the switch, and peak primary current. This verification must be done at the minimum and the maximum input voltage and load.

Figure 5 and Figure 6 show the slew rate of the falling drain voltage across Switch Q_C at heavy and half loads (active to passive transition). The main criteria in designing the resonant tank is to ensure that the combined energy of $L_{LEAKAGE}$ and $L_{EXTERNAL}$ is greater than 8/3 C_{OSS} + C_{XFR}, where C_{XFR} is primary side winding capacitance. Due to higher peak currents at heavier loads, this constraint is achieved easily. However, this is not true at lighter loads, and ZVS is not achieved. To counter this effect, the ADP1055 employs the ADT feature. The ADT feature adds a programmable delay of 0 ns to 280 ns on either the rising or falling edge or both edges of any PWM. Figure 7 shows the ADT window in the graphical user interface (GUI).

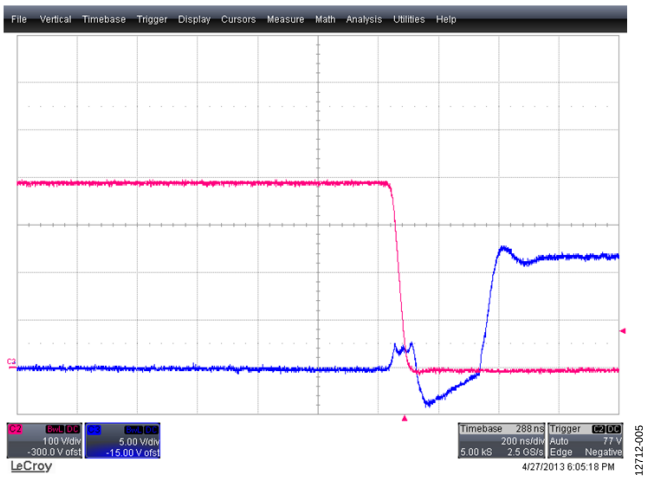

Figure 5. Slew Rate of the Falling Drain Voltage Across Switch Q_C at Heavy Load (Active to Passive Transition)
(Note That Red Trace Is the Voltage from Drain to Source on QC, VDS_QC, and Blue Trace Is the Voltage from Gate to Source on QC, VGS_QC.)

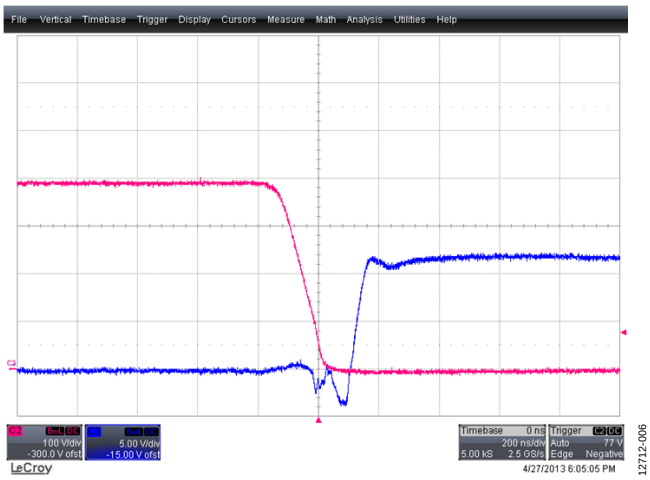

Figure 6. Slew Rate of the Falling Drain Voltage Across Switch Q_C at Half Load (Active to Passive Transition)
(Note That Red Trace Is the Voltage from Drain to Source on QC, VDS_QC, and Blue Trace Is the Voltage from Gate to Source on QC, VGS_QC.)

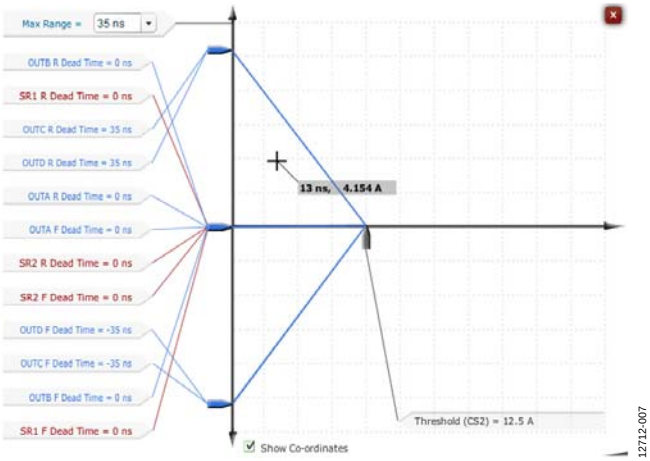

Figure 7. Adaptive Dead Time (ADT) Window

The x-axis in the ADT window is the sensed current either at the CS1 pin via a current transformer (see Figure 1) or the CS2 pin (load current). The y-axis is the programmable delay. Programming is set in the conventional drag and drop style of the Windows® environment. The **Show Co-ordinates** box displays the x and y coordinates of the graph. Figure 7 shows OUTC falling dead time is decreased by 35 ns (maximum setting of 280 ns) when the reported current is 0 A. As the current starts increasing, the dead time decreases linearly until it reaches 0 ns. All programmed delays move simultaneously in real time. The delay of the PWM edges is based on the primary current because it is a function of both the input voltage and the load. In addition, as previously mentioned, C_{OSS} is nonlinear and varies with input voltage. Therefore, the primary current is best suited for this adjustment. However, the ADP1055 also provides an option for ADT to be based off load current as the reference for the adjustment.

In addition to the maximum and minimum delay, two other programmable elements determine the operation of the ADT algorithm. The first element is the averaging period, which means that the decision to move the edges based on ADT is after each averaging period programmable to either 327 µs or 2.5 ms. The second element is the update rate. The PWMs move with a 5 ns step. This setting determines the number of switching cycles in which the total programmed and required delays add or subtract based on the CS1 reading. This is programmable in Register 0xFE1D, Bits[5:3]. If the contents are $111(2^2 + 2^1 + 2^0)$, the PWMs moves by 5 ns every $2^6 + 1$ switching cycle to add the total dead time.

Use the ADP1055 GUI to program this function because the graphical nature reduces programming complexity.

The design of the full bridge phase shifted topology mostly depends on factors such as duty cycle loss (due to ZVS transition and current commutation), though there are other pertinent factors. It is an interesting dynamic to note that if the initial condition of the current in the resonant inductor is high, that is, a high output load, the ZVS transition time is less than when compared to the time at a lower load condition. See Figure 8 for additional details. The worst case ZVS time is $T_{RES}/4$, where T_{RES} is the resonant period determined by the switch node capacitance (also includes transformer primary winding capacitance) and resonant inductance (also includes leakage inductance of the transformer).

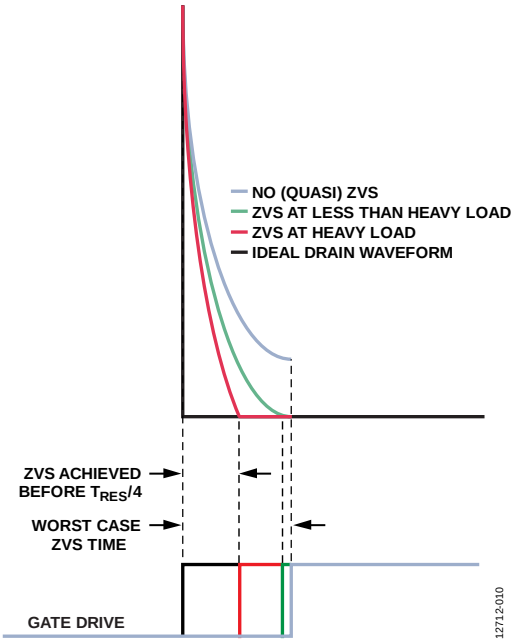

Figure 8. ZVS Transition at Various Loads

SATISFYING ZVS USING ADAPTIVE DEAD TIME

There are several modes of operation in the full bridge phase shifted converter. In this example, the converter powered by the output PFC converter has an output of 385 V dc. The phase shifted converter has an output rating of 48 V, 600 W with a resonant inductor of 33 µH and a MOSFET output capacitance of 594 pF. The resonant frequency is 1.136 kHz, and the worst case ZVS time for the passive to active transition is 220 ns. The following formulae provide the important transition times of the converter:

$$t_{PASSIVE\ TO\ ACTIVE} = \frac{1}{2 \times \pi \times \sqrt{L_{RESONANT} \times (2 \times C_{OSS})}}$$

$$t_{ACTIVE\ TO\ PASSIVE} = VIN \times 2 \times \frac{C_{OSS}}{N1/N2 \times I_{LOAD}}$$

$$t_{COMMUTATION} = 2 \times \frac{N1}{N2} \times \frac{I_{LOAD} \times L_{RESONANT}}{V_{IN}}$$

$$t_{DRIVER\ PROP\ DELAY} = 0\,\text{ns}(\text{or assume constant})$$

$$t_{EFFECTIVE\ DUTY\ CYCLE} = \frac{T_{SW}}{2} - [t_{PASSIVE\ TO\ ACTIVE} + t_{ACTIVE\ TO\ PASSIVE} + t_{COMMUTATION} + t_{DRIVER\ PROP\ DELAY}]$$

where:
T_{SW} is the switching period.
$L_{RESONANT}$ is the sum of leakage inductance and any external inductance in Figure 1.
N1 and *N2* are the turns of the transformer.

Figure 9, Figure 10, and Figure 11 show the passive to active ZVS transitions at heavy load, half load, and light load.

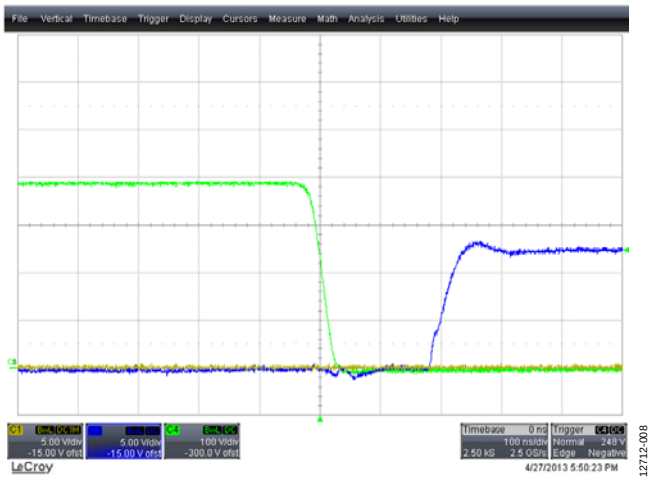

Figure 9. ZVS Transition at Heavy Load (Passive to Active) (Note That Green Trace Is the Voltage from Drain to Source on QB, VDS_QB, and Blue Trace Is the Voltage from Gate to Source on QB, VGS_QB.)

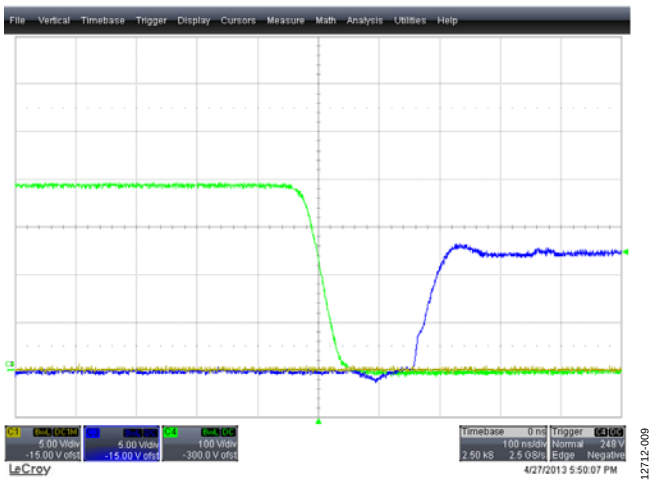

Figure 10. ZVS Transition at Half Load (Passive to Active)
(Note That Green Trace Is the Voltage from Drain to Source on QB, VDS_QB, and Blue Trace Is the Voltage from Gate to Source on QB, VGS_QB.)

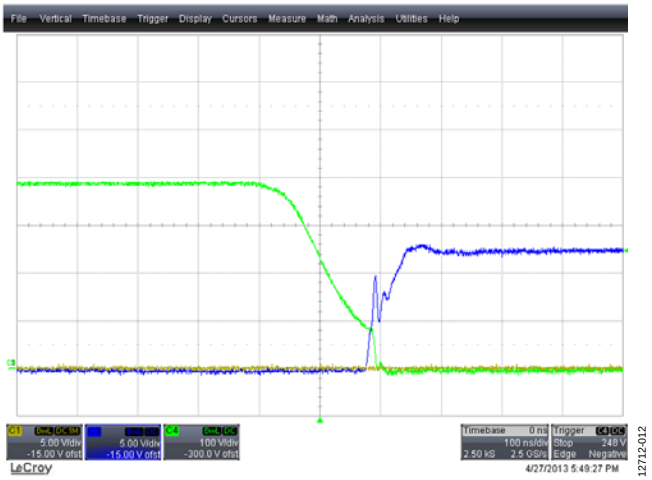

Figure 11. ZVS Transition at Light Load (Passive to Active)
(Note That Green Trace Is the Voltage from Drain to Source on QB, VDS_QB, and Blue Trace Is the Voltage from Gate to Source on QB, VGS_QB.)

Figure 12 shows the required dead times to achieve ZVS in the worst case condition (passive to active transition) based on an input range of 340 V to 385 V. Beyond a certain minimum load condition, ZVS is not achieved. The worst case dead time is approximated by a 1/x function multiplied by a gain factor where x is the load current. For a load current lower than this, add a constant dead time that is equal to a quarter of the resonant period ($T_{RES}/4$). This addition of dead time allows the primary switch to turn on at quasi ZVS when the minimum voltage is present across the switch, as is shown in Figure 11. Any further delay causes the resonance to flip in polarity (see Figure 13).

Figure 12 and Figure 14 show the theoretical deadtime for the passive to active and active to passive transition from the equations previously mentioned as compared to the approximation function 1/x, which can be used in the adaptive dead time feature.

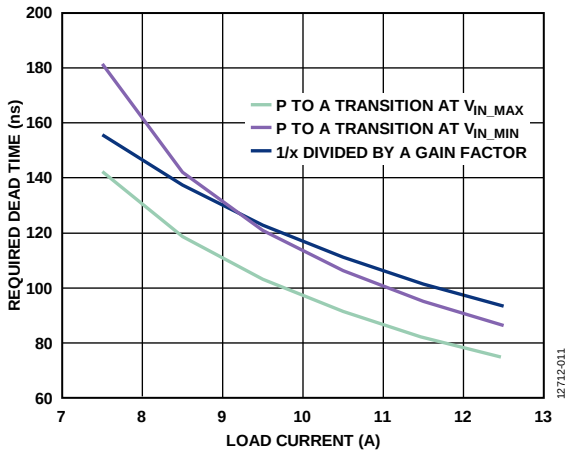

Figure 12. ZVS Transition Time During Passive to Active (P to A) Transition Based on Load Current

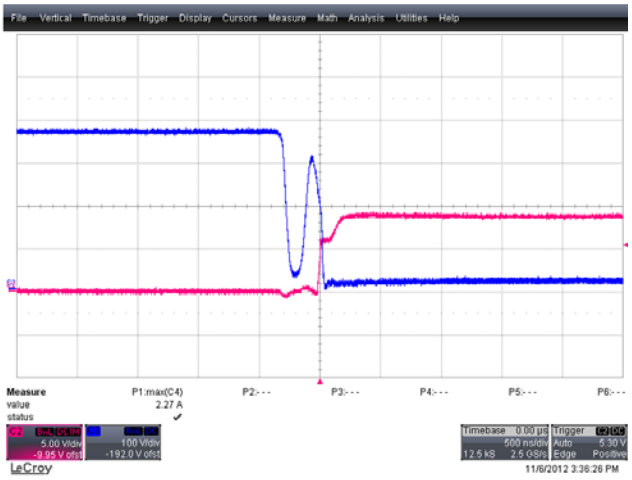

Figure 13. Nonoptimized ZVS Transition Time (Note That the Blue Trace Is the Switch Drain Voltage and the Red Trace Is the Gate Drive.)

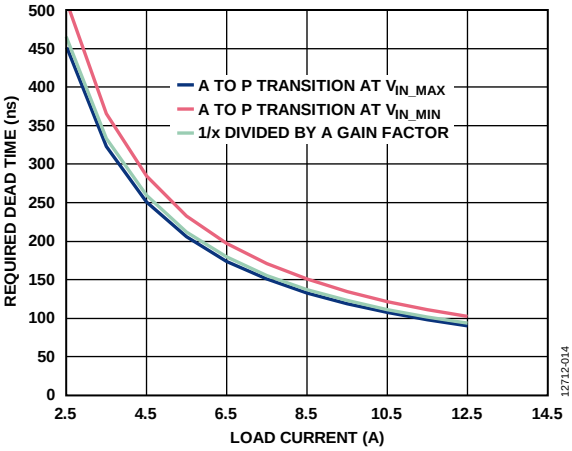

Figure 14. ZVS Transition Time During Active to Passive (A to P) Transition Based on Load Current

CONCLUSION

The ADT feature of the ADP1055 can be applied to any rising or falling edge of the PWM, and it is particularly useful in full bridge phase shifted topologies to achieve ZVS at light loads. With a programmable update rate, the adjustment is applied over a period of several switching cycles, which does not interfere with the control loop during load transients. Switching losses and external inductances are reduced, or in some cases, eliminated by achieving ZVS using ADT, thus compacting the size and weight of the power supply. ADT also enables a high efficiency at light load conditions.

REVISION HISTORY

11/14—Revision 0: Initial Version

AN12712-0-11/14(0)