Optimizing Multiple Output Power Converters

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INTRODUCTION

Many of ADI's integrated circuits that are mainly targeted at single output power converters work well to produce multiple outputs. Our boost ICs can work in flyback, SEPIC, and Cúk configurations, and combinations of these. Many of our buck ICs can effectively implement inverting buck boost, ZETA, and combinations, as well as "flybuck" topologies. This article will not attempt to describe all of the possibilities. Rather, it will focus on one particularly useful topology subset, and three different, not widely known techniques that can help improve performance.

SEPIC, Cúk, ZETA, flyback, and inverting buck boost converters are some of the more likely choices when the buck and boost cannot quite do what is needed. After allowing for turn ratios and voltage inversion, they are all governed by the same relationship between voltage and duty cycle. That relationship is: $V_{OUT} = (D \times V_{IN})/(1 - D)$, where "D" represents the duty cycle. This formula is most easily interpreted for continuous conduction mode (CCM), where the inductor current is always ramping either up or down. For discontinuous conduction mode (DCM), the interval when the total inductor current dwells at zero must be subtracted from the total switching period before calculating the duty cycle.

While there are many useful variations for producing one output, SEPIC, Cúk, ZETA, flyback, and inverting buck boost converters are particularly well suited for generating two or more outputs. Some topology variations and techniques have been developed to improve performance. This article describes some common and some less well known multiple output buck boost topologies, along with three favorite tricks to improve their performance. It also explains why these tricks work.

This article is targeted at engineers with some power conversion experience, and is intended to provide neither a complete design manual nor a complete method for choosing a power conversion topology. However, the information here may affect a designer's choice in topologies by showing ways to gain significant performance improvement. For example, it may be possible to eliminate a switching voltage regulator and avoid producing frequency beats by replacing two single output types with one dual output type. Obviously, this can also reduce cost or lower parts count. We will present five complete designs with test data and BOMs, as well as some other designs for which the concepts apply.

TRICKS AND TOPOLOGIES

For reference, the tricks are:

1) Take at least some feedback to the control loop from all outputs.
2) Series connect the dc; don't just tap the winding.
3) Apply SEPIC (or Cúk, or ZETA) capacitor coupling to output windings.

The first trick is aimed at the control loop, while Trick 2 and Trick 3 are aimed at the plant. We may think of the control loop as being analogous to the controlling "brains," while the "plant" is the physical capability of the power components. In general, neither can substitute for the other. A good power converter needs to be well designed in the plant as well as the control loop.

Let's dive into the subject material with an ac input isolated flyback design, which may be at least partially familiar to many experienced designers. This design uses an industry-standard flyback control IC, but it replaces the old fashioned, adjustable, shunt reference plus optocoupler feedback with the ADuM3190, which uses ADI's *i*Coupler® technology. Compared to the optocoupler, the international safety approved ADuM3190 offers much tighter gain limits across many samples as well as over time and vs. temperature.

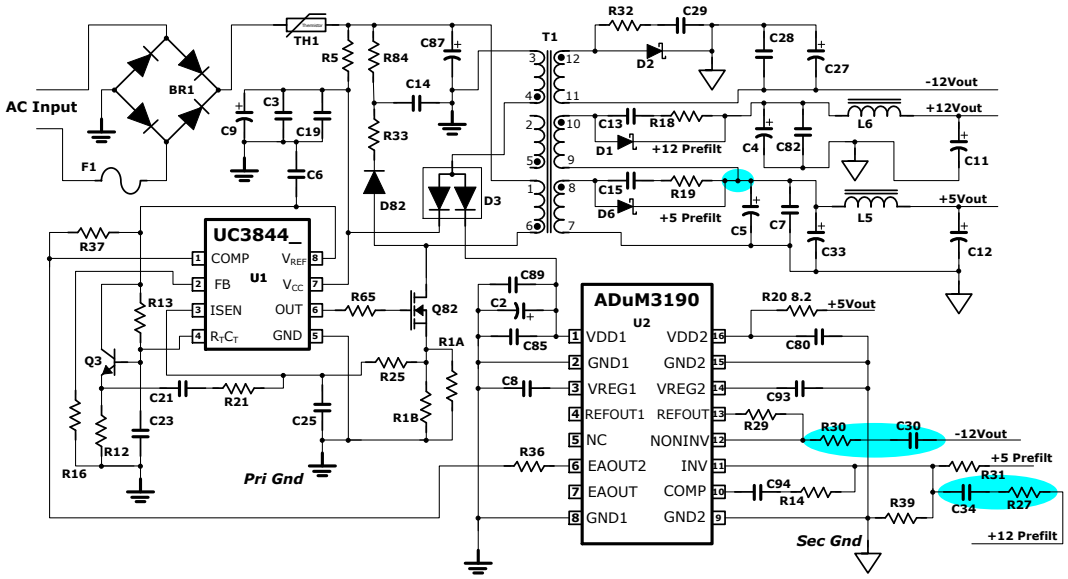

Figure 1. Demonstration Flyback Power Supply with No Input EMI Filter as Designed for 100 V to 250 V AC Input and Triple Outputs of +5 V and ±12 V and 25 W Total Output Power; This Converter Runs at About 75 kHz

Figure 1 is a tested triple output flyback power supply. The blue shaded areas highlight Tricks 1 and 2 as applied to this converter. R31 is the upper feedback divider for the +5 V output. It senses the output from a point before the output filter to help improve the feedback loop phase margin. Snubber R32-C29 is oriented opposite from R18-C13 and R19-C15. This is done for the best fit in the pcb layout. The snubber capacitors are 0603 chips, while the snubber resistors are 1206 chips.

For Trick 1, R27 and C34 (highlighted) couple ac feedback from the +12 output, while C30 and R30 couple ac feedback from the –12 output. The figures below illustrate the results of doing this:

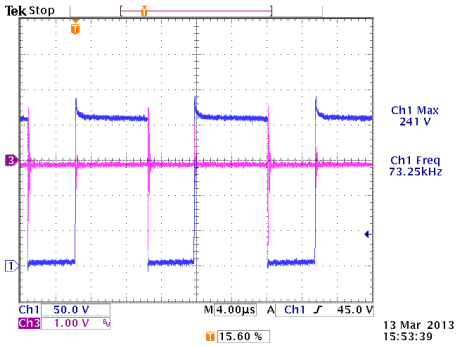

Figure 2. Ch1 is the Drain of the Main Switch (Q82) and Ch3 is the +12 Output; the Converter is Stable in Spite of Some Very Unfavorable Load Conditions: the –12 V Output is Loaded, the +5 Main Output is Unloaded, and the +12 Output Load Current is Between 0 A to 2 A

If the converter in Figure 2 did not include Trick 1, these conditions would cause operation to become severely unstable, as shown in Figure 3.

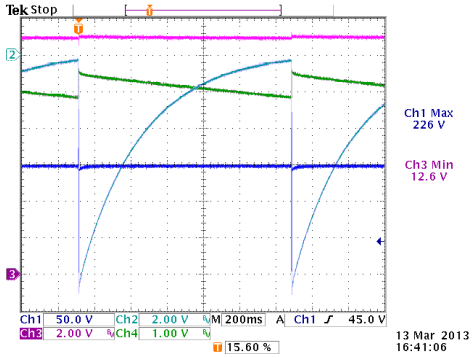

Figure 3. R27 and R30 are Removed; Ch1 is the Main Switch Drain, Ch2 is the –12 V Output, Ch3 is the +12 V Output, and Ch4 is the +5 V Output

For Figure 3, we removed R27 and R30. Ch1 is the main switch drain, Ch2 is the –12 V output, Ch3 is the +12 V output, and Ch4 is the +5 V output. This is a severe example of "multiple output instability" for this offline flyback. The instability is exacerbated by the hiccup/restart of the controller IC. Notice that we have about 12 V p-p oscillation of the –12 output. For this figure, the +12 is unloaded, but with R27 and R30 disconnected, loading the +12 does not resolve the instability.

We will offer a diagnosis of this malfunction later in the article. However, there are some key points to remember:

1) You may have a converter that seems to work acceptably with a severe imbalanced loading condition, as we have described, with little or no load on the main, regulated output. However, the important question is not whether the converter can run in a stable manner; it is whether such

operation is assured. The "acid test" is to try to induce instability and be unable to do so within any foreseeable load conditions. For this purpose, we recommend operating with in-spec full load on all outputs, and then suddenly disconnecting the load from the main output. It is common to find that a design that seemed to work well can be kicked into instability by this method.

2) Assuring stability with any one output loaded alone probably requires dc or ac feedback from that output. If an output in question uses a linear post regulator, take feedback from a point ahead of that regulator. When it is regulating, a linear regulator will decouple its output from changes at its input. Those changes need to be coupled into the switching converter's feedback loop.
3) The usefulness of this technique is not subtle. Once the need has been identified, it is clear and convincing for those many cases where it is applicable.
4) AC-coupled feedback (as opposed to dc) can be much easier to apply when working with negative outputs. Regardless of the output polarity, it is very helpful if you do not want to compromise the dc accuracy of the main output.
5) Synchronous rectification with forced CCM can also prevent multiple output instability, and eliminate the need for this added feedback. We will elaborate on this later.

In Figure 1, we have highlighted the connection of Transformer Pin 9 (the +12 winding) to the cathode of D6, (the +5 rectifier). This is our example of Trick 2. Instead of connecting the two windings directly in series, we are essentially connecting a +7 V dc rectified output in series with a +5 V dc rectified output. The +12 output current is passing through both the +5 and +12 rectifiers. The reason for doing this is to get improved dc cross regulation between the two outputs.

Figure 4 and Figure 5 depict the relationship between +12 output voltage and +5 output current. In both figures, the blue line shows test results with the +12 winding connected to the cathode of D6, while the red line shows test results with the +12 winding connected to the anode of D6. Figure 4 is limited because with 2 A on the +12, we cannot draw much +5 load before running into our 25 W power limit.

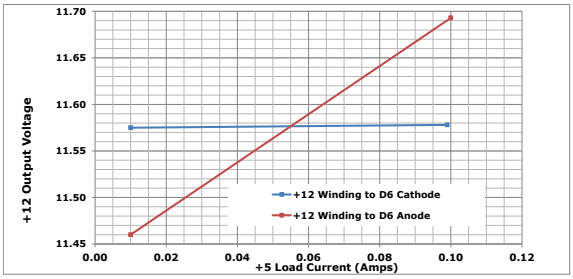

Figure 4. Variation in +12 V_{OUT} vs. +5 Load Current with 2 A Load on the +12 Using Two Different Connections of +12 Winding

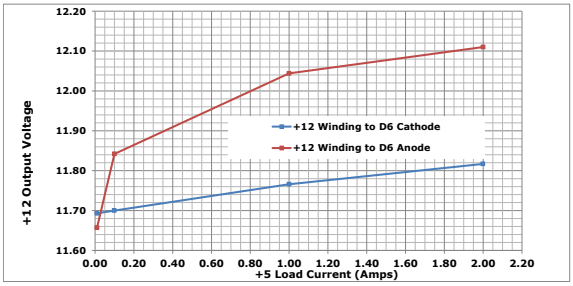

Figure 5. Variation in +12 V_{OUT} vs. +5 Load Current with 1 A Load on the +12 Using Two Different Connections of +12 Winding

Notice that the +12 output voltage is much flatter for both +12 load current values. Counterintuitively, the winding-to-cathode connection in Figure 4 (blue line) actually delivers more +12 output voltage than does the winding-to-anode connection when the +5 output current is very low. This is because with the usual anode connection, the voltage drop through D6 is low when its forward current is low due to low +5 current. Due to this small voltage drop, the feedback loop can hold the +5 output in regulation with reduced volts per turn out of the transformer. This reduced volts per turn out of the transformer causes the +12 output to sag. With the +12 winding connected to the cathode of D6, all of the +12 output current flows through D6 and D1, thus increasing current and dropping voltage in D6. The converter needs to produce more volts per turn out of the transformer in order to regulate the +5, thus causing an increase in the output from the +12 winding. If a design needs to maintain a minimum value of +12 output under such adverse load conditions, the winding-to-anode connection (in other words, the tapped winding) might require a higher +12:+5 turns ratio. This modification would increase the +12 output voltage higher than desired for other, more balanced load conditions. This would degrade efficiency. The result is that the +12 winding to +5 cathode connection could help the designer achieve a more efficient design in spite of the +12 output having two series diode forward voltage drops. We do not assert that this will always be the best approach, but rather that it is worth considering when trying to produce multiple outputs such as these.

Let's have a look at the next circuit example:

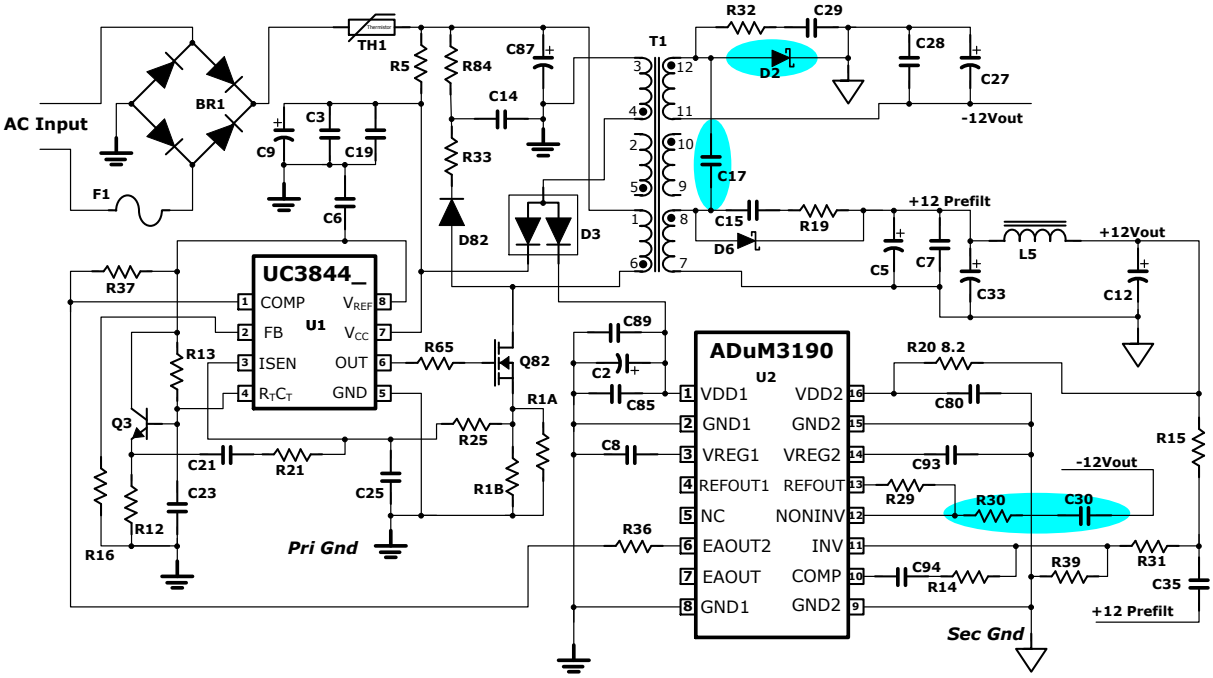

Figure 6. Demonstration of 100 V to 250 V AC Input Flyback Power Supply, Producing ±12 V Outputs of 36 W Total Output Power; This Converter Runs at About 120 kHz

Figure 6 is a dual output power supply that is built on the same pcb as that of Figure 1. For purposes of clarity, most of the unpopulated component locations are not shown.

This converter includes Trick 1, implemented by R30 and C30 (obvious once you see it in the triple output version), while C17 and the connection of the –12 rectifier D2 implement Trick 3. Similar to Trick 2, the objective of Trick 3 is cross regulation.

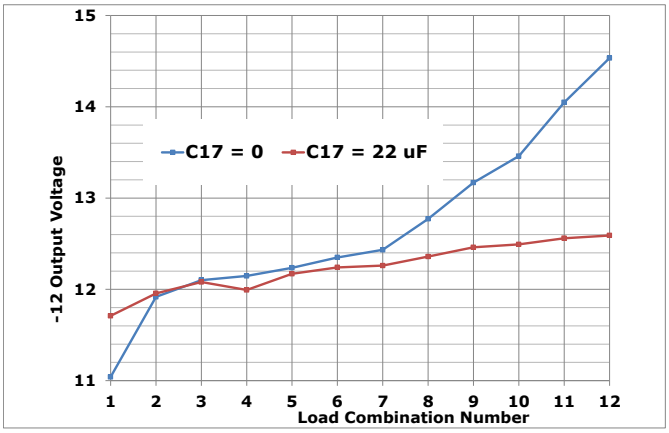

Figure 7. ±12 Output Flyback Converter Using 12 Different Output Load Current Combinations

Table 1: ±12 Output Flyback Converter Load Combinations

Load Combination Number (x-axis)	+12 Output Amps	–12 Output Amps
1	0.01	0.50
2	0.01	0.02
3	0.10	0.02
4	0.10	0.01
5	0.20	0.01
6	0.50	0.02
7	0.50	0.01
8	1.00	0.01
9	2.00	0.02
10	2.00	0.01
11	3.00	0.02
12	3.00	0.01

For this graph, we tested the ±12 output flyback converter using 12 different output load current combinations, both with and without coupling capacitor C17. These load combinations are listed in Table 1. Because the dc feedback is tightly closed around the +12 output, that output stayed

within an 8 mV window and all significant dc voltage variation was in the –12 output. We sorted the results without C17 in order of increasing –12 volt readings. Then we plotted V_{OUT} vs. the same load combinations for the data taken with C17 connected. Figure 7 illustrates that we get much better voltage regulation out of the –12 when C17 is connected; the windings and D2 must be connected as shown in order to use C17. Why is this?

Ideally, a multiple output flyback converter drives its multiple outputs with proportional voltage sources. Unfortunately, real circuits give us stray impedances which serve to decouple this proportionality. These impedances intervene between the outputs and usually introduce load dependence.

The sources of these stray impedances include ESR and ESL of the diodes, ESR and ESL of the pcb layout, and ESR and leakage inductance between the transformer windings. In most typical multiple output flyback designs, the winding leakage inductance is the largest error contributor. It resonates with winding and diode capacitance to cause overshoot and ringing, and the output diodes feeding lightly loaded outputs peak rectify the resulting overshoot. The result is that lightly loaded output voltages rise relative to the more heavily loaded ones and the voltage proportionality is degraded.

In fact, this modification involving D2 and C17 is a significant topological change. In the original design, the two outputs are transformer coupled. We require dc and ac fidelity in the voltage waveform produced by the transformer winding. The magnetic coupling needs to be tight for this to work well; winding leakage inductance will degrade the cross regulation. However, if we apply C17 large enough and sufficiently low impedance, we could insert a large amount of leakage inductance in series with the –12 winding and have the output regulate well. In fact we could replace the –12 winding with a discrete inductor with no magnetic coupling to the transformer (equivalent to infinite leakage inductance), and have it work well. The –12 output then works like that of a Cúk converter, and that is what it is. With both windings on one transformer core, we have a coupled inductor Cúk output.

In a coupled inductor Cúk, the magnetic coupled waveform on both windings should be identical, so that the capacitor has no (ideal and simple analysis) ac voltage across it. In other words, the turns and the phase of the two windings should be the same so that the ac voltages match and they are not trying to drive significant ac through the coupling capacitor. The –12 winding conducts the dc, and the coupling capacitor conducts the ac. In order to keep LC resonant frequencies low enough, very low leakage inductance can require a large value capacitor, so the tightest possible coupling (lowest possible leakage inductance) is not necessarily ideal. This point is not likely to be a big design problem, any more than adding leakage inductance between transformer windings is likely to be difficult.

The triple output converter (Figure 1) cannot use Trick 3 when the +12 winding is connected to the cathode of D6. This is because the +12 winding is working as a 7 V winding with a +5 V dc offset, while the –12 winding is working as a 12 V winding. The two windings have different turns and different ac voltages, so coupling the +12 and –12 rectifier anodes with a capacitor would place an ac short across the transformer.

For our next example circuit, let us do another ±12 V output, but this time it is a nonisolated SEPIC/Cúk combination.

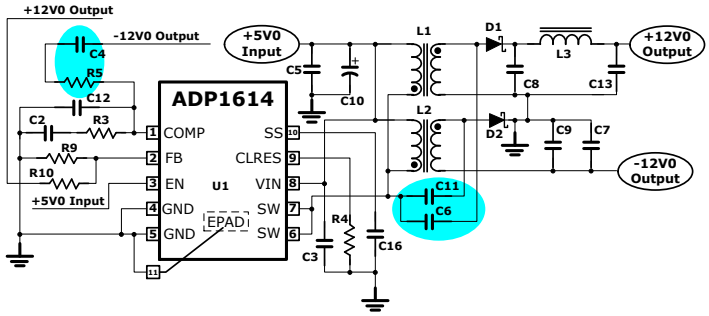

Figure 8. 5 V Input to ±12 V, 250 mA Output SEPIC-Cúk Converter (A Bill of Materials is Included in the Appendix of this Article)

Figure 8 is the schematic for a SEPIC/Cúk converter with ±12 V outputs. This takes a +5 V dc input and converts it to ±12 V dc at up to 250 mA. R9 and R10 are the feedback divider for the main (+12 V) output. In theory, our converter could alternatively sense either the –12 V output alone or the total 24 V output differential, but these options would require some added parts such as an op amp. Barring instability, the dc load regulation on the unregulated output of a well designed SEPIC/Cúk is adequate for many purposes, and a single control loop can tightly and directly regulate only one output anyway, regardless of the converter topology. Trick 3, which is included in any SEPIC or Cúk converter, is implemented with capacitors C6 and C11.

In this topology, the main switch (internal to the ADP1614) is subjected to (adding magnitudes; forget about polarity) V_{IN} plus (either V_{OUT}). With 5 V input and 12 V output, we have 17 V peak on the main switch, which in the ADP1614 is rated at 20 V.

With this design, Trick 1 uses ac feedback from the unregulated negative output to the compensation pin (C4

and R5). Doing this provides the correct feedback polarity for this negative output, but requires that the IC's error amplifier be a transconductance type. Since there is no accurate dc reference associated with the error amplifier output at the compensation pin, dc errors would be difficult to avoid if we used dc coupling. This ac-coupled signal tells the feedback loop which direction the unregulated output is headed at any moment, but does not affect the dc regulation point. If the unregulated output is falling or climbing rapidly while the regulated output is relatively stable, that output voltage slope information turns out to be very useful.

Figure 9 is an illustration of multiple output instability with the SEPIC-Cúk. Unlike the similar misbehavior shown in Figure 3 of the UC3844 ac input flyback, the IC is continuously "awake" with no hiccup restart cycle to contribute to the malaise. R5-C4 was disconnected in order to produce this instability. An initial perturbation may be required in order to upset the feedback loop, so a designer might miss seeing the malfunction if testing is not thorough. The perturbation can be a sudden application of the load on the unregulated output or a sudden removal of the load on the regulated output, for example.

For the oscilloscope shot shown in Figure 10, operation is stable. All conditions are the same as Figure 9, except that R5-C4 are connected, as shown in Figure 8. The control loop could no longer be upset with load current or input voltage perturbations. Although the test conditions and the oscillation are severe, there is no exaggeration here. The improvement from adding a small RC (as shown) can be dramatic.

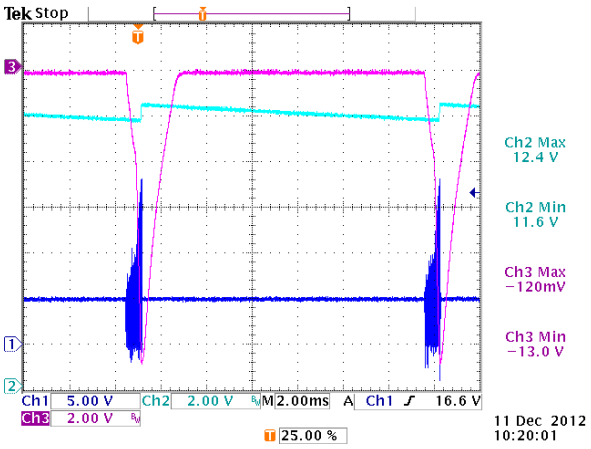

Figure 9. Multiple Output Instability in the SEPIC-Cúk Converter with C4 and R5 Disconnected

In Figure 9, we are testing with a severe corner condition: 150 mA load on the unregulated –12 V output and no load applied to the +12 V output. Ch1 is the main switch node, Ch2 is the unloaded +12 output, and Ch3 is the negative output with 150 mA fixed constant current load.

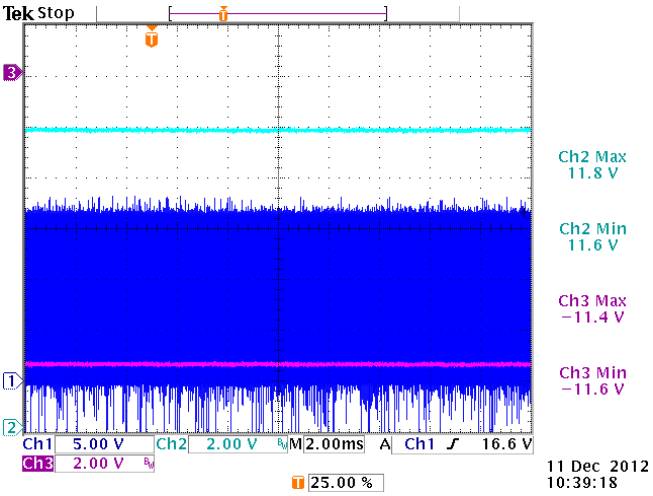

Figure 10. Same Conditions as Figure 9 Except that C4 = 1 nF and R5 = 100 kΩ are Connected as Shown on the Schematic Diagram.

In Figure 10, the output is now stable and cannot be upset by momentary load current or line voltage perturbations. Positive V_{OUT} = 11.993 and negative V_{OUT} = 11.230, which is 6.4% low. This is reasonably good in light of a severe worst case corner condition loading and an unregulated output.

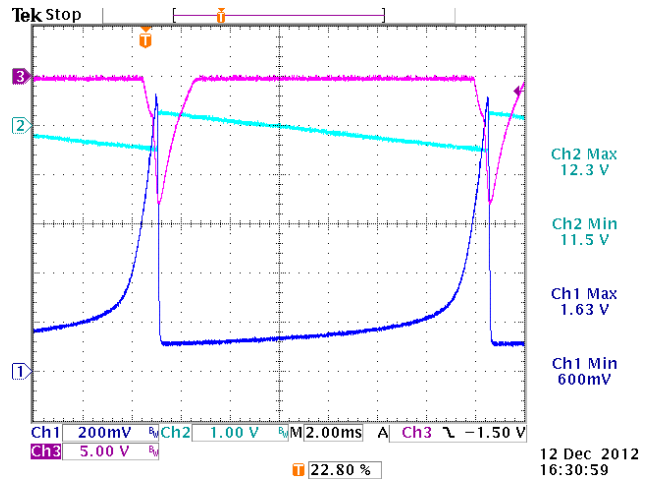

Figure 11. Similar to Figure 9, but Oscilloscope Ch1 is Connected to the COMP Pin of the Controller IC; the Scale Factor on Ch3 (–12 output) has Been Changed to Make Ch1 More Visible, Ch2 Still Indicates the +12 Output

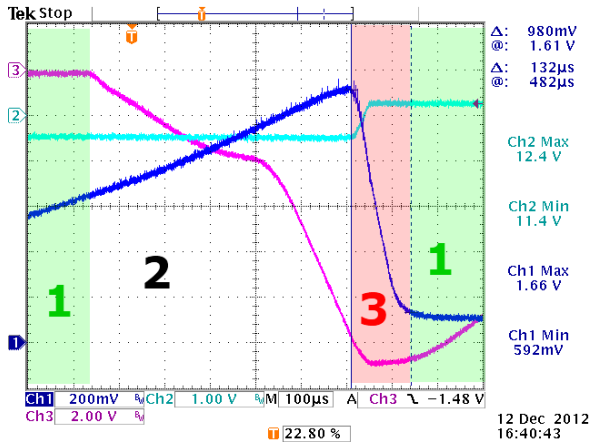

Figure 12: A Faster Time-Based Acquisition of Figure 11, with Shaded Areas to Indicate Phases of the Oscillation Waveform

Our multiple output SEPIC, Cúk, ZETA, flyback, and inverting buck boost converters achieve their slaved output regulation due to fixed ratios of voltage sources connected via the rectifiers to the outputs. These fixed ratios result from regulated volts per transformer turn in a flyback, or the identical ac driving waveform coupling through a capacitor in a SEPIC or Cúk. However, during a pulse skip, this ac voltage momentarily collapses and the multiple outputs become unlinked as the rectifiers become reverse biased. If the voltage on the unregulated output drops way below the expected regulation band during this time, the control loop will typically not know about it and will not quickly respond to correct the error.

Table 2 explains the chain of events that comprises this oscillation seen in Figure 12:

This oscillating scenario takes us outside the realm of linear systems. We have one disconnect between the main output and feedback loop and the unregulated output during a PWM skip, and a second such disconnect when the unregulated output magnitude is rising rapidly. These discontinuities give us a nonlinear system, so an analysis that is limited to linear systems will not explain it properly. However, as is often the case with unstable feedback loops, there is a causal relationship that involves a phase lag between the output voltage and the feedback. C4 and R5 add additional feedback that bypasses most of the phase lag.

Synchronous rectifiers are capable of conducting current in both directions. Some synchronous rectified control ICs (such as the ADP2442) are capable of operating in forced CCM, which avoids pulse skipping, thus there is no significant time when the outputs are decoupled from each other. The bidirectional conduction can permit a large conduction interval to the main output without the need to pass significant dc. As a result, ICs with synchronous rectification and forced CCM can often avoid multiple output instability without the need for feedback from the additional outputs.

Our subject approach to eliminating this instability is to inform the feedback loop as soon as possible that the output voltage magnitude is changing. In linear terms, this would reduce the feedback lag which is an essential component of the severe oscillation. Applying a small amount of ac feedback from the unregulated output accomplishes this goal without affecting the dc accuracy of the main output.

Table 2: Figure 12 Oscillation Waveforms

Waveform Section	What Is Happening
1	The control loop and the regulated output have overshot for some reason and a pulse skip has initiated. The unregulated output is fully loaded so that its voltage magnitude drops rapidly when it is unsupported by the converter output. Meanwhile, the main output has a very light load so its output capacitor sustains the overshot output voltage that is still slightly above the feedback regulation point, and the controller does not quickly resume pulses. The feedback loop is telling the controller "output is too high; deliver no power." Remember that our unregulated output is negative, so the flat top of Ch3 toward the left side of Figure 12 is at its minimum magnitude.
2	Eventually the main output voltage sags enough, and the COMP voltage inside the IC rises enough to command a resumption of pulses, but by this time the fully loaded unregulated output has dropped far under the regulation band. In our example, it has decayed to nearly zero. When energy transfer resumes, the unregulated output clamps the transformer output to its now lower magnitude voltage so that the main output rectifier remains reverse biased. The unregulated output's filter capacitor gets all of the output energy and none is delivered to the main output. The main output drops further as the control loop commands more power and it charges the unregulated output filter capacitor as fast as possible.
3	By the time the unregulated output approaches the normal regulation band, the converter is delivering full power and may be in current limit. At this point, the converter begins to deliver energy to the main output, but because the error amplifier output is at its maximum, it cannot swing back to a stable point fast enough and the main output voltage overshoots. The control loop then reacts by swinging to its minimum and shuts down the PWM output. This initiates another pulse skip, and the cycle repeats.

Some engineers may observe that taking feedback from two points in the output makes it difficult to analyze the resulting linear network stability. We will not argue that philosophical issue here. A relatively small amount of added ac coupling added from the secondary output can make this undesirable mode completely vanish. There are few circumstances where a remedy as small and inexpensive as one small series RC so dramatically resolves a problem.

This added feedback coupling would typically have some effect upon the transient load response waveform. However, the use of very light coupling in the form of a small value capacitor and a high value series resistor can minimize any deleterious effects without sacrificing the desired stability. The effect on transient load response may in fact be favorable. It is possible that if you have a very good simulator with excellent models, the circuit values can be calculated. But if you do not have adequate faith in your simulation, then resolving it on the bench may well be better. Just be sure to margin your component values so that normal variation will not send your design into trouble. Plan on minimizing the added feedback coupling from the unregulated output.

Given that defining and measuring the feedback loop response with two or more feedback points is not straightforward, we use the following methodology to ensure stability:

1) With only main feedback connected, design the feedback loop as would normally be done, assuring good gain and phase margins. Use high di/dt speed load switching to measure and record the converter load transient response. Our purpose in this test is to observe the converter as a linear system, not to push it into multiple output instability. Be careful here; many electronic loads are not capable of switching fast enough to excite the loop at frequencies near unity gain crossover, so a discrete test circuit using a square wave or pulse generator to switch a MOSFET and load resistor may be required. With the transient load applied to only one output at a time, perform this testing on all outputs. Measure all outputs for every test, and try different static load combinations as this may turn up some surprises.
2) Test to see whether the converter is vulnerable to multiple output instability. Most often, a full load on an unregulated output with an unloaded main output is most likely to trigger the issue. It may be necessary to suddenly disconnect the load on the main output.
3) Experimentally determine how much coupling from the nonregulated output is required to prevent the problem. Start coupling with a relatively high capacitor value and low valued resistor. In the circuits that we have discussed, sample starting values would be around 20 kΩ and 100 nF. Assuming this combination fixes the problem, first start increasing the resistor value to find the maximum effective value, then cut that by about half to provide some margin. Second, do similar with the capacitor; start decreasing to find the minimum effective value, then double it.
4) Now repeat the dynamic load response tests. It is common to find improvements in the response waveforms. We have never seen evidence of significant degradation of the gain or phase margin.

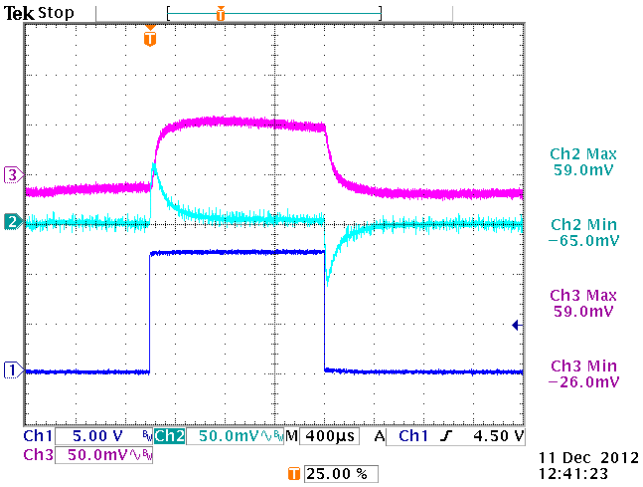

Figure 13. 207 Ω Load (About 58 mA) Switched to Ground from the Positive Output of the SEPIC-Cúk Converter; R4-C5 Are Connected

In Figure 13, we switch a 207 Ω load to ground from the positive output of the SEPIC-Cúk converter. R4-C5 are connected for this test. Ch1 indicates the drain of the load switch FET. Ch2 shows the +12 V output voltage and Ch3 shows the –12 V output voltage. The +12 V output has an additional fixed 20 mA load and the –12 V output has a fixed 150 mA load.

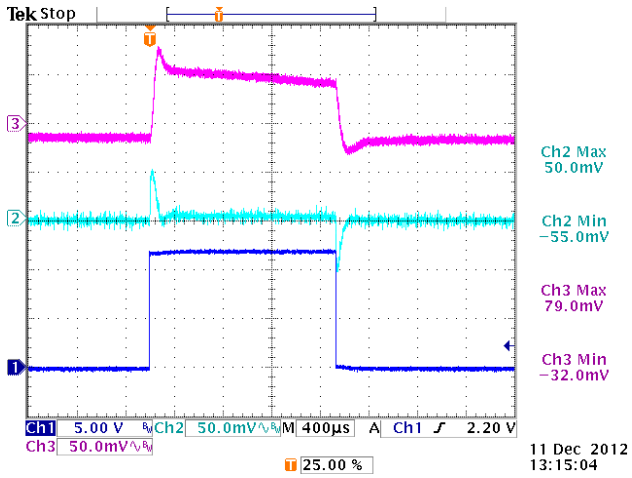

Figure 14. Here We Have Duplicated the Test Shown in Figure 13, but R4-C5 Are Disconnected

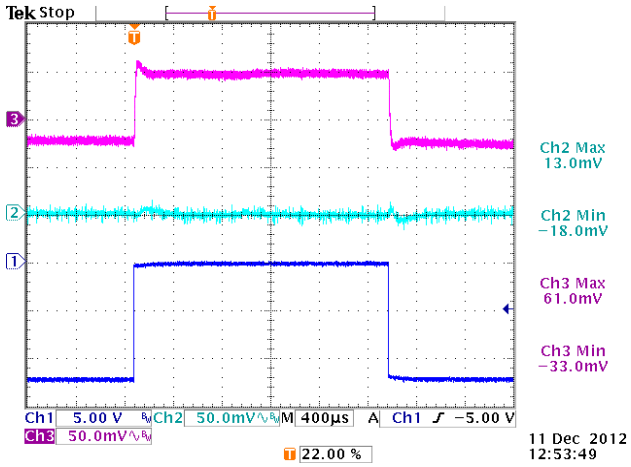

Figure 15. 207 Ω Load (about 58 mA) Switched to Ground from the Negative Output of the SEPIC-Cúk Converter; R4-C5 are Connected

Here, in Figure 15, we switch a 207 Ω load (about 58 mA) to ground from the negative output of the SEPIC-Cúk converter. R4-C5 are connected for this test. Ch1 indicates the drain of the load switch FET. Ch2 shows the +12 V output voltage and Ch3 shows the –12 V output voltage. The –12 V output has an additional fixed 20 mA load and the +12 V output has a fixed 150 mA load.

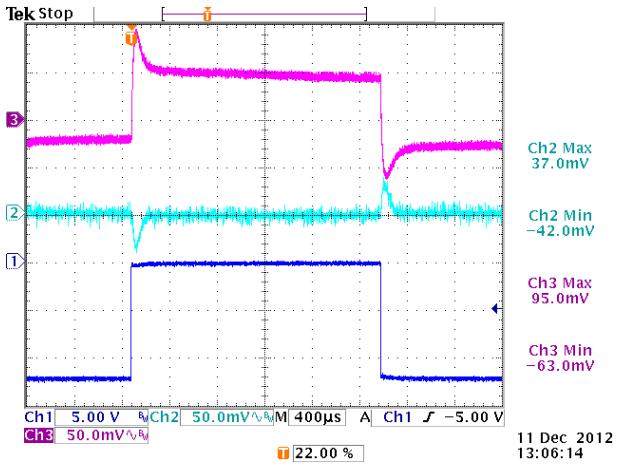

Figure 16. Here We Have Duplicated the Test Shown in Figure 15, but R4-C5 Are Disconnected

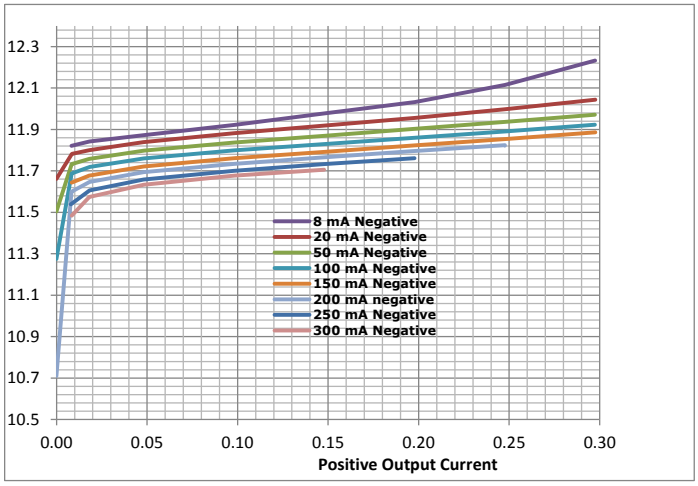

Figure 17. SEPIC-Cúk Measured Negative V_{OUT} vs. Positive I_{OUT} for Different Values of Negative I_{OUT}

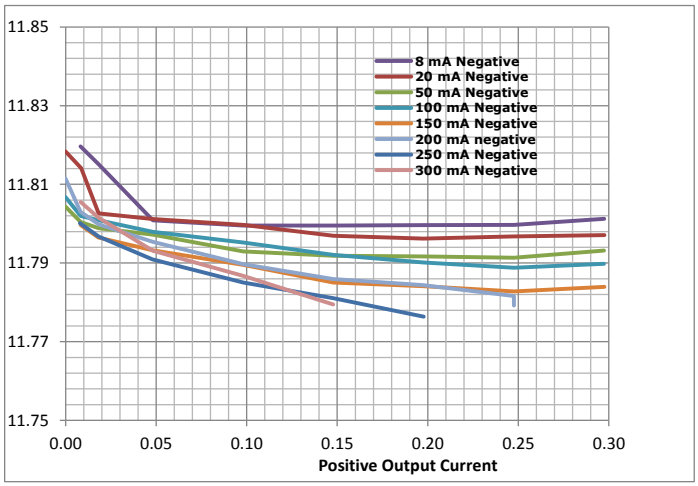

Figure 18. SEPIC-Cúk Measured Positive V_{OUT} vs. Positive I_{OUT} for Different Values of Negative I_{OUT}

Next is a brief detour in the direction of multiple output buck boost converters which can be built similar to the SEPIC-Cúk (such as with an ADP1614 IC). The converters shown in Figure 19 and Figure 20 both lend themselves to all three tricks. Both produce output voltages with a 2:1 ratio. In exchange for these rigid voltage ratios, you get better voltage regulation than you would get from a design that sets output voltage according to transformer turns.

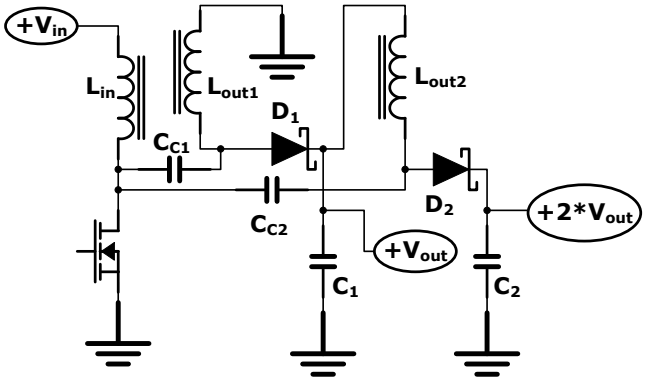

Figure 19. Dual Output SEPIC with Three Inductors, but It Could Alternatively be Built with the Two Coupled Inductors

This is a dual output SEPIC that happens to be built with three inductors, but it could alternatively be built with the two coupled inductors. It is capable of taking 4 V to 7 V dc inputs, and producing +6 V dc and +12 V dc output. Once we include an appropriate control loop, we can implement all three tricks.

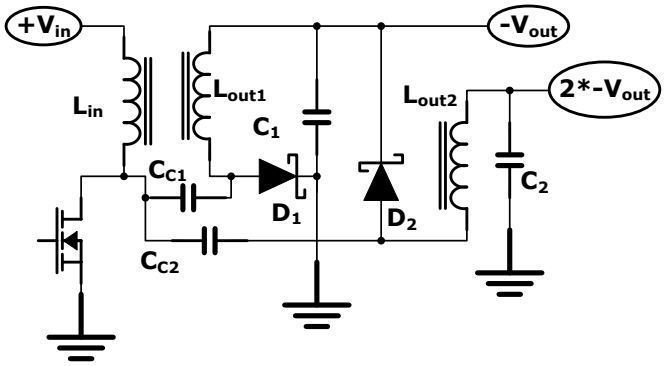

Figure 20. Dual Output Cúk with Capabilities Comparable to the Dual Output SEPIC Shown in Figure 19, but Output Voltages Are Negative

Now, back to our subject of multiple output converters producing symmetrical ±output from positive input. Another way to do this is a combination inverting buck boost/ZETA. The design in Figure 21 uses Trick 1 by taking feedback from the difference between the two outputs, and Trick 3 thanks to its ZETA converter design.

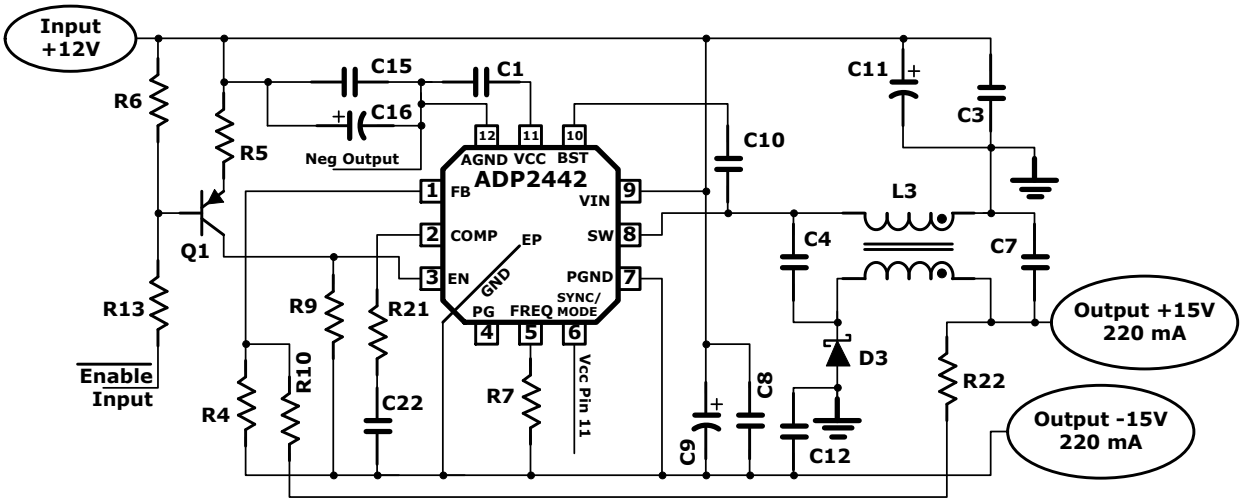

Figure 21. Combined Inverting Buck Boost/ZETA Based on ADP2442 Produces Two Symmetrical Rails Using Only One 2-Winding Coupled Inductor

The ADP2442 provides synchronous rectification for the main –15 V output. With pins 6 and 11 connected as shown, we have forced PWM operation. As a result, this converter is well protected against multiple output instability. Further insurance is provided by the R10-R4 feedback divider sensing the +15 to –15 differential. The control loop is really regulating 30 V. If we reconnect R10 to ground (instead of +15) and adjust the divider ratio accordingly, then the –15 will be tightly regulated and the +15 will be the added output, which is slaved to the –15.

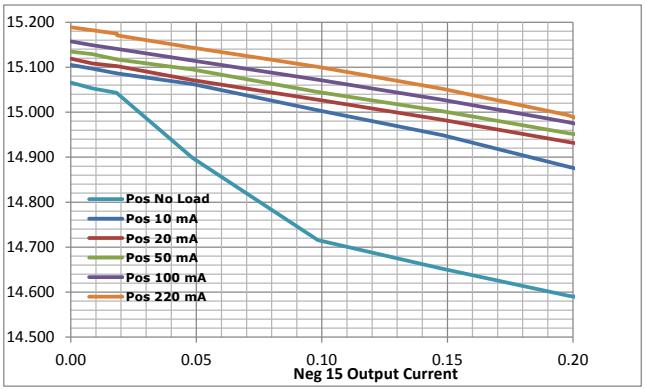

Figure 22. ADP2442 Inverting Buck Boost/ZETA Measured Negative V_{OUT} vs. Negative I_{OUT} for Different Values of Positive I_{OUT}

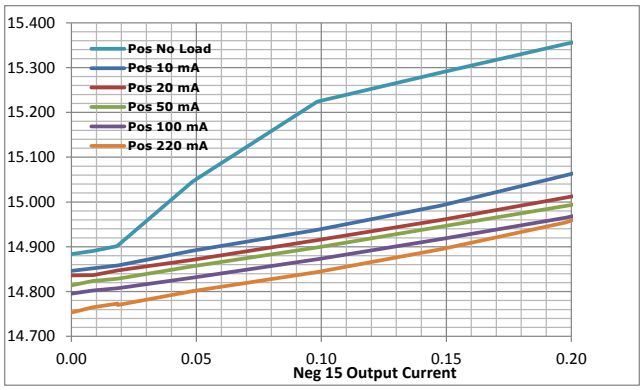

Figure 23. ADP2442 Inverting Buck Boost/ZETA Measured Positive V_{OUT} vs. Negative I_{OUT}, for Different Values of Positive I_{OUT}

Figure 22 and Figure 23 show the measured load/cross regulation of the two outputs. There is a symmetry to these two sets of graphs due to the fact that the differential between the +15 and –15 is tightly regulated by the feedback loop. If one output climbs by 100 mV, the other must fall by a similar amount when the feedback loop is working properly.

In this type of converter, the IC ground pin is not connected to system ground; rather it slews to –15 as the converter starts up. Q1, R5, R6, and R13 scale and level shift the IC precision enable/UVLO function so that the R13 enable responds to the +12 V dc input level and/or an inverted, ground referenced enable signal. If the R13 input is wired to ground, you get a simple input undervoltage lockout. If it is switched to ground, you get the input UVLO function combined with a low going enable control.

The ADP2442 is rated for 36 V maximum, measured from its V_{IN} pin to its ground pin. In this application, the IC V_{IN} pin is at +12 and the ground pin is at –15, so it is subjected to a 27 V differential. This is well within its ratings.

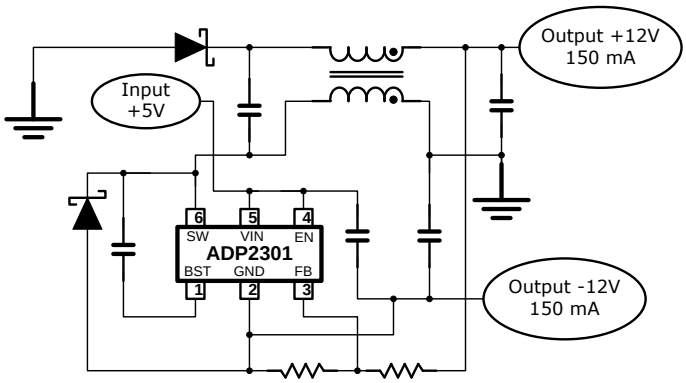

Figure 24. Inverting Buck Boost/ZETA Using ADP2301

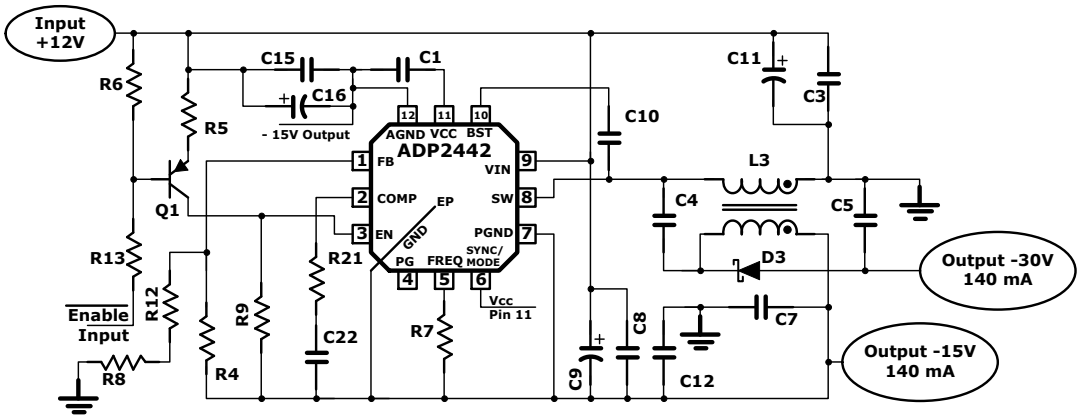

Figure 25: Dual Negative Output Inverting Buck Boost using ADP244

In Figure 24, we have another inverting buck boost/ZETA, similar to Figure 21, but using ADP2301. Freedom from multiple output instability is assured by feedback from the 24 V output differential. Using Trick 1, feedback is taken from both outputs. The ZETA output uses Trick 3. The ADP2301 is capable of handling 20 V so this conversion fits nicely. We do not recommend a dual negative output configuration with the ADP2301 as we do below with the ADP2442, because the ADP2301 has neither an accessible transconductance type COMP pin, nor forced CCM capability. The dual negative output topology will be more susceptible to multiple output instability unless more complex feedback is used.

Figure 25 shows a variation on the circuit in Figure 21 (the two were tested on the same pcb design). Instead of producing one negative and one positive output, we produced two negative outputs. Capacitor coupling (Trick 3) between inductor windings helps this converter to produce dual outputs, which track better than tapped inductors do. Forced CCM operation (Pins 6 and Pin 11 tied together) allows this configuration to behave well without exhibiting dual output instability. Do not couple the –30 V output into Pin 2 COMP, as this can cause improper operation.

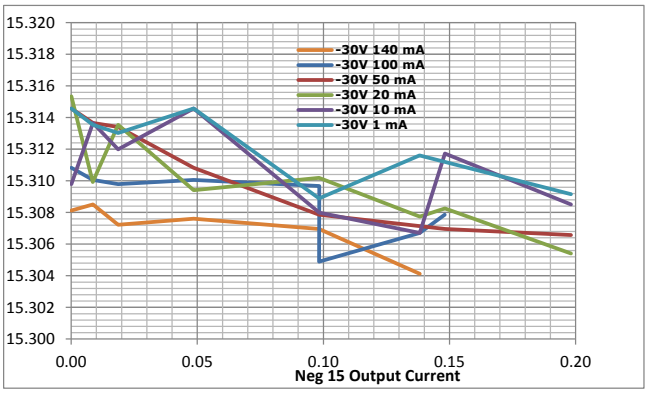

Figure 26. ADP2442 Dual Negative Output Inverting Buck Boost Measured –15 V_{OUT} vs. –15 I_{OUT} for Different Values of –30 I_{OUT}

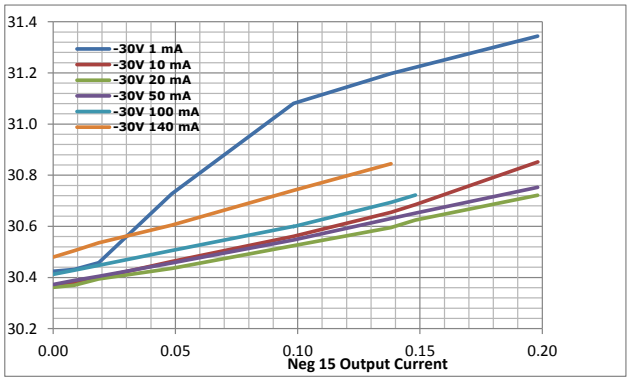

Figure 27. ADP2442 Dual Negative Output Inverting Buck Boost Measured –30 V_{OUT} vs. –15 I_{OUT} for Different Values of –30 I_{OUT}

Figure 26 and Figure 27 show the voltage regulation out of the dual negative buck boost. The –15 regulation shown in Figure 26 looks erratic, but in fact the output is tightly regulated within a <0.1% window. The vertical scale is magnified to show what little variation there is. There are several possible explanations for the weird curve shapes, but the –15 output is directly and tightly regulated; dissecting imperfections in this nearly perfect result is not the purpose of this article. Figure 27 is really the more interesting of the two. The –30 V magnitude climbs with increasing –15 current in all the curves as expected, but as you move between the curves you are observing the effect on the –30 V of varying load current from that output. Increasing the load on the –30 actually increases the load on both outputs, due to the series dc connection. The increasing load on the –15 would tend to increase the voltage out of the –30 as the feedback loop compensates for increased I × R voltage drop in the inductor winding. However, the load also increases the load and the voltage drop on the –30 winding, which would tend to decrease the –30 output voltage. We have opposing trends producing a nonobvious outcome. It turns out that you get the minimum magnitude –30 output voltage when you have a –30 load current that is towards the light load end of the range.

CONCLUSION

This article has presented some useful tricks for improving the performance of several types of multiple output voltage converters. It has also presented some likely unfamiliar or novel topologies which can take advantage of these tricks.

Although most of the designs produce two outputs, all of the topologies shown can be extended to producing three or more outputs in cases where those are needed.

The author hopes that readers are intrigued by some of the ideas presented, so as to inspire creative new designs.

APPENDIX: BILLS OF MATERIAL

For all BOMs, resistors are 1% 0603 except as noted.

Table 3: BOMS for Isolated AC Input Flyback Converters

Ref Des	+5 V ±12 V	±12 V
	Figure 1	**Figure 6**
BR1	KBP208	KBP208
C2	Panasonic FR 150 µF 25 V	Panasonic FR 150 µF 25 V
C3	1 µF 16 V 0805	1 µF 16 V 0805
C4	Panasonic FM 1200 16 V	DNP
C5	Panasonic FM 2200 6.3 V	Panasonic FM 1200 16 V
C6	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C7	Murata GRM31CR61A106KA01	C3216X5R1C475K
C8	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C9	Panasonic FR 25 V	Panasonic FR 25 V
C11	Panasonic FM 680 16 V	DNP
C12	Panasonic FM 1200 6 V3	Panasonic FM 680 16 V
C13	330 pF 100 V NP0 0603	DNP
C14	47 nF 1 kV 1210	47 nF 1 kV 1210 X7R
C15	470 pF 100 V NP0 0603	82 pF 100 V NP0 0603
C17	DNP	22 µF 25 V 1210 X5R
C19	C1608X7R1C105K TDK	C1608X7R1C105K TDK
C21	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C23	1 nF 50 V NP0 0603	1 nF 50 V NP0 0603
C25	100 pF 50 V NP0 0603	100 pF 50 V NP0 0603
C27	Panasonic FM 680 16 V	Panasonic FM 680 16 V
C28	TDK C3216X5R1C475K	TDK C3216X5R1C475K
C29	82 pF 100 V NP0 0603	82 pF 100 V NP0 0603
C30	3.3 nF 50 V X7R 0603	3.3 nF 50 V X7R 0603
C33	Panasonic FM 2200 6 V3	Panasonic FM 1200 16 V
C34	10 nF 50 V X7R 0603	10 nF 50 V X7R 0603
C35	DNP	100 nF 50 V X7R 0603
C80	TDK C1608X7R1C105K	TDK C1608X7R1C105K
C82	C3216X5R1C475K	DNP
C85	TDK C1608X7R1C105K	TDK C1608X7R1C105K
C87	Aluminum Electrolytic 150 µF 400 V 105° snap in	Aluminum Electrolytic 150 µF 400 V 105° snap in
C89	C1608X7R1C105K	C1608X7R1C105K
C93	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C94	3.3 nF 50 V X7R 0603	22 nF 50 V X7R 0603
D1	MBRS360T3 ON Semi	DNP
D2	MBRS1100 ON Semi	SS2PH10 Vishay
D3	BAW56	BAW56
D6	PDS1040L Diodes Inc.	SS5P10 Vishay
D82	ES1J Fairchild	ES1J Fairchild
F1	2A 250 VAC time delay	2A 250 VAC time delay
L5	ME3220 1 µH Coilcraft	500 nH; 4T AWG 20 on Micrometals T30-52
L6	ME3220 1 µH Coilcraft	DNP
Q3	MMBT3904	MMBT3904
Q82	SPD03N60C3 Infineon	SPD03N60C3 Infineon
R12	2.0 k	2.0 k
R13	12.7 k	7.5 k
R14	20 k	20 k
R15	DNP	27.4 k
R16	100 Ω	100 Ω
R18	8.2 Ω 1206 5%	DNP
R19	16.9 Ω 1206	33 Ω 5% 1206
R20	8.2 Ω 1206	8.2 Ω 1206
R21	10 k	10 k
R25	1 k	1 k
R27	47.5 k	DNP
R29	3.48 k	3.48 k
R30	10 k	10 k
R31	15 k	15 k
R32	33 Ω 5% 1206	33 Ω 5% 1206
R36	200 Ω	200 Ω
R37	20 k	20 k
R39	4.75E+03	4.75E+03
R65	8.2 Ω 1206	8.2 Ω 1206
R84	20 kΩ 500 mW; 2 × 20 kΩ 1206's in parallel, in series with two more (4 total)	20 k Ω 500 mW; 2 × 20 k Ω 1206's in parallel, in series with two more (4 total)

R1A	0.68 Ω 1206	0.68 Ω 1206
R1B	DNP	DNP
R33	75 Ω 500 mW; 2 × 75 Ω 1206's in parallel, in series with two more (4 total)	75 Ω 500 mW; 2 × 75 Ω 1206's in parallel, in series with two more (4 total)
R5	132.6 k 0.75W (6 × 22.1 k 1206 in series)	132.6 k 0.75W (6 × 22.1 k 1206 in series)
T1	Transformer wound on Ferroxcube PQ3230 3F3 46T primary, 3T 5V output, 4T +12 V output, 7T -12 V output, 7T control	Transformer wound on Ferroxcube PQ3230 3F3 36T primary, 5T 12 V output, 5T control
Th1	Inrush limiter 16 Ω 1.2 A	Inrush limiter 16 Ω 1.2 A
U1	UC3844A or UC3844B	UC3844A or UC3844B
U2	ADuM3190 Analog Devices, Inc.	ADuM3190 Analog Devices, Inc.

Table 4: BOM for ADP1614 SEPIC/Cúk found in Figure 8:

Ref	Rating	Size/Type/PN	Manufacturer
C2	2.2 nF 25 V, 10%	0603, X7R	Generic
C3	1.0 µF 10 V, 20%	0603, X5R	Generic
C4	1.0 nF 25 V, 10%	0603, X7R or NP0	Generic
C5	10 µF 10 V, 10%	GRM31CR61A106K	Murata
C6	2.2 µF 25 V, 10%	GRM21BR61E225KA12L	Murata
C7	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C8	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C9	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C10	68 µF 16 V	EEUFC1C680	Panasonic
C11	2.2 µF 25 V, 10%	GRM21BR61E225KA12L	Murata
C12	15 pF 10 V, 10%	0603, NP0	Generic
C13	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C16	100 nF 10 V, 10%	0603, X7R	Generic
D1	Schottky 1A 30 V	STPS1L30U	ST Micro
D2	Schottky 1A 30 V	STPS1L30U	ST Micro
L1	Inductor Coupled 22 µH	LPD6235-223	Coilcraft
L2	Inductor Coupled 22 µH	LPD6235-223	Coilcraft
L3	Inductor 1 µH	ME3220-102	Coilcraft
R3	20 k 5%	0603	Generic
R4	110 k 1%	0603	Generic
R5	49.9 k 1%	0603	Generic
R9	4.99 k 1%	0603	Generic
R10	26.1 k 1%	0603	Generic
U1	ADP1614ACPZ-1.3	Boost regulator IC 1.3 MHz	Analog Devices, Inc.

Table 5: BOMs for the Two Dual Output ADP2442 Converters

	±15 V_{OUT}	**–15 V and –30 V_{OUT}**
	Figure 21	**Figure 25**
C1	TDK C1608X5R1C105M	TDK C1608X5R1C105M
C3	TDK C2012X5R1C475M	TDK C2012X5R1C475M
C4	TDK C3216X7R1E105K	TDK C3216X7R1E105K
C5	DNP	Murata GRM32ER71H475KA88
C7	Murata GRM32DR61E106K	Murata GRM32DR61E106K
C8	TDK C3216X7R1H105K	TDK C3216X7R1H105K
C9	Suncon 35CE4R7GA	Suncon 35CE4R7GA
C10	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C11	Suncon 16CE22KX	Suncon 16CE22KX
C12	TDK C3216X7R1E475M	TDK C3216X7R1E475M
C15	Murata GRM32ER71H475KA88	Murata GRM32ER71H475KA88
C16	DNP	DNP
C22	2.20E-09	2.20E-09
D3	Vishay SS1P4	Vishay SS1P4
L3	Coilcraft LPD6235-473	Coilcraft LPD6235-473
Q1	MMBT3906	MMBT3906
R4	3.01 k	3.01 k
R5	26.1 k	26.1 k
R6	10 k	10 k
R7	200 k	200 k
R8	47.5 k	DNP
R9	4.99 k	4.99 k
R10	DNP	4.32 k
R12	26.1 k	DNP
R13	4.99 k	4.99 k
R21	20 k	20 k
R22	DNP	143 k
U1	ADP2442ACPZ ADI	ADP2442ACPZ ADI

ACKNOWLEDGEMENTS

I want to thank Dr. Richard Redl for valuable consultation on the content of this article.

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