ANALOG DEVICES

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APPLICATION NOTE

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How to Successfully Apply Low Dropout Regulators

by Ken Marasco

INTRODUCTION

A low dropout (LDO) regulator is capable of maintaining its specified output voltage over a wide range of load currents and input voltages, down to a very small difference between input and output voltages. This difference, known as the dropout voltage or headroom requirement, can be as low as 80 mV at 2 A. The adjustable output, low dropout regulator (see "Break Loose from Fixed IC Regulators" by Dobkin in the References section) first came to public attention in 1977. Current portable devices often require up to 20 low dropout linear regulators. Many of the LDOs in today's portable devices are integrated into multifunction power management ICs (PMICs), highly integrated systems with many power domains for audio, battery charging, housekeeping, lighting, communications, and other functions. For more information on power management ICs, visit www.analog.com/power-management.

As portable systems rapidly evolve, however, the integrated PMIC cannot keep up with peripheral power requirements. Dedicated LDOs must be added in the later stages of system development to power such optional items as camera modules, Bluetooth®, WiFi®, and other bolt-on functions. LDOs have also been used to reduce noise, to solve voltage-regulation problems caused by electromagnetic interference (EMI) and printed circuit board (PCB) routing, and to improve system power efficiency by switching off unneeded functions.

This application note reviews the basic LDO topology, explains key specifications, and shows the application of low dropout voltage regulators in systems. Examples are given using design characteristics of Analog Devices, Inc., LDO families. For more information on LDOs, visit www.analog.com/linear-regulators.

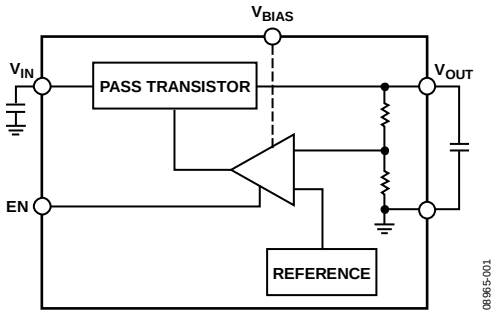

Figure 1. An LDO Regulates the Output Voltage with a Low Dropout Voltage (The Difference Between V_{OUT} and the Lowest Specified Value of V_{IN} at the Rated Load Current)

TABLE OF CONTENTS

BASIC LDO ARCHITECTURE

An LDO consists of a voltage reference, an error amplifier, a feedback voltage divider, and a pass transistor, as shown in Figure 1 (see "Ask The Applications Engineer—37, Low-Dropout Regulators" by Patoux in the References section). Output current is delivered via the pass transistor. Its gate voltage is controlled by the error amplifier, which compares the reference voltage with the feedback voltage, amplifying the difference to reduce the error voltage. If the feedback voltage is lower than the reference voltage, the gate of the pass transistor is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the pass transistor is pulled higher, restricting the current flow and decreasing the output voltage.

The dynamics of this closed-loop system are based on two main poles: the internal pole formed by the error amplifier/pass transistor and the external pole formed by the output impedance of the amplifier and the equivalent series resistance (ESR) of the output capacitor. The output capacitance and its ESR affect the loop stability and the response to transient changes in load current. An ESR of ≤1 Ω is recommended to ensure stability. Also, LDOs require input and output capacitors to filter noise and control load transients. Larger values improve the transient response of the LDO, but increase the start-up time. Analog Devices LDOs are designed to be stable over the specified operating conditions when the specified capacitors are used.

LDO EFFICIENCY

Increased efficiency is a constant demand from the design engineer. This translates into a reduction of the quiescent current (I_Q) and forward-voltage drop.

$$LDO\ efficiency = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN}(I_{OUT} + I_Q)} \right) \times 100\%$$

With I_Q in the denominator, it is evident that the higher I_Q is, the lower the efficiency becomes. Current LDOs have reasonably low I_Q, and for simplicity, I_Q can be neglected in efficiency calculations if I_Q is very small compared to I_{LOAD}. Then LDO efficiency is simply (V_{OUT}/V_{IN}) × 100%. Because the LDO has no way to store significant amounts of unused energy, power not delivered to the load is dissipated as heat within the LDO.

$$Power\ dissipated\ (P_D) = (V_{IN} - V_{OUT}) \times I_{IN}$$

Providing a stable power supply voltage independent of load and line variations, changes in ambient temperature, and the passage of time, LDOs are most efficient with small differences between supply voltage and load voltage. For example, as a lithium-ion battery drops from 4.2 V (fully charged) to 3.0 V (discharged), a 2.8 V LDO connected to the battery maintains a constant 2.8 V at the load (dropout voltage less than 200 mV), but its efficiency increases from 67% with the fully charged battery to 93% with the discharged battery.

To improve efficiency, LDOs can be connected to an intermediate voltage rail generated by a high efficiency switching regulator such as the ADP2108. With a 3.3 V switching regulator, for example, the LDO efficiency is constant at 85%, and the overall system efficiency is 81%, assuming 95% efficiency for the switching regulator.

CIRCUIT FEATURES ENHANCE LDO PERFORMANCE

An enable input permits external control of LDO turn-on and turn-off, allowing supplies to be sequenced in proper order in multirail systems. Soft start limits inrush current and controls output voltage rise time during power-up. A sleep state minimizes power drain, especially useful in battery-based systems, while allowing fast turn-on. Thermal shutdown turns the LDO off if its temperature exceeds the specified value. Overcurrent protection limits the LDO's output current and power dissipation. Undervoltage lockout disables the output when the supply voltage is below the specified minimum value. Figure 2 shows a simplified typical power system for portable designs.

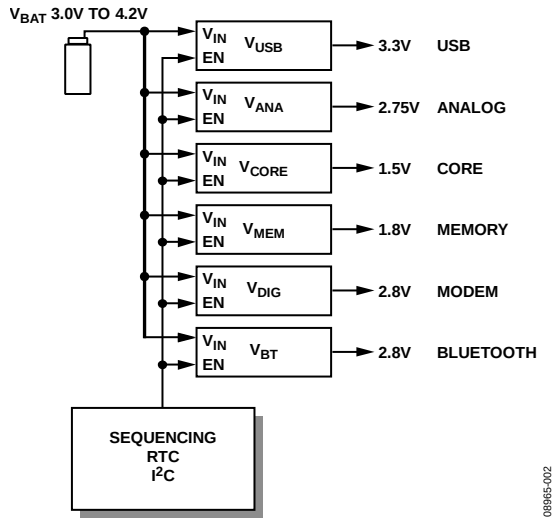

Figure 2. Typical Power Domains in a Portable System

UNDERSTANDING LINEAR REGULATOR REQUIREMENTS

LDOS FOR DIGITAL LOADS

Digital linear regulators such as the ADP170 and ADP1706 are designed to support the main digital power supply requirements of a system, usually microprocessor cores and system input/output (I/O) circuitry. LDOs for DSPs and microcontrollers have to work with good efficiency and handle high and rapidly varying currents. Newer application requirements put tremendous strain on the digital LDO because processor cores often change clock speed to save energy. The clock speed variation, in response to software-induced loading, translates into a demanding need for LDO load regulation capability.

The important characteristics for digital loads are line and load regulation and transient undershoot and overshoot. When powering low voltage microprocessor cores, accurate output control is very important at all times; inadequate regulation can allow the core to latch up. These parameters are not always featured in data sheets, and graphs of transient response may show optimistic rise and fall speed in response to transient signals. Line and load regulation can be expressed as percent deviation of output voltage with load change, actual V/I values, or both, at a specific load current.

To save energy, digital LDOs are designed with low I_Q to increase battery life, and portable systems have long periods of low power operation when the software is idling. During periods of inactivity, the system goes to sleep, requiring the LDO to shut down and consume less than 1 μA. While the LDO is in sleep mode, all of the circuits, including the band gap reference, are switched off. When the system returns to active mode, fast turn-on times are required, during which the digital supply voltage must not overshoot excessively. Excessive overshoot can result in system latch-up, sometimes requiring the removal of the battery or activation of the master reset button to correct the problem and restart the system.

LDOS FOR ANALOG AND RF LOADS

Low noise and high power supply ripple rejection (PSRR) as found in the ADP121 and ADP130 are important for LDOs used in the analog environment because analog devices are more sensitive to noise than digital devices. Analog LDO requisites are mainly driven by the wireless interface requirements: do no harm to the receiver or transmitter, and create no pop or hum in the audio system. The wireless connection is highly susceptible to noise, and the receiver's effectiveness can be reduced if the noise interferes with the signal. When considering an analog linear regulator, it is important for the device to suppress noise from upstream sources and downstream loads, while not adding further noise itself. Analog regulator noise is measured in volts rms and should be below 35 mV when used in sensitive circuits. PSRR, the LDOs ability to suppress upstream noise on the power supply line should be greater than 60 dB. The ADP150 ultralow noise LDO with an output noise of 9 mV and a PSRR of 70 dB is an excellent choice to power sensitive analog circuits. Adding an external filter or a bypass capacitor can also reduce noise, but adds cost and increases PCB solution size. Noise reduction and supply noise rejection can also be achieved by care and ingenuity in the internal design of the LDO. When selecting LDOs, it is important to review the product details in relation to the overall performance needed for each system.

KEY LDO SPECIFICATIONS AND DEFINITIONS

Specifications on the front page of manufacturer data sheets are brief summaries, often presented in a way that emphasizes the attractive features of the device. The key parameters often emphasize typical performance characteristics that can be more fully understood only when consulting the complete specifications and other data within the body of the data sheet. Because there is little standardization among manufacturers in the way specifications are presented, power designers need to understand the definition and the methodology used to obtain key parameters listed in the electrical specifications table. The system designer should pay close attention to key parameters, such as ambient and junction temperature ranges, X and Y scales of graphic information, loads, rise and fall times of transient signals, and bandwidth. The following sections describe some important parameters relating to the characterization and application of Analog Devices LDOs.

INPUT VOLTAGE RANGE

An LDO's input voltage range determines the lowest usable input supply voltage. The specifications may show a wide input voltage range, but the lowest input voltage must be greater than the dropout voltage plus the desired output voltage. For example, a 150 mV dropout means that the input voltage must be above 2.95 V for a regulated 2.8 V output. If the input voltage drops below 2.95 V, the output voltage drops below 2.8 V.

GROUND (QUIESCENT) CURRENT

The quiescent current, I_Q, is the difference between the input current, I_{IN}, and the load current, I_{OUT}, measured at the specified load current. For fixed-voltage regulators, I_Q is the same as the ground current, I_G. For adjustable-voltage regulators, such as the ADP171, the quiescent current is the ground current minus the current from the external resistance divider network.

SHUTDOWN CURRENT

Shutdown current is the input current consumed when the device has been disabled. Usually below 1.0 µA for portable LDOs, this specification is important for battery charge life during long standby times when the portable device is turned off.

OUTPUT VOLTAGE ACCURACY

Analog Devices LDOs are designed for high output voltage accuracy; they are factory-trimmed to within ±1% at 25°C. Output voltage accuracy is specified over the operating temperature, input voltage, and load current ranges; error is specified as ±x% worst case.

LINE REGULATION

Line regulation is the change in output voltage for a change in the input voltage. To avoid inaccuracy due to changes in chip temperature, the measurement is made under conditions of low power dissipation or by using pulse techniques.

DYNAMIC LOAD REGULATION

Most LDOs can easily hold the output voltage nearly constant as long as the load current changes slowly. When the load current changes quickly, however, the output voltage changes. How much the output voltage changes when subjected to a change in load current defines load transient performance.

DROPOUT VOLTAGE

Dropout refers to the smallest difference between input and output voltages required to maintain regulation; that is, an LDO can hold the output load voltage constant as the input is decreased until the input reaches the output voltage plus the dropout voltage, at which point the output drops out of regulation. The dropout voltage should be as low as possible to minimize power dissipation and maximize efficiency. Typically, dropout is considered to be reached when the output voltage has dropped to 100 mV below its nominal value. The load current and junction temperature can affect the dropout voltage. The maximum dropout voltage should be specified over the full operating temperature range and load current.

START-UP TIME

Start-up time is defined as the time between the rising edge of the enable signal to V_{OUT} reaching 90% of its nominal value. This test is usually performed with V_{IN} applied and the enable pin toggled from off to on. Note that, in some cases where the enable is connected to V_{IN}, the start-up time can substantially increase because the band gap reference takes time to stabilize. Start-up time of a regulator is an important consideration for applications where the regulator is frequently turned off and on to save power in portable systems.

CURRENT-LIMIT THRESHOLD

Current-limit threshold is defined as the load current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

OPERATING TEMPERATURE RANGE

Operating temperature range can be specified by ambient and junction temperature. Because an LDO dissipates heat, the IC always operates above the ambient. How much it operates above the ambient temperature depends on the operating conditions and the PCB thermal design. A maximum junction temperature (T_J) is specified because operation above the maximum junction temperature for extended periods may affect device reliability, statistically specified as mean time to failure (MTTF).

THERMAL SHUTDOWN (TSD)

Most LDOs incorporate silicon thermostats to protect the IC from thermal runaway. They are used to power down the LDO if the junction temperature exceeds the specified thermal shutdown threshold. Hysteresis is required to allow the LDO to cool down before restarting. TSD is important because it protects more than the LDO alone; excessive heat affects more than just the regulator. Heat conducted from the LDO to the PCB (or to the LDO from hotter elements on the board) can damage the PCB material and solder connections over time and damage nearby components, reducing the life of the device. Thermal shutdown also affects system reliability. Thermal design to control the board temperature (for example, heat sinking, cooling) is thus an important system consideration.

ENABLE INPUT

LDO enables, offered in positive and negative logic, turn the device on and off. Active-high logic enables the device when the enable voltage exceeds the logic high threshold. Active-low logic enables the device when the enable voltage is below the logic low threshold. The enable input permits external control of LDO turn-on and turn-off, an important feature in the sequencing of supplies in multirail systems. Some LDOs have substantially lower start-up times because their band-gap reference is on while the LDO is disabled, allowing the LDO to turn on faster.

UNDERVOLTAGE LOCKOUT

Undervoltage lockout (UVLO) ensures that voltage is supplied to the load only when the system input voltage is above the specified threshold. UVLO is important because it only allows the device to power on when the input voltage is at or above what the device requires for stable operation.

OUTPUT NOISE

The LDO internal band gap voltage reference is the source of noise, usually specified in microvolts rms over a specific bandwidth. For example, the ADP121 has an output noise of 40 μV rms from 10 kHz to 100 kHz at a V_{OUT} of 1.2 V. When comparing data sheet specifications, the specified bandwidth and operating conditions are important considerations.

POWER-SUPPLY RIPPLE REJECTION

PSRR, expressed in decibels, is a measure of how well the LDO rejects ripple from the input power supply over a wide frequency range (1 kHz to 100 kHz). In an LDO, PSRR can be characterized in two frequency bands. Band 1 is from dc to the control loop's unity-gain frequency; PSRR is set by the open-loop gain of the regulator. Band 2 is above the unity-gain frequency; PSRR is unaffected by the feedback loop. Here PSRR is set by the output capacitor and any leakage paths from the input to the output pins. Choosing a suitably high value output capacitance typically improves PSRR in this latter band. In Band 1, the Analog Devices proprietary circuit design reduces changes in PSRR due to input voltage and load variations. For optimum supply rejection, the PCB layout must be considered to reduce the leakage from input to output, and grounding should be robust.

MINIMUM INPUT AND OUTPUT CAPACITANCE

The minimum input and output capacitance should be greater than specified over the full range of operating conditions, especially operating voltage and temperature. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R-type and X5R-type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

REVERSE-CURRENT PROTECTION FEATURE

A typical LDO with a PMOS pass transistor has an intrinsic body diode between V_{IN} and V_{OUT}. When V_{IN} is greater than V_{OUT}, this diode is reverse-biased. If V_{OUT} is greater than V_{IN}, the intrinsic diode becomes forward-biased and conducts current from V_{OUT} to V_{IN}, potentially causing destructive power dissipation. Some LDOs, such as the ADP1740/ADP1741 for example, have additional circuitry to protect against reverse current flow from V_{OUT} to V_{IN}. The reverse current protection circuitry detects when V_{OUT} is greater than V_{IN} and reverses the direction of the intrinsic diode connection, reverse-biasing the diode.

SOFT START

Programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. For applications that require a controlled inrush current at startup, LDOs such as the ADP1740/ADP1741 provide a programmable soft start (SS) function. To implement soft start, a small ceramic capacitor is connected from SS to GND.

CONCLUSION

LDOs perform a vital function. Though simple in concept, there are many factors to consider in applying them. This application note has reviewed basic LDO topology, and explained key specifications and application of low dropout voltage regulators in systems. Data sheets contain much helpful information; and more information (selection guide, data sheets, application notes), as well as ways to obtain assistance, are available on the Analog Devices power management web site. For more information, visit www.analog.com/power-management. Also available is ADIsimPower™, the fastest, most accurate dc-to-dc power management design tool (visit www.analog.com/ADIsimPower).

REFERENCES

Dobkin, Robert. April 12, 1977. "Break Loose from Fixed IC Regulators." *Electronic Design*.

Patoux, Jerome. 2007. "Ask The Applications Engineer—37, Low-Dropout Regulators." *Analog Dialogue* 41-2, pp. 8-10.

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