5 A, Low V_{IN}, Low Noise, CMOS Linear Regulator

Data Sheet **ADP1765**

FEATURES

- 5 A maximum output current
- Low input voltage supply range
  - V_{IN} = 1.10 V to 1.98 V, no external bias supply required
- Fixed output voltage range (V_{OUT_FIXED}): 0.55 V to 1.5 V
- Adjustable output voltage range (V_{OUT_ADJ}): 0.5 V to 1.5 V
- Ultralow noise: 2 µV rms, 100 Hz to 100 kHz
- Noise spectral density: 5 nV/√Hz at 10 kHz; 4 nV/√Hz at 100 kHz
- Low dropout voltage: 59 mV typical at 5 A load
- Operating supply current: 5 mA typical at no load
- ±1.5% fixed output voltage accuracy over line, load, and temperature
- Excellent power supply rejection ratio (PSRR) performance
  - 61 dB typical at 10 kHz at 5 A load
  - 43 dB typical at 100 kHz at 5 A load
- Excellent load/line transient response
- Soft start to reduce inrush current
- Optimized for small 22 µF ceramic capacitors
- Current-limit and thermal overload protection
- Power-good indicator
- Precision enable
- 16-lead, 3 mm × 3 mm LFCSP package

APPLICATIONS

- Regulation to noise sensitive applications such as radio frequency (RF) transceivers, analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuits, phase-locked loops (PLLs), voltage controlled oscillators (VCOs) and clocking integrated circuits
- Field-programmable gate array (FPGA) and digital signal processor (DSP) supplies
- Medical and healthcare
- Industrial and instrumentation

GENERAL DESCRIPTION

The ADP1765 is a low noise, low dropout (LDO) linear regulator. It is designed to operate from a single input supply with an input voltage as low as 1.10 V without the requirement of an external bias supply to increase efficiency and provide up to 5 A of output current (I_{OUT}).

The low 59 mV typical dropout voltage at a 5 A load allows the ADP1765 to operate with a small headroom while maintaining regulation and providing better efficiency.

The ADP1765 is optimized for stable operation with small 22 µF ceramic output capacitors. The ADP1765 delivers optimal transient performance with minimal printed circuit board (PCB) area.

TYPICAL APPLICATION CIRCUITS

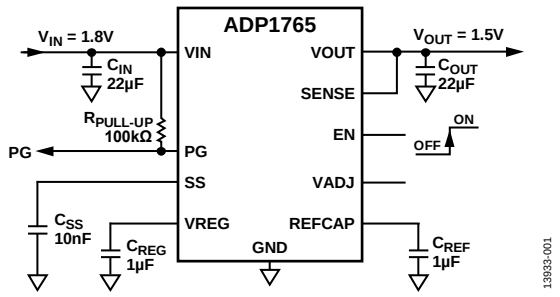

Figure 1. Fixed Output Operation

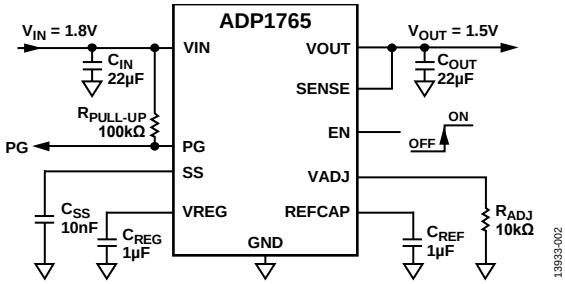

Figure 2. Adjustable Output Operation

The ADP1765 is available in fixed output voltages ranging from 0.55 V to 1.5 V. The output voltage (V_{OUT}) of the adjustable output model can be set from 0.5 V to 1.5 V through an external resistor connected between VADJ and ground.

The ADP1765 has an externally programmable soft start time by connecting a capacitor to the SS pin. Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP1765 is available in a small, 16-lead LFCSP package for the smallest footprint solution to meet a variety of applications.

Table 1. Related Devices

Model	Input Voltage	Maximum Current	Fixed/ Adjustable	Package
ADP1761	1.10 V to 1.98 V	1 A	Fixed/ adjustable	16-lead LFCSP
ADP1762	1.10 V to 1.98 V	2 A	Fixed/ adjustable	16-lead LFCSP
ADP1763	1.10 V to 1.98 V	3 A	Fixed/ adjustable	16-lead LFCSP
ADP1740/ ADP1741	1.6 V to 3.6 V	2 A	Fixed/ adjustable	16-lead LFCSP
ADP1752/ ADP1753	1.6 V to 3.6 V	0.8 A	Fixed/ adjustable	16-lead LFCSP
ADP1754/ ADP1755	1.6 V to 3.6 V	1.2 A	Fixed/ adjustable	16-lead LFCSP

Rev. A Document Feedback

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REVISION HISTORY

6/2017—Rev. 0 to Rev. A

Changed Thermal Resistance Section to Thermal Resistance/Parameter Section ... 5
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1/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{OUT} + 0.2 V or V_{IN} = 1.1 V, whichever is greater, I_{OUT} = 100 mA, C_{IN} = 22 µF, C_{OUT} = 22 µF, C_{REF} = 1 µF, C_{REG} = 1 µF, T_A = 25°C, minimum and maximum limits at T_J = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE SUPPLY RANGE	V_{IN}	T_J = −40°C to +125°C	1.10		1.98	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		5	17	mA
		I_{OUT} = 100 mA		5	18	mA
		I_{OUT} = 5 A		12	25	mA
SHUTDOWN CURRENT	I_{GND_SD}	EN = GND		4		µA
		T_J = −40°C to +85°C			200	µA
		T_J = 85°C to 125°C			900	µA
NOISE[1]						
Output Noise	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.9 V		3		µV rms
		100 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.9 V		2		µV rms
		10 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.3 V		3		µV rms
		100 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.3 V		2		µV rms
		10 Hz to 100 kHz, V_{IN} = 1.7 V, V_{OUT} = 1.5 V		3		µV rms
		100 Hz to 100 kHz, V_{IN} = 1.7 V, V_{OUT} = 1.5 V		2		µV rms
Noise Spectral Density	OUT_{NSD}	V_{OUT} = 0.55 V to 1.5 V, I_{OUT} = 100 mA				
		At 10 kHz		5		nV/√Hz
		At 100 kHz		4		nV/√Hz
POWER SUPPLY REJECTION RATIO[1]	PSRR	I_{OUT} = 5 A, modulated V_{IN}				
		10 kHz, V_{OUT} = 1.3 V, V_{IN} = 1.7 V		61		dB
		100 kHz, V_{OUT} = 1.3 V, V_{IN} = 1.7 V		43		dB
		1 MHz, V_{OUT} = 1.3 V, V_{IN} = 1.7 V		33		dB
		10 kHz, V_{OUT} = 0.9 V, V_{IN} = 1.3 V		57		dB
		100 kHz, V_{OUT} = 0.9 V, V_{IN} = 1.3 V		43		dB
		1 MHz, V_{OUT} = 0.9 V, V_{IN} = 1.3 V		33		dB
OUTPUT VOLTAGE RANGE		T_J = 25°C				
Fixed	V_{OUT_FIXED}		0.55		1.5	V
Adjustable	V_{OUT_ADJ}		0.5		1.5	V
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 100 mA, T_J = 25°C	−0.75		+0.75	%
		100 mA < I_{OUT} < 5 A, T_J = 0°C to 85°C	−1.3		+1.3	%
		100 mA < I_{OUT} < 5 A, T_J = 0°C to 125°C	−1.5		+1.5	%
ADJUSTABLE PIN CURRENT	I_{ADJ}	T_J = 25°C, V_{ADJ} = 0.5 V	49.5	50.0	50.7	µA
		V_{IN} = V_{OUT} + 0.2 V or V_{IN} = 1.1 V, whichever is greater to 1.98 V	49.0	50.0	51.2	µA
ADJUSTABLE OUTPUT VOLTAGE GAIN FACTOR	A_D	V_{ADJ} = 0.5 V; V_{IN} = V_{OUT}+ 0.2 V or V_{IN} = 1.1 V, whichever is greater, to 1.98 V				
		T_J = 25°C		2.99		
		T_J = −40°C to +125°C	2.96		3.02	
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT} + 0.2 V or V_{IN} = 1.1 V, whichever is greater, to 1.98 V	−0.10		+0.10	%/V
Load[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 mA to 5 A		0.12	0.3	%/A
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 4 A, V_{OUT} = 1.2 V		47	75	mV
		I_{OUT} = 5 A, V_{OUT} = 1.2 V		59	95	mV
START-UP TIME[1, 4]	$t_{STARTUP}$	C_{SS} = 10 nF, V_{OUT} = 1 V		1		ms
SOFT START CURRENT	I_{REF}	1.1 V ≤ V_{IN} ≤ 1.98 V	8	10	12	µA
CURRENT-LIMIT THRESHOLD[1, 5]	I_{LIMIT}		7.0	8.0	8.5	A

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
THERMAL SHUTDOWN[1]						
Threshold	TS_{SD}	T_J rising		152		°C
Hysteresis	TS_{SD_HYS}			16		°C
POWER-GOOD (PG) OUTPUT						
Output Voltage Threshold						
Falling	PG_{FALL}	$1.1\ V \le V_{IN} \le 1.98\ V$		−6.2		%
Rising	PG_{RISE}	$1.1\ V \le V_{IN} \le 1.98\ V$		−3.5		%
Output Voltage Low	PG_{LOW}	$1.1\ V \le V_{IN} \le 1.98\ V$, $I_{PG} \le 1\ mA$			0.3	V
Leakage Current	I_{PG_LKG}	$1.1\ V \le V_{IN} \le 1.98\ V$		0.01	1	µA
Delay	PG_{DELAY}	EN_{RISING} to PG_{RISING}		0.75		ms
PRECISION EN INPUT		$1.1\ V \le V_{IN} \le 1.98\ V$				
Logic Input Voltage						
High	EN_{HIGH}		0.60	0.65	0.69	V
Low	EN_{LOW}		0.55	0.60	0.65	V
Input Logic Hysteresis	EN_{HYS}			50		mV
Input Leakage Current	I_{EN_LKG}	$V_{EN} = V_{IN}$ or GND		0.01	1	µA
Input Delay Time	t_{EN_DLY}	From EN rising from 0 V to V_{IN} to $0.1 \times V_{OUT}$		100		µs
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage						
Rising	$UVLO_{RISE}$	$T_J = -40°C$ to $+125°C$		1.00	1.06	V
Falling	$UVLO_{FALL}$	$T_J = -40°C$ to $+125°C$	0.85	0.93		V
Hysteresis	$UVLO_{HYS}$			70		mV

[1] Guaranteed by characterization but not production tested.
[2] Based on an endpoint calculation using 100 mA and 5 A loads.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage, which applies only for output voltages above 1.1 V.
[4] Start-up time is the time from the rising edge of V_{EN} to V_{OUT} being at 90% of its nominal value.
[5] Current-limit threshold is the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

INPUT AND OUTPUT CAPACITOR: RECOMMENDED SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE[1]		$T_A = -40°C$ to $+125°C$				
Input	C_{IN}		14.5	22		µF
Output	C_{OUT}		14.5	22		µF
Regulator	C_{REG}		0.7	1		µF
Reference	C_{REF}		0.07	1		µF
CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR)	R_{ESR}	$T_A = -40°C$ to $+125°C$				
C_{IN}, C_{OUT}					0.2	Ω
C_{REG}					0.5	Ω
C_{REF}					2	Ω

[1] The minimum input and output capacitance must be >14.5 µF over the full range of the operating conditions. Consider the full range of the operating conditions in the application during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended. Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN to GND	−0.3 V to +2.16 V
EN to GND	−0.3 V to +3.96 V
VOUT to GND	−0.3 V to V_{IN}
SENSE to GND	−0.3 V to V_{IN}
VREG to GND	−0.3 V to V_{IN}
REFCAP to GND	−0.3 V to V_{IN}
VADJ to GND	−0.3 V to V_{IN}
SS to GND	−0.3 V to V_{IN}
PG to GND	−0.3 V to +3.96 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Operating Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP1765 can be damaged when the junction temperature limits are exceeded. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 4.

Use the following equation to calculate the junction temperature (T_J) from the board temperature (T_{BOARD}) or package top temperature (T_{TOP})

$$T_J = T_{BOARD} + (P_D \times \Psi_{JB})$$

$$T_J = T_{TOP} + (P_D \times \Psi_{JT})$$

Ψ_{JB} is the junction to board thermal characterization parameter and Ψ_{JT} is the junction to top thermal characterization parameter with units of °C/W.

Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications.

THERMAL RESISTANCE/PARAMETER

Values shown in Table 5 are calculated in compliance with JEDEC standards for thermal reporting. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance. θ_{JB} is the junction to board thermal resistance. Ψ_{JB} is the junction to board thermal characterization parameter. Ψ_{JT} is the junction to top thermal characterization parameter.

In applications where high maximum power dissipation exists, close attention to thermal board design is required. Thermal resistance/parameter values may vary, depending on the PCB material, layout, and environmental conditions.

Table 5. Thermal Resistance/Parameter

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
CP-16-48[1]	40.65	7.47	17.38	12.9	0.85	°C/W

[1] Thermal resistance/parameter simulated values are based on a JEDEC 2S2P thermal test board for Ψ_{JT}, Ψ_{JB}, θ_{JA} and θ_{JB} and a JEDEC 1S0P thermal test board for θ_{JC} with four thermal vias. See JEDEC JESD51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

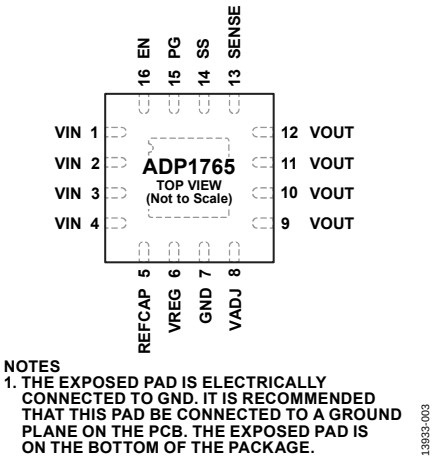

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	VIN	Regulator Input Supply. Bypass VIN to GND with a 22 µF or greater capacitor. Note that all four VIN pins must be connected to the source supply.
5	REFCAP	Reference Filter Capacitor. Connect a 1 µF capacitor from the REFCAP pin to ground. Do not connect a load from this pin to ground.
6	VREG	Regulated Input Supply to LDO Amplifier. Bypass VREG to GND with a 1 µF or greater capacitor. Do not connect a load from this pin to ground.
7	GND	Ground.
8	VADJ	Adjustable Voltage Pin for the Adjustable Output Option. Connect a 10 kΩ external resistor between the VADJ pin and ground to set the output voltage to 1.5 V. For the fixed output option, leave this pin floating.
9 to 12	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 22 µF or greater capacitor. Note that all four VOUT pins must be connected to the load.
13	SENSE	Sense Input. The SENSE pin measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close to the load as possible to minimize the effect of IR drop between VOUT and the load.
14	SS	Soft Start Pin. A capacitor connected to this pin determines the soft start time.
15	PG	Power-Good Output. This open-drain output requires an external pull-up resistor. If the device is in shutdown mode, current-limit mode, or thermal shutdown mode, or if the V_{OUT} voltage falls below 90% of the nominal output voltage, the PG pin immediately transitions to low.
16	EN	Enable Input. Drive the EN pin high to turn on the regulator. Drive the EN pin low to turn off the regulator. For automatic startup, connect the EN pin to the VIN pin.
	EP	Exposed Pad. The exposed pad is electrically connected to GND. It is recommended that this pad be connected to a ground plane on the PCB. The exposed pad is on the bottom of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{OUT} + 0.2 V or V_{IN} = 1.1 V, whichever is greater, V_{OUT} = 1.3 V, I_{OUT} = 100 mA, T_A = 25°C, unless otherwise noted.

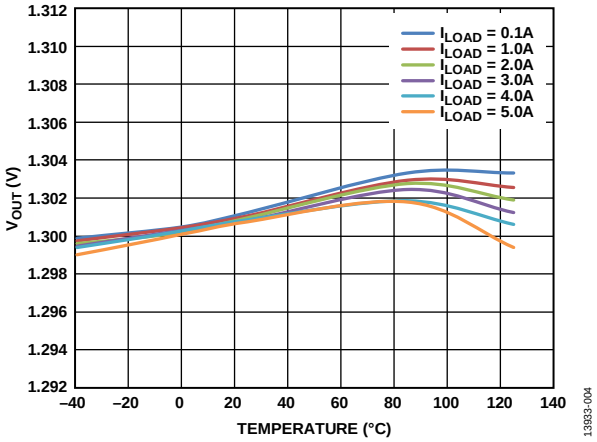

Figure 4. Output Voltage (V_{OUT}) vs. Temperature, V_{OUT} = 1.3 V

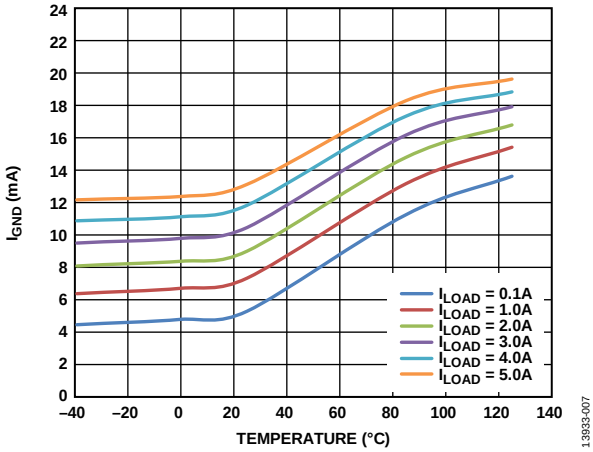

Figure 7. Ground Current (I_{GND}) vs. Temperature, V_{OUT} = 1.3 V

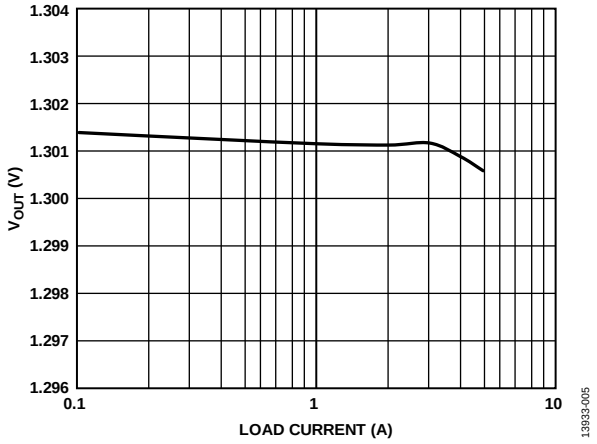

Figure 5. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 1.3 V

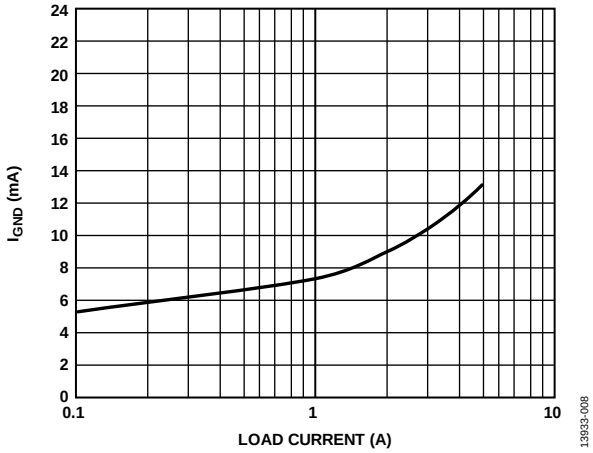

Figure 8. Ground Current (I_{GND}) vs. Load Current (I_{LOAD}), V_{OUT} = 1.3 V

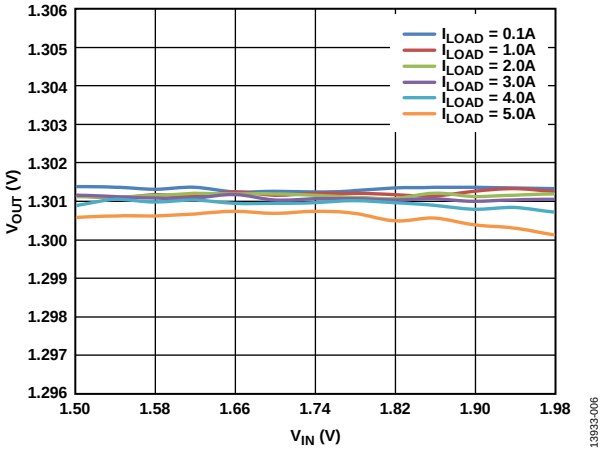

Figure 6. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 1.3 V

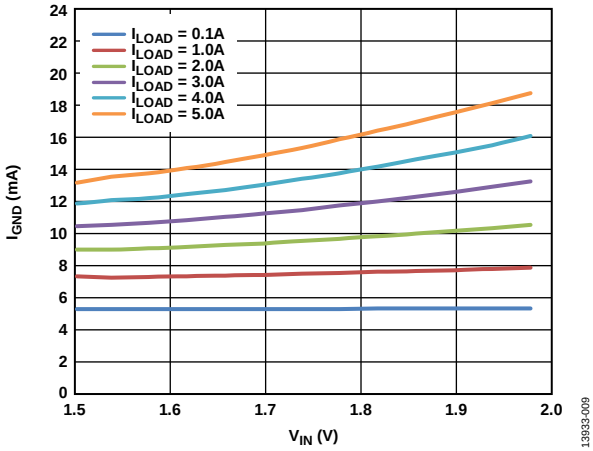

Figure 9. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}), V_{OUT} = 1.3 V

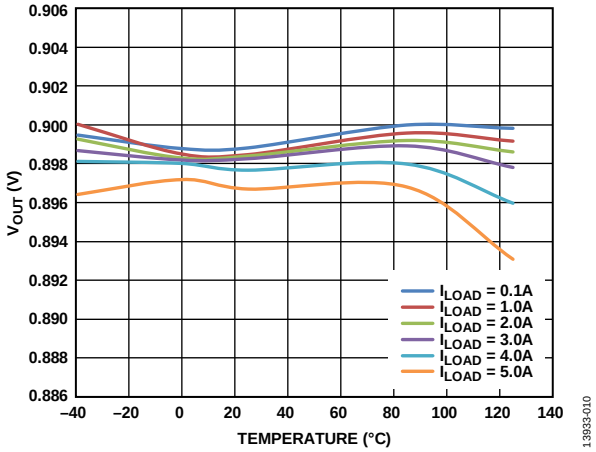

Figure 10. Output Voltage (V_{OUT}) vs. Temperature, V_{OUT} = 0.9 V

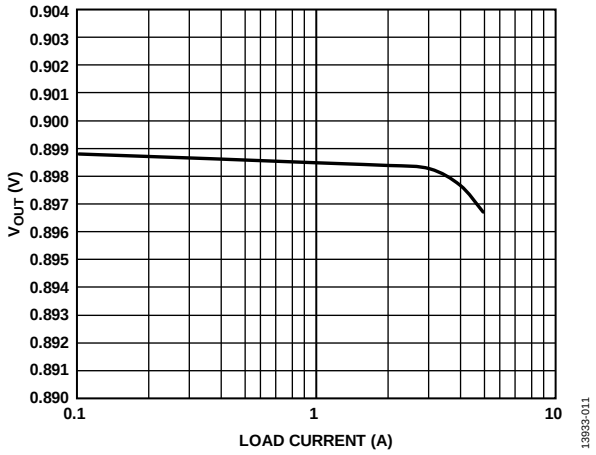

Figure 11. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 0.9 V

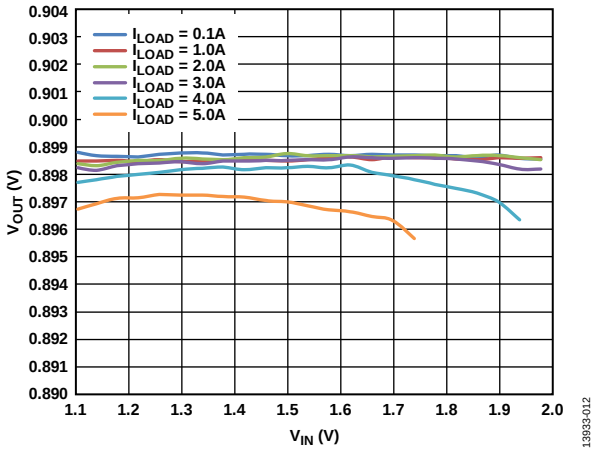

Figure 12. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 0.9 V

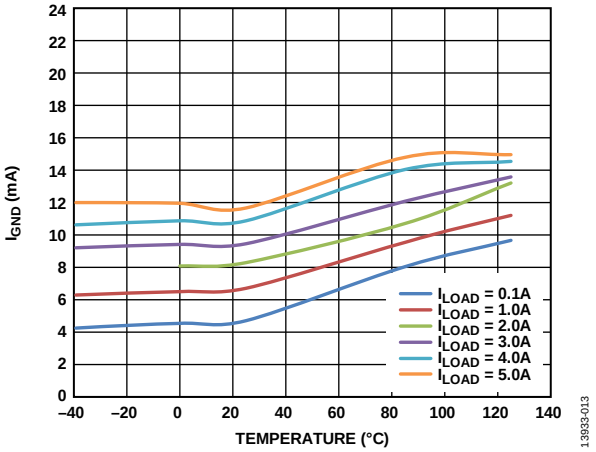

Figure 13. Ground Current (I_{GND}) vs. Temperature, V_{OUT} = 0.9 V

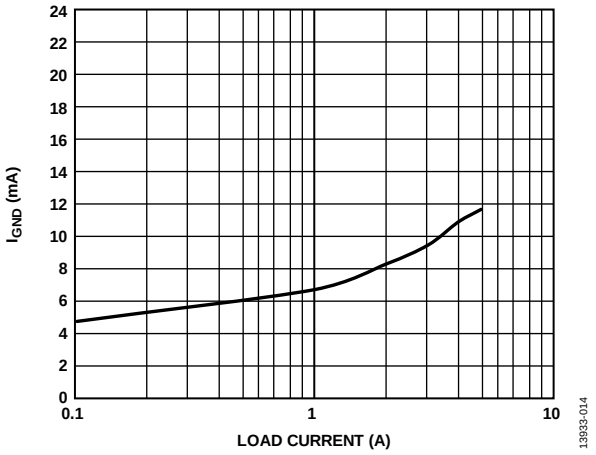

Figure 14. Ground Current (I_{GND}) vs. Load Current (I_{LOAD}), V_{OUT} = 0.9 V

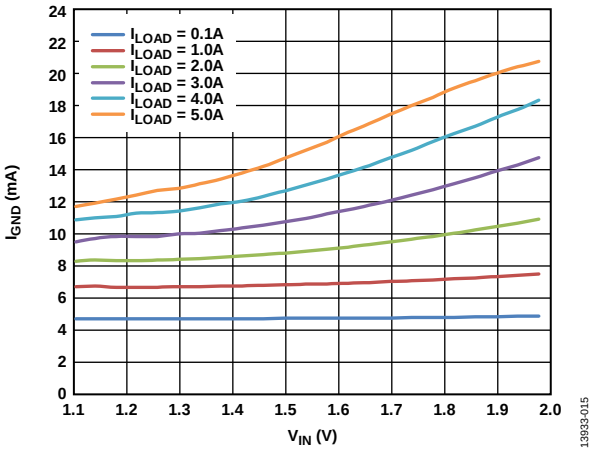

Figure 15. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}), V_{OUT} = 0.9 V

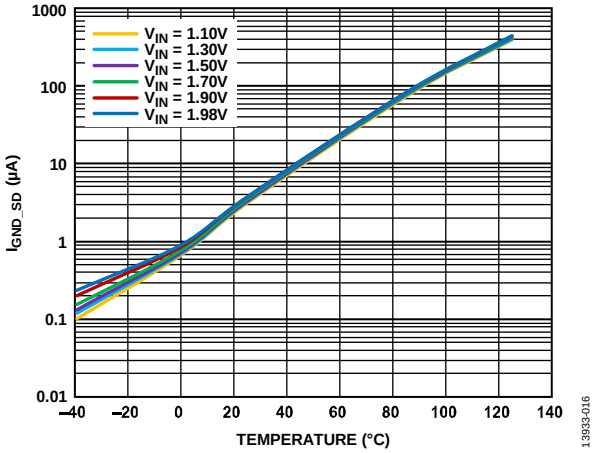

Figure 16. Shutdown Current (I_{GND_SD}) vs. Temperature at Various Input Voltages (V_{IN}), V_{OUT} = 0.9 V

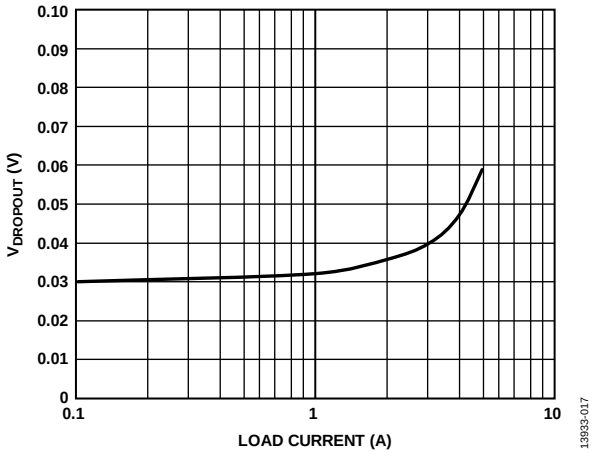

Figure 17. Dropout Voltage ($V_{DROPOUT}$) vs. Load Current (I_{LOAD}), V_{OUT} = 1.3 V

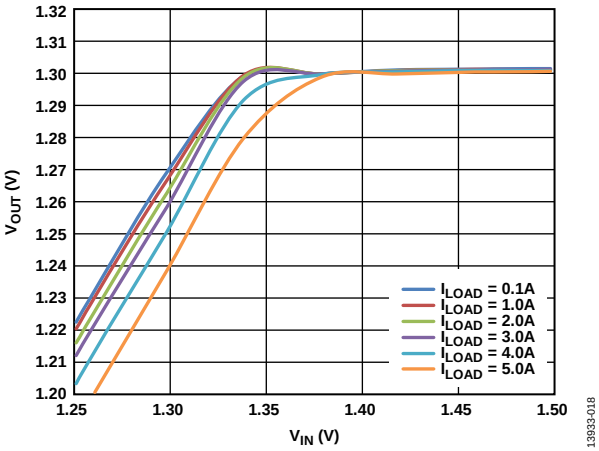

Figure 18. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 1.3 V

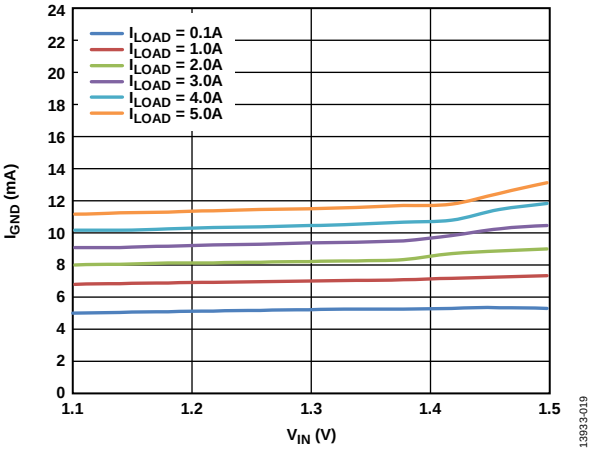

Figure 19. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 1.3 V

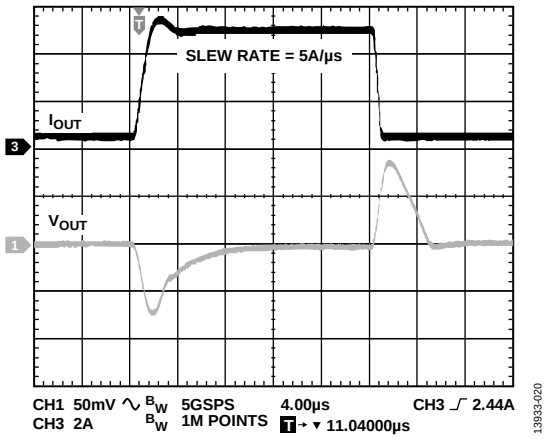

Figure 20. Load Transient Response, C_{OUT} = 22 µF, V_{IN} = 1.8 V, V_{OUT} = 1.3 V

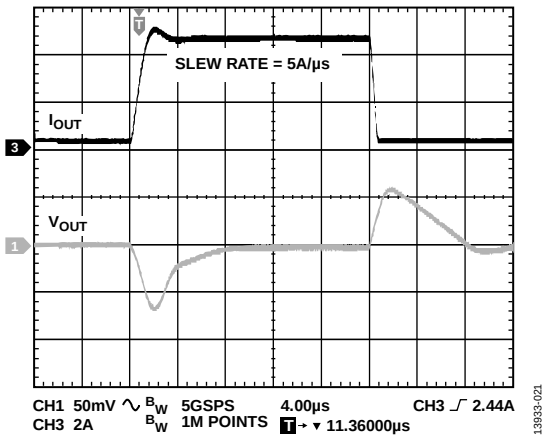

Figure 21. Load Transient Response, C_{OUT} = 47 µF, V_{IN} = 1.8 V, V_{OUT} = 1.3 V

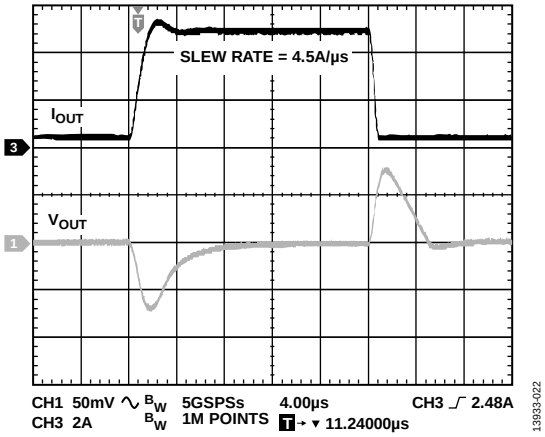

Figure 22. Load Transient Response, C_{OUT} = 22 µF, V_{IN} = 1.4 V, V_{OUT} = 0.9 V

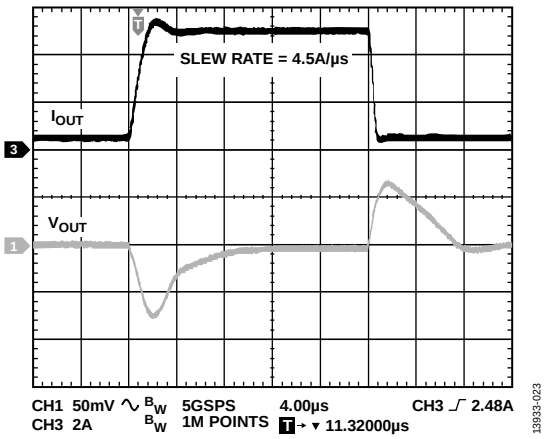

Figure 23. Load Transient Response, C_{OUT} = 47 µF, V_{IN} = 1.4 V, V_{OUT} = 0.9 V

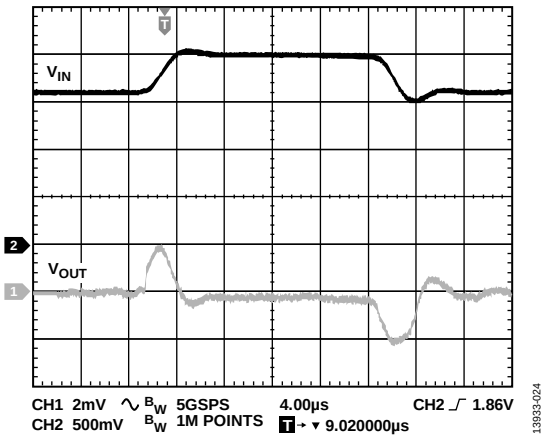

Figure 24. Line Transient Response, Load Current = 5 A, V_{IN} = 1.6 V to 1.98 V Step, V_{OUT} = 1.3 V

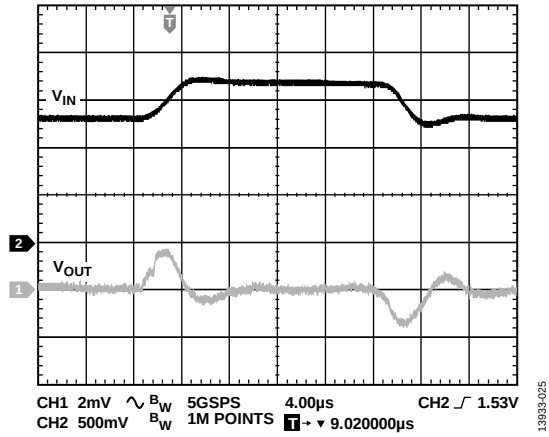

Figure 25. Line Transient Response, Load Current = 5 A, V_{IN} = 1.3 V to 1.7 V Step, V_{OUT} = 0.9 V

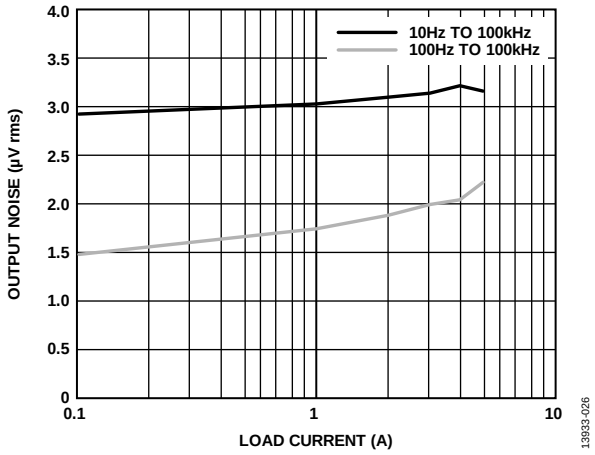

Figure 26. Output Noise vs. Load Current (I_{LOAD})

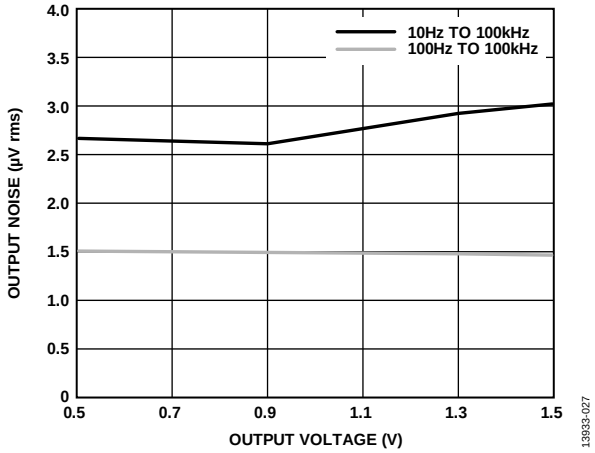

Figure 27. Output Noise vs. Output Voltage (V_{OUT})

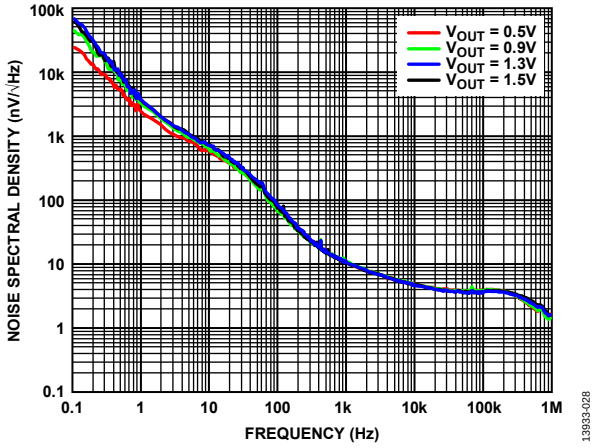

Figure 28. Noise Spectral Density vs. Frequency at Various Output Voltages (V_{OUT}), 0.1 Hz to 1 MHz

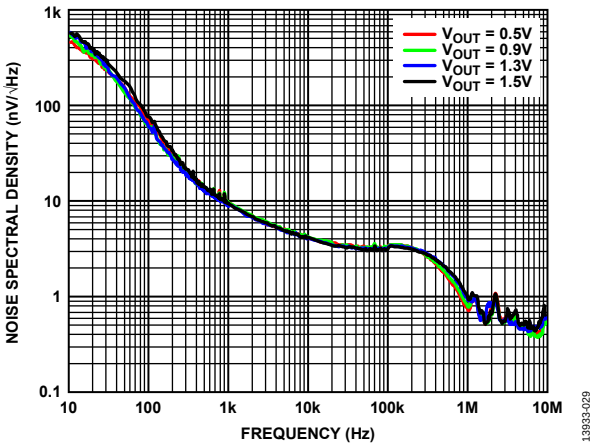

Figure 29. Noise Spectral Density vs. Frequency at Various Output Voltages (V_{OUT}), 10 Hz to 10 MHz

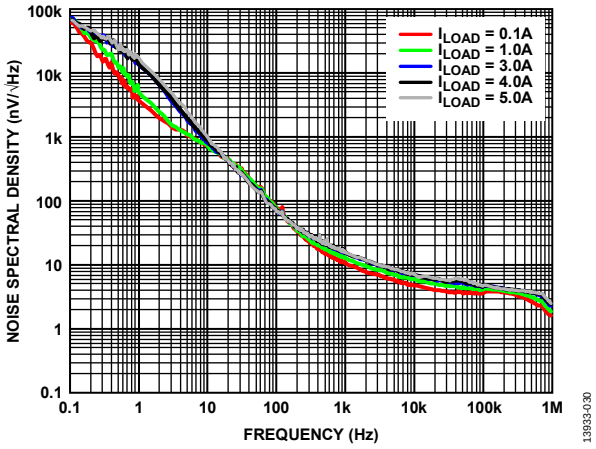

Figure 30. Noise Spectral Density vs. Frequency at Various Load Current (I_{OUT}), 0.1 Hz to 1 MHz

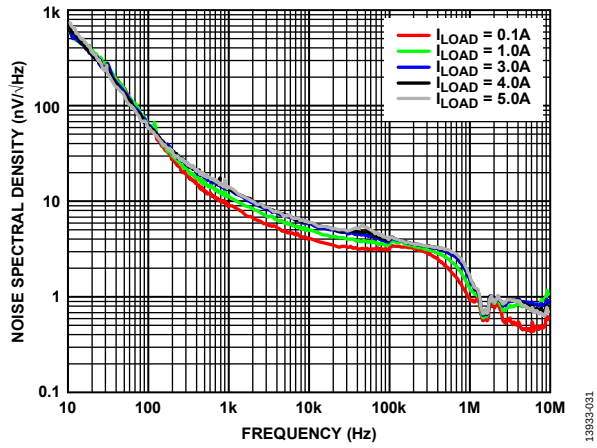

Figure 31. Noise Spectral Density vs. Frequency at Various Load Current (I_{OUT}), 10 Hz to 10 MHz

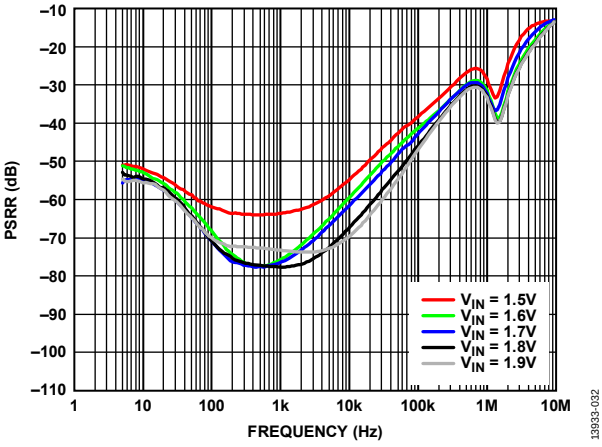

Figure 32. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Input Voltages (V_{IN}), V_{OUT} = 1.3 V, Load = 5 A

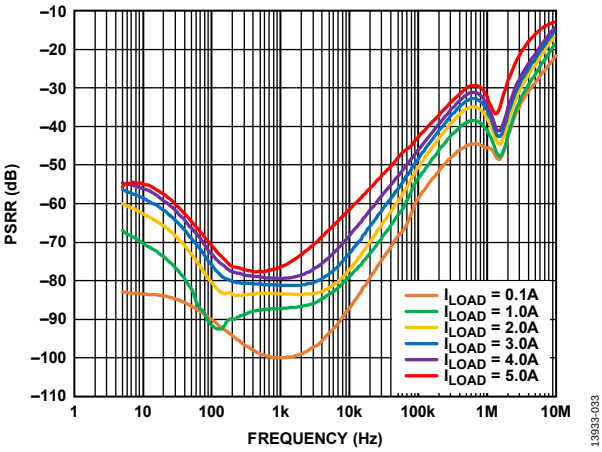

Figure 33. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads (I_{LOAD}), V_{OUT} = 1.3 V, V_{IN} = 1.7 V

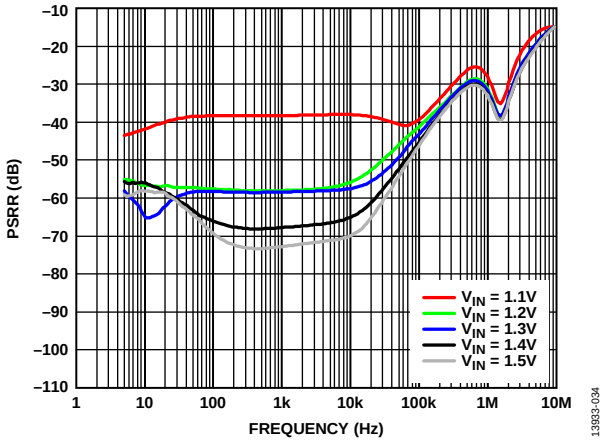

Figure 34. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Input Voltages (V_{IN}), V_{OUT} = 0.9 V, Load = 5 A

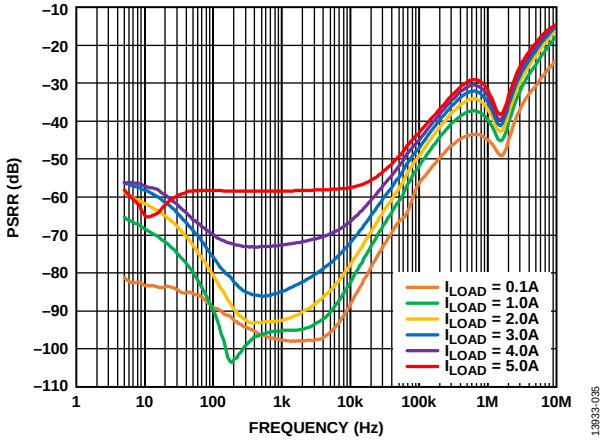

Figure 35. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads (I_{LOAD}), V_{OUT} = 0.9 V, V_{IN} = 1.3 V

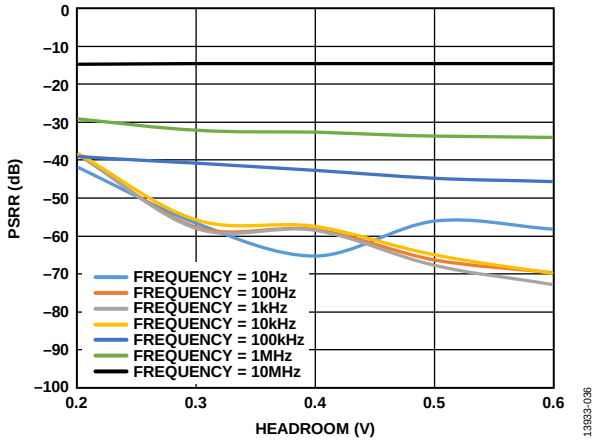

Figure 36. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage at Various Frequencies, V_{OUT} = 0.9 V, Load = 5 A

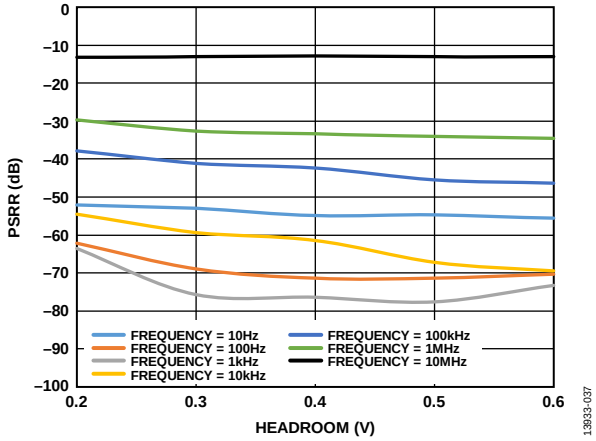

Figure 37. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage at Various Frequencies, V_{OUT} = 1.3 V, Load = 5 A

THEORY OF OPERATION

The ADP1765 is a low dropout (LDO), low noise linear regulator that uses an advanced proprietary architecture to achieve high efficiency regulation. It also provides high PSRR and excellent line and load transient response using a small 22 µF ceramic output capacitor. The device operates from a 1.10 V to 1.98 V input rail to provide up to 5 A of output current. The supply current in shutdown mode is less than 4 µA.

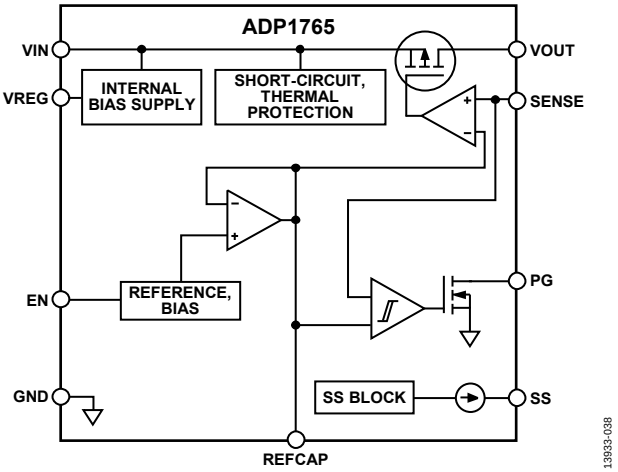

Figure 38. Functional Block Diagram, Fixed Output

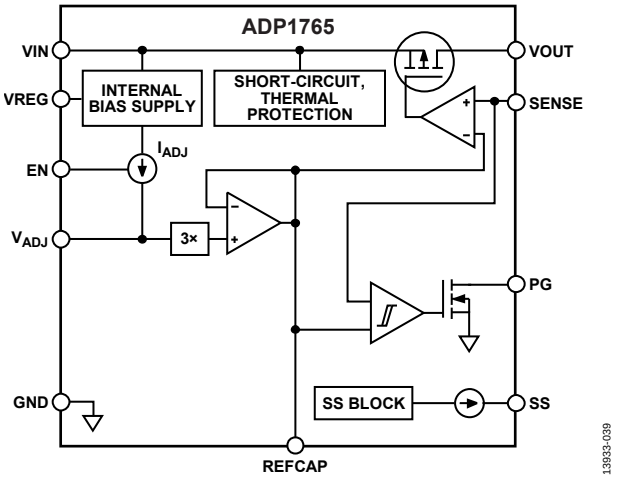

Figure 39. Functional Block Diagram, Adjustable Output

Internally, the ADP1765 consists of a reference, an error amplifier, and a pass device. The output current is delivered via the pass device, which is controlled by the error amplifier, forming a negative feedback system that ideally drives the feedback voltage to equal the reference voltage. If the feedback voltage is lower than the reference voltage, the negative feedback drives more current, increasing the output voltage. If the feedback voltage is higher than the reference voltage, the negative feedback drives less current, decreasing the output voltage.

The ADP1765 is available in output voltages ranging from 0.55 V to 1.5 V for a fixed output. Contact your local Analog Devices, Inc., sales representative for other fixed voltage options. The adjustable output option can be set from 0.5 V to 1.5 V. The ADP1765 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on. When EN is low, VOUT turns off. For automatic startup, tie EN to VIN.

SOFT START FUNCTION

For applications that require a controlled startup, the ADP1765 provides a programmable soft start function. The programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement soft start, connect a small ceramic capacitor from SS to GND. At startup, a 10 µA current source charges this capacitor. The voltage at SS limits the ADP1765 start-up output voltage, providing a smooth ramp up to the nominal output voltage. To calculate the start-up time for the fixed output ($t_{STARTUP\_FIXED}$) and adjustable ($t_{STARTUP\_ADJ}$) output, use the following equations:

$$t_{STARTUP\_FIXED} = t_{DELAY} + V_{REF} \times (C_{SS}/I_{SS}) \quad (1)$$

$$t_{STARTUP\_ADJ} = t_{DELAY} + V_{ADJ} \times (C_{SS}/I_{SS}) \quad (2)$$

where:

t_{DELAY} is a fixed delay of 100 µs.
V_{REF} is a 0.5 V internal reference for the fixed output model option.
C_{SS} is the soft start capacitance from SS to GND.
I_{SS} is the current sourced from SS (10 µA).
V_{ADJ} is the voltage at the VADJ pin, equal to $R_{ADJ} \times I_{ADJ}$.

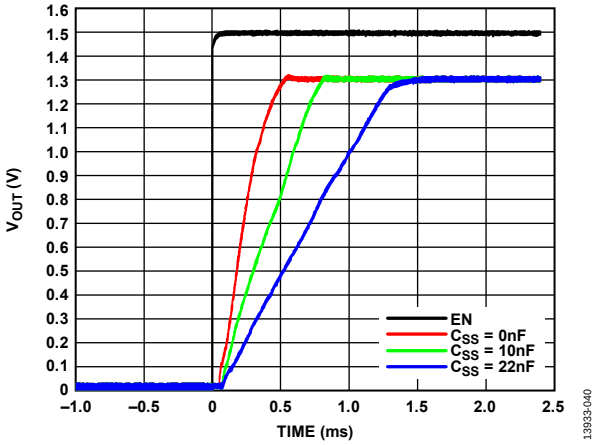

Figure 40. Fixed V_{OUT} Ramp-Up with External Soft Start Capacitor ($V_{OUT, EN}$) vs. Time

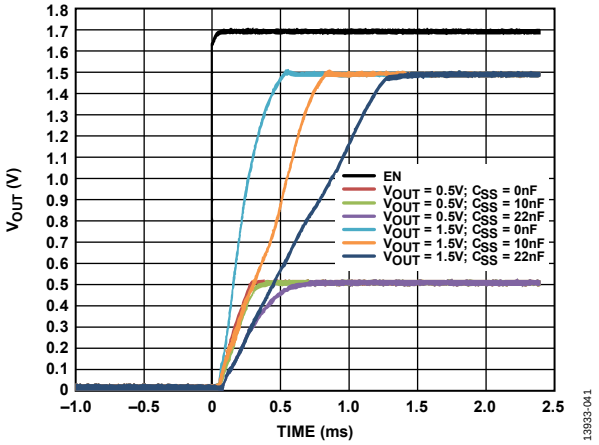

Figure 41. Adjustable V_{OUT} Ramp-Up with External Soft Start Capacitor ($V_{OUT, EN}$) vs. Time

ADJUSTABLE OUTPUT VOLTAGE

The output voltage of the ADP1765 can be set over a 0.5 V to 1.5 V range. Connect a resistor (R_{ADJ}) from the VADJ pin to ground to set the output voltage. To calculate the output voltage (V_{OUT}), use the following equation:

$$V_{OUT} = A_D \times (R_{ADJ} \times I_{ADJ}) \quad (3)$$

where:

A_D is the gain factor with a typical value of 2.99 between the VADJ pin and VOUT pin.

I_{ADJ} is the 50 µA constant current out of the VADJ pin.

ENABLE FEATURE

The ADP1765 uses the EN pin to enable and disable the VOUT pins under normal operating conditions. As shown in Figure 42, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

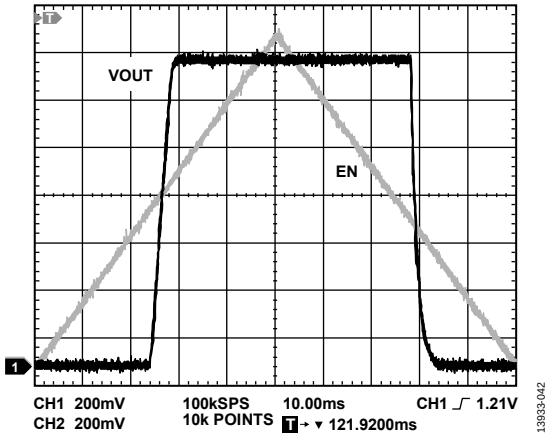

Figure 42. Typical EN Pin Operation

As shown in Figure 43, the EN pin has built in hysteresis. This hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

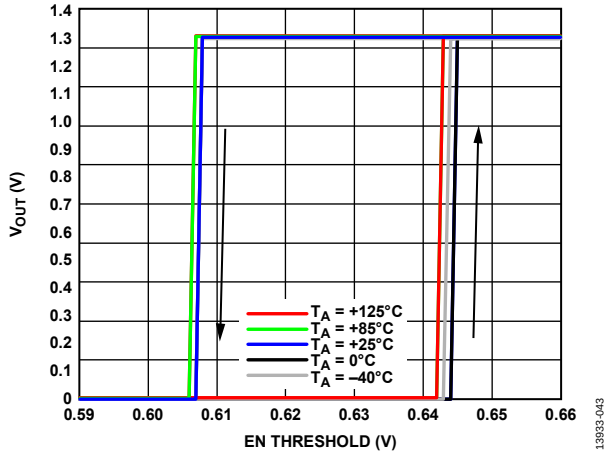

Figure 43. Output Voltage (V_{OUT}) vs. EN Threshold, V_{OUT} = 1.3 V

POWER-GOOD (PG) FEATURE

The ADP1765 provides a power-good pin (PG) to indicate the status of the output. This open-drain output requires an external pull-up resistor that can be connected to VIN or VOUT. If the device is in shutdown mode, current-limit mode, or thermal shutdown, or if it falls below 90% of the nominal output voltage, PG immediately transitions low. During soft start, the rising threshold of the power-good signal is 96.5% of the nominal output voltage.

The open-drain output is held low when the ADP1765 has sufficient input voltage to turn on the internal PG transistor. An optional soft start delay can be detected. The PG transistor is terminated via a pull-up resistor to VIN or VOUT.

Power-good accuracy is 93.8% of the nominal regulator output voltage when this voltage is rising, with a 96.5% trip point when this voltage is falling.

Regulator input voltage brownouts or glitches trigger a power no good if VOUT falls below 93.8%.

A normal power-down triggers a power good when V_{OUT} is at 96.5%.

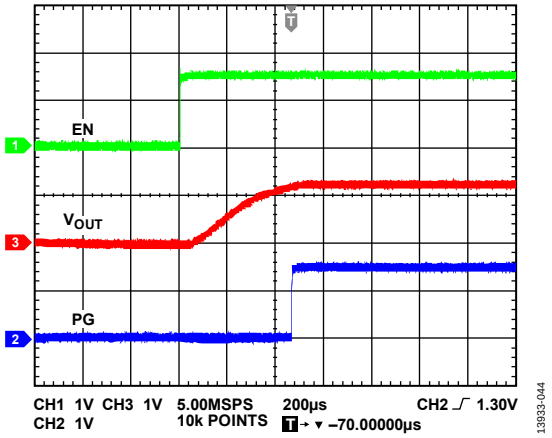

Figure 44. Typical PG Voltage Behavior vs. V_{OUT}, V_{IN} Rising (V_{OUT} = 1.3 V)

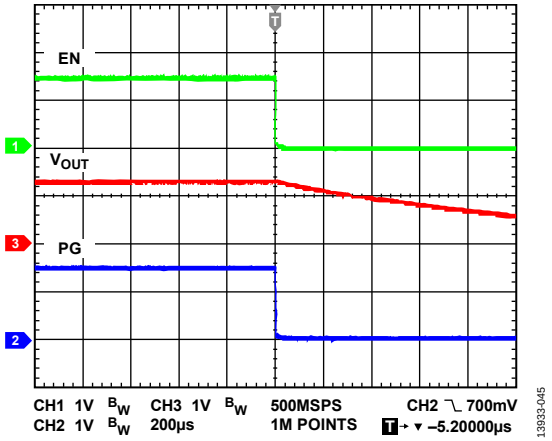

Figure 45. Typical PG Voltage Behavior vs. V_{OUT}, V_{IN} Falling (V_{OUT} = 1.3 V)

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1765 is designed for operation with small, space-saving ceramic capacitors, but it can function with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 22 µF capacitance with an ESR of 50 mΩ or less is recommended to ensure the stability of the ADP1765. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1765 to large changes in load current. Figure 46 and Figure 47 show the transient responses for output capacitance values of 22 µF and 47 µF, respectively.

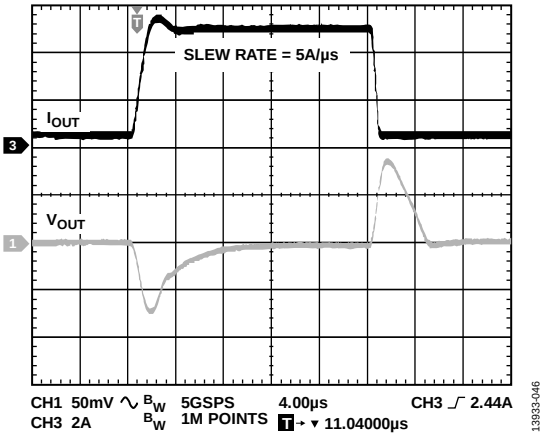

Figure 46. Output Transient Response, C_{OUT} = 22 µF, V_{OUT} = 1.3 V

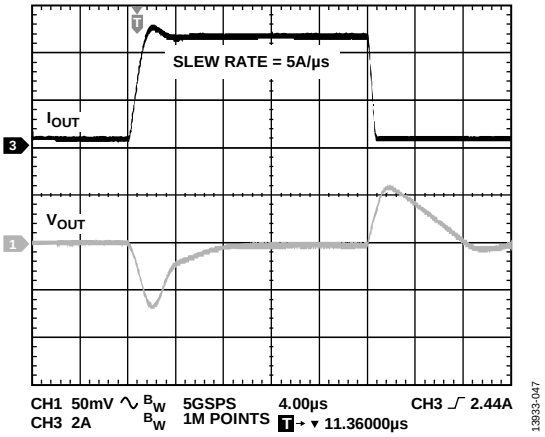

Figure 47. Output Transient Response, C_{OUT} = 47 µF, V_{OUT} = 1.3 V

Input Bypass Capacitor

Connecting a 22 µF capacitor from the VIN pin to the GND pin to the ground plane reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedances are encountered. If an output capacitance greater than 22 µF is required, it is recommended to increase the input capacitor to match it.

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP1765 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 48 shows the capacitance vs. dc bias voltage characteristics of a C2012X5R1A226K125AB, 0805 case, 22 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits improved stability. The temperature variation of the X5R dielectric is about ±15% over the −55°C to +85°C temperature range and is not a function of package size or voltage rating.

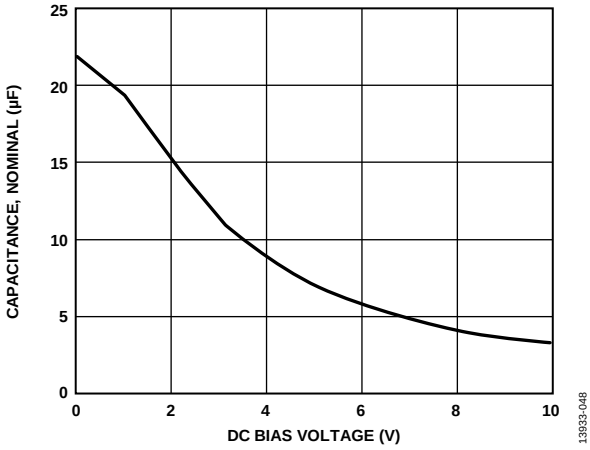

Figure 48. Capacitance vs. DC Bias Voltage

Use Equation 4 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL) \quad (4)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
C_{OUT} is the output capacitor.
TEMPCO is the worst case capacitor temperature coefficient.
TOL is the worst case component tolerance.

In this example, the worst case temperature coefficient (TEMPCO) over −55°C to +125°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} = 19.48 µF at 1.0 V, as shown in Figure 48.

Substituting these values in Equation 4 yields

$$C_{EFF} = 19.48\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 14.9\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP1765, it is imperative to evaluate the effects of dc bias, temperature, and tolerances on the behavior of the capacitors for each application.

UNDERVOLTAGE LOCKOUT

The ADP1765 has an internal undervoltage lockout (UVLO) circuit that disables all inputs and the output when the input voltage is less than approximately 1.06 V. The UVLO ensures that the ADP1765 inputs and output behave in a predictable manner during power-up.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1765 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP1765 is designed to reach the current limit when the output load reaches 8.0 A (typical). When the output load exceeds 8.0 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included that limits the junction temperature to a maximum of 152°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature begins to rise above 152°C, the output turns off, reducing the output current to zero. When the junction temperature drops below 136°C (typical), the output turns on again, and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP1765 reaches the current limit so that only 8.0 A is conducted into the short. If self-heating of the junction becomes great enough to cause its temperature to rise above 152°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 136°C, the output turns on and conducts 8.0 A into the short, again causing the junction temperature to rise above 152°C. This thermal oscillation between 136°C and 152°C causes a current oscillation between 8.0 A and 0 A that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

PARALLELING ADP1765 DEVICES FOR HIGH CURRENT APPLICATIONS

In applications where high output current is required while maintaining low noise and high PSRR performance, connect two ADP1765 devices in parallel to handle loads up to 9 A.

When paralleling theADP1765, the two outputs must be of the same voltage setting to maintain good current sharing between the two LDOs. To improve current sharing accuracy, add identical ballast resistors ($R_{BALLAST}$) at the output of each regulator, as shown in Figure 49. Note that large ballast resistors improve current sharing accuracy, but degrade the load regulation performance and increase the losses along the power line. Therefore, it is best to keep the ballast resistors at a minimum. In addition, tie the VADJ, SS, and REFCAP pins of the LDO regulators together to minimize error between the two outputs.

Use Equation 5 to calculate the output of the two paralleled ADP1765 LDOs.

$$V_{OUT} = 2 \times A_D \times (R_{ADJ} \times I_{ADJ}) \quad (5)$$

where:
A_D is the gain factor with a typical value of 2.99 between the VADJ pin and VOUT pin.
I_{ADJ} is the 50 µA constant current out of the VADJ pin.

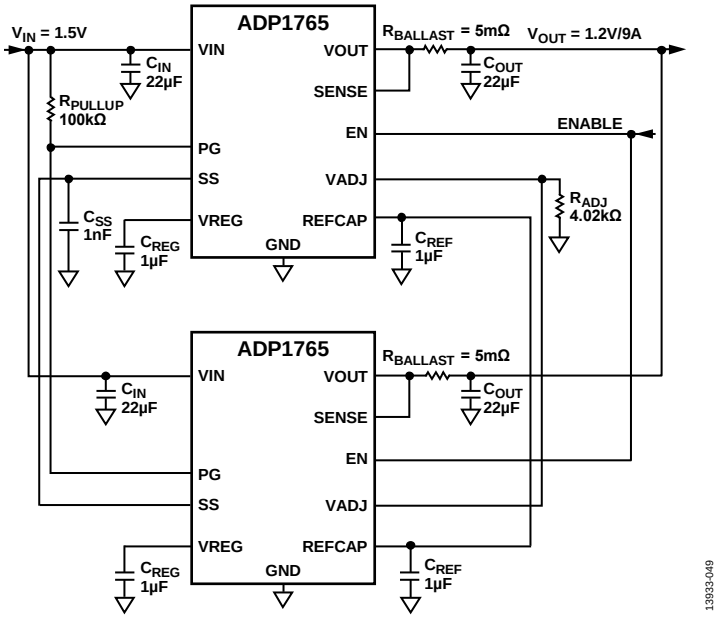

Figure 49. Two ADP1765 Devices Connected in Parallel to Achieve Higher Current Output

THERMAL CONSIDERATIONS

In applications with a low input-to-output voltage differential, the ADP1765 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough to cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 152°C, the regulator enters thermal shutdown. The regulator recovers only after the junction temperature decreases below 136°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the board temperature and the temperature rise of the package due to the power dissipation, as shown in Equation 6.

To guarantee reliable operation, the junction temperature of the ADP1765 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include board temperature, power dissipation in the power device, and thermal characterization parameter between the junction and board (Ψ_{JB}). The Ψ_{JB} parameter is dependent on the package assembly compounds and the PCB copper area. Table 7 shows the typical Ψ_{JB} values for the 16-lead LFCSP package for various PCB copper areas.

Table 7. Typical non-JEDEC Ψ_{JB} Values

PCB Copper Area (mm²)	Ψ_{JB} (°C/W) at 2W
25	71.05
100	18.9
500	13.45
1000	13.15

Calculate the junction temperatures of the ADP1765 by

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (6)$$

where:
T_B is the board temperature.
P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{OUT}) \times I_{LOAD}) + (V_{IN} \times I_{GND}) \quad (7)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_B + (((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \Psi_{JB}) \quad (8)$$

As shown in Equation 8, for a given board temperature, input-to-output voltage differential and continuous load current, a minimum copper area requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C.

Figure 50 to Figure 55 show the junction temperature calculations for the different board temperatures, power dissipation, and areas of the PCB copper.

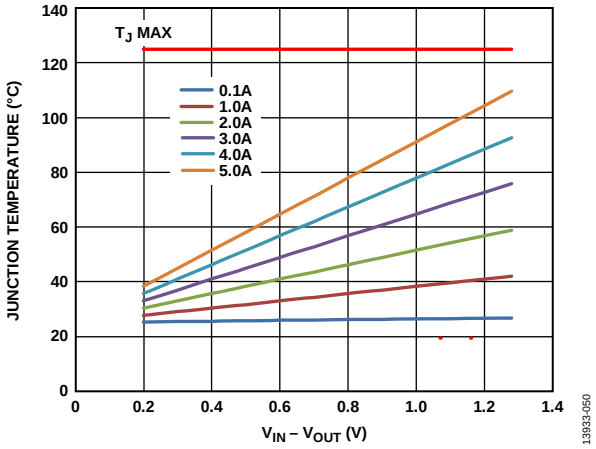

Figure 50. 1000 mm² of PCB Copper, T_B = 25°C

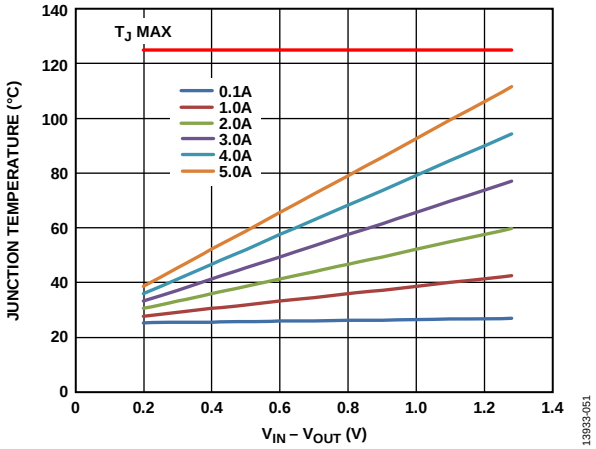

Figure 51. 500 mm² of PCB Copper, T_B = 25°C

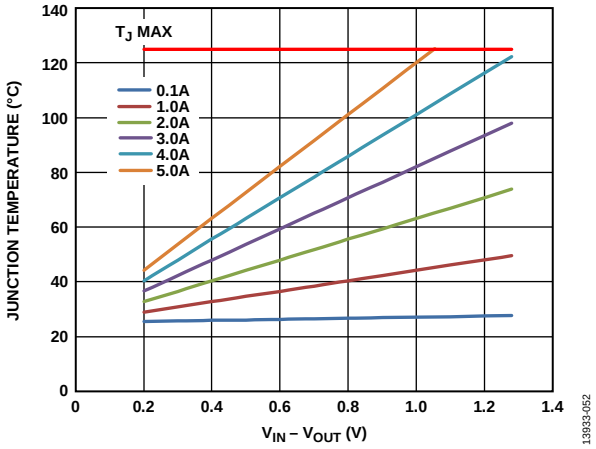

Figure 52. 100 mm² of PCB Copper, T_B= 25°C

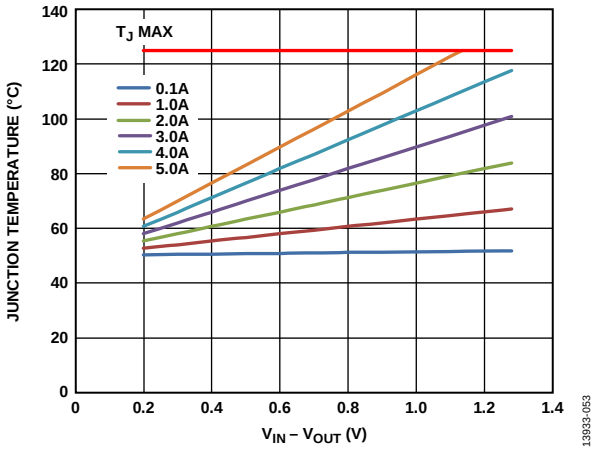

Figure 53. 1000 mm² of PCB Copper, T_B = 50°C

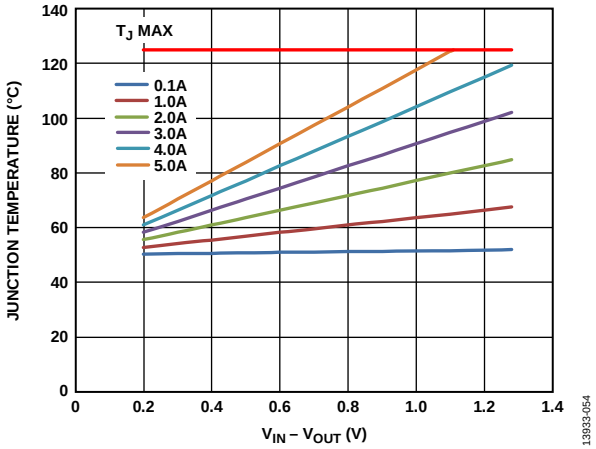

Figure 54. 500 mm² of PCB Copper, T_B = 50°C

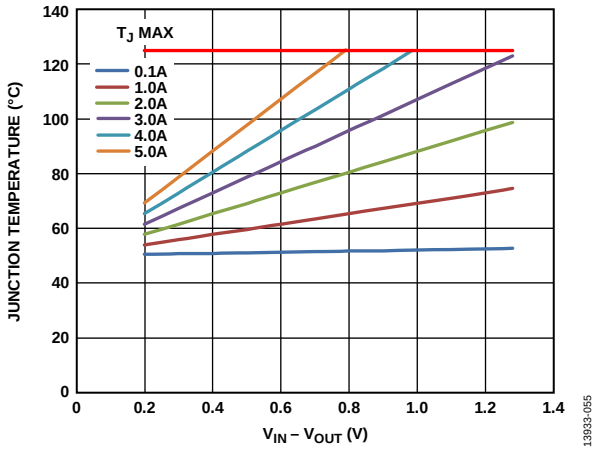

Figure 55. 100 mm² of PCB Copper, T_B = 50°C

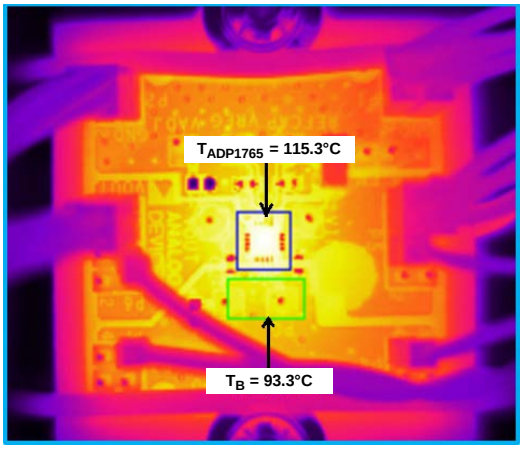

Figure 56. Thermal Image of the ADP1765 Evaluation Board at I_{LOAD} = 5 A, V_{IN} = 1.5 V, V_{OUT} = 1.3 V, T_B = 93.3°C

Figure 56 shows a thermal image of the ADP1765 evaluation board operating at a 5 A current load. The total power dissipation on the ADP1765 is 933 mW, which makes the temperature on the surface of the device higher by 22°C than the temperature of the evaluation board.

PCB LAYOUT CONSIDERATIONS

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Place the soft start capacitor (C_{SS}) as close as possible to the SS pin. Place the reference capacitor (C_{REF}) and regulator capacitor (C_{REG}) as close as possible to the REFCAP pin and VREG pin, respectively. Connect the load as close as possible to the VOUT and SENSE pins.

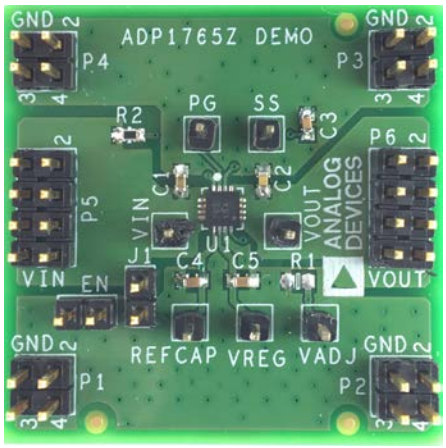

Figure 57. Evaluation Board

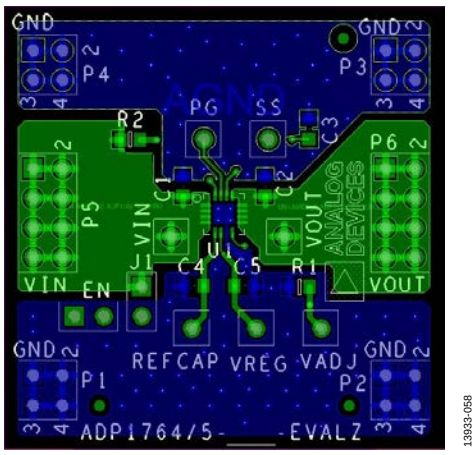

Figure 58. Typical Board Layout, Top Side

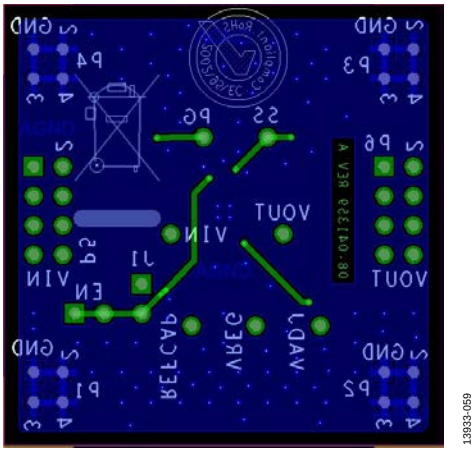

Figure 59. Typical Board Layout, Bottom Side

OUTLINE DIMENSIONS

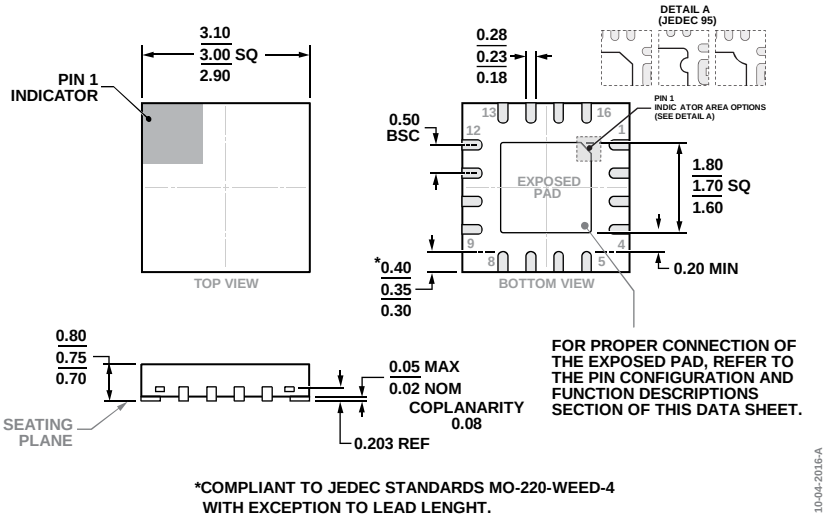

Figure 60. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP1765ACPZ0.85-R7	−40°C to +125°C	0.85	16-Lead LFCSP	CP-16-48	LUA
ADP1765ACPZ-0.9-R7	−40°C to +125°C	0.9	16-Lead LFCSP	CP-16-48	LUB
ADP1765ACPZ0.95-R7	−40°C to +125°C	0.95	16-Lead LFCSP	CP-16-48	LUM
ADP1765ACPZ-1.0-R7	−40°C to +125°C	1.0	16-Lead LFCSP	CP-16-48	LUD
ADP1765ACPZ-1.1-R7	−40°C to +125°C	1.1	16-Lead LFCSP	CP-16-48	LUE
ADP1765ACPZ-1.2-R7	−40°C to +125°C	1.2	16-Lead LFCSP	CP-16-48	LUF
ADP1765ACPZ1.25-R7	−40°C to +125°C	1.25	16-Lead LFCSP	CP-16-48	LUR
ADP1765ACPZ-1.3-R7	−40°C to +125°C	1.3	16-Lead LFCSP	CP-16-48	LUG
ADP1765ACPZ-1.5-R7	−40°C to +125°C	1.5	16-Lead LFCSP	CP-16-48	LUJ
ADP1765ACPZ-R7	−40°C to +125°C	Adjustable	16-Lead LFCSP	CP-16-48	LUK
ADP1765-1.0-EVALZ		1.0	Evaluation Board (Fixed)		
ADP1765-ADJ-EVALZ		1.0	Evaluation Board (Adjustable)		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local Analog Devices sales or distribution representative. Additional voltage options are available by special order and include the following: 0.55 V, 0.6 V, 0.65 V, 0.7 V, 0.75 V, 0.8 V, 1.05 V, 1.15 V, 1.35 V, 1.4 V, and 1.45 V.

D13933-0-6/17(A)