

**FEATURES****Two Output Voltages: 1.5 V, 1.2 V****Output Current: each 20 A****Input voltage: 12 V****DC plus Ripple  $<\pm 2\%$  of Output Voltage****Transient step  $\pm 5\%$ , 5 to 15 A at 1 A/ $\mu$ s****ADP1821 REFERENCE DESIGN DESCRIPTION**

This ADP1821 Reference Design uses 12 V  $+5\%$   $-8\%$ , for the input voltage. The output voltages and currents are as follows:

- $V_{OUT1} = 1.5$  V with a maximum output current of 20 A
- $V_{OUT2} = 1.2$  V with a maximum output current of 20 A

This ADP1821 Reference Design was configured for a lower parts count and to meet a specified output voltage ripple (DC+Ripple  $\pm 2\%$ ) and transient ( $\pm 5\%$ , 5 to 15 A at 1 A/ $\mu$ s).

All of the results tested from the evaluation board were running at a switching frequency  $f_{SW} = 300$  kHz with  $V_{IN} = 12$  V,  $V_{OUT1} = 1.5$  V at up to 20 A and  $V_{OUT2} = 1.2$  V at up to 20 A.

Other aspects of the design were tested (such as short circuit, loop stability, switching waveforms) and indicate a sufficient design. The switching waveforms show no shoot through, and the ringing indicates no snubber is necessary.

One condition to note is that if the input supply is ramped up or down slowly with the PWM enabled, a period exists in which the output of the supply will turn on and off multiple times. While this is non-destructive to the converter, it is likely not ideal for the system. To avoid operation in this condition, bring the input voltage up to the normal operating range before enabling the PWM, and disable the PWM before reducing the input voltage.

**Rev. A**

Reference designs are as supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. No license is granted by implication or otherwise under any patents or other intellectual property by application or use of reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Analog Devices reserves the right to change devices or specifications at any time without notice. Trademarks and registered trademarks are the property of their respective owners. Reference designs are not authorized to be used in life support devices or systems.

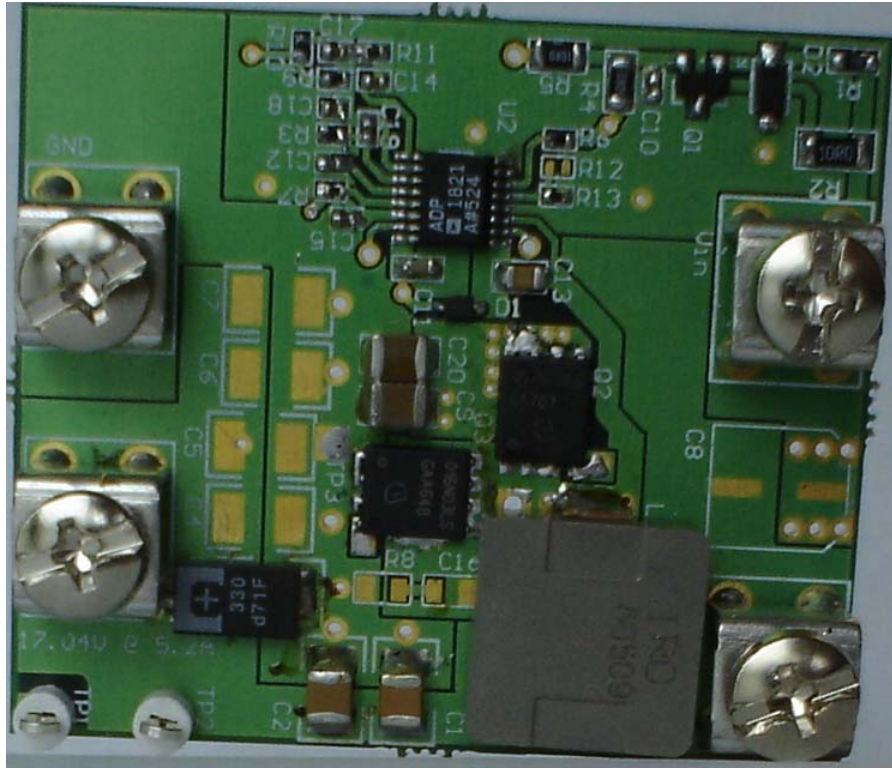


Figure 1. ADP1821 Demo Board

## TABLE OF CONTENTS

Features.....	1
ADP1821 Reference Design Description.....	1
Revision History.....	4
General Description .....	5
Schematic .....	5
Bill of Materials .....	6
Powering the ADP1821 Reference Design .....	8
Input Power Source .....	8
Output Load .....	8
Input and Output Voltmeters.....	8
Turning On the Evaluation Board.....	8
Typical Performance Characteristics.....	9

## TABLE OF FIGURES

Figure 1. ADP1821 Demo Board .....	2
Figure 2. Schematic: 12 V ->1.5 V @ 20 A, 1.2 V @ 20 A .....	5
Figure 3. ADP1821 demo board efficiency for each output .....	9
Figure 4. Voltage Ripple; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 12.6 V .....	9
Figure 5. Voltage Ripple; Ch1 = 1.2 V @ 20 A, Ch2 = $V_{IN}$ @ 12.6 V .....	10
Figure 6. Voltage Ripple; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 11.04 V .....	10
Figure 7. Voltage Ripple; Ch1 = 1.2 V @ 20 A, Ch2 = $V_{IN}$ @ 11.04 V .....	11
Figure 8. Load Transient; Ch1 = 1.2 V @ 5-15 A 1 A/us, Ch2 = $V_{IN}$ @ 11.04 V .....	11
Figure 9. Load Transient; Ch1 = 1.2 V @ 15-5 A 1 A/us, Ch2 = $V_{IN}$ @ 11.04 V .....	12
Figure 10. Load Transient; Ch1 = 1.2 V @ 5-15 A 1 A/us, Ch2 = $V_{IN}$ @ 12.6 V .....	12
Figure 11. Load Transient; Ch1 = 1.2 V @ 15-5 A 1 A/us, Ch2 = $V_{IN}$ @ 12.6 V .....	13
Figure 12. Output Enable; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 11.04 V, Ch3 = Enable .....	13
Figure 13. Output Enable; Ch1 = 1.2 V @ 20 A, Ch2 = $V_{IN}$ @ 11.04 V, Ch3 = Enable .....	14
Figure 14. Output Enable; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 12.6 V, Ch3 = Enable .....	14
Figure 15. Output Enable; Ch1 = 1.2 V @ 20 A, Ch2 = $V_{IN}$ @ 12.6 V, Ch3 = Enable .....	15
Figure 16. Output Disable; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 11.04 V, Ch3 = Enable .....	15
Figure 17. Output Disable; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 12.6 V, Ch3 = Enable .....	16
Figure 18. Output Shorted; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ @ 12 V .....	16
Figure 19. Output Short Removed; Ch1 = 1.2 V @ 20 A, Ch2 = $V_{IN}$ @ 12 V, .....	17
Figure 20. $V_{IN}$ Ramped On; Ch1 = 1.2 V @ 0 A, Ch2 = $V_{IN}$ .....	17
Figure 21. $V_{IN}$ Ramped On; Ch1 = 1.2 V @ 10 A, Ch2 = $V_{IN}$ .....	18

Figure 22.  $V_{IN}$  Ramped Off; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$ ..... 18

Figure 23.  $V_{IN}$  Ramped Off; Ch1 = 1.2 V @ 10 A, Ch2 =  $V_{IN}$ ..... 19

Figure 24. 1.2 V @ 0 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V ..... 19

Figure 25. 1.2 V @ 0 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V ..... 20

Figure 26. 1.2 V @ 20 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V ..... 20

Figure 27. 1.2 V @ 20 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V ..... 21

Figure 28. 1.2 V @ 0 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 12.6 V ..... 21

Figure 29. 1.2 V @ 0 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 12.6 V ..... 22

Figure 30. 1.2 V @ 20 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V ..... 22

Figure 31. 1.2 V @ 20 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V ..... 23

**REVISION HISTORY**

- 6/15/2007—Revision 2: Testing on a couple of the outputs
- 5/24/2007—Revision 1: Testing on a couple of the outputs
- 5/14/2007—Revision 0: Initial Version

## GENERAL DESCRIPTION

The ADP1821 is a versatile, single output, synchronous PWM buck controller that generates outputs from an input voltage of 3.7 V to 20 V. The controller can be configured to provide output voltage from 0.6 V to 85% of the input voltage.

The ADP1821 operates at a pin-selectable fixed switching frequency of either 300 kHz or 600 kHz. For some noise sensitive applications, it can also be synchronized to an external clock to achieve switching frequency between 300 kHz and 1 MHz. The switching frequency chosen is 300 kHz to get good efficiency over a wide range of input and output conditions.

The ADP1821 includes an adjustable soft start to limit input inrush current, power-good output, and a power enable pin. It also provides current-limit and short-circuit protection by sensing the voltage on the synchronous MOSFET.

## SCHEMATIC

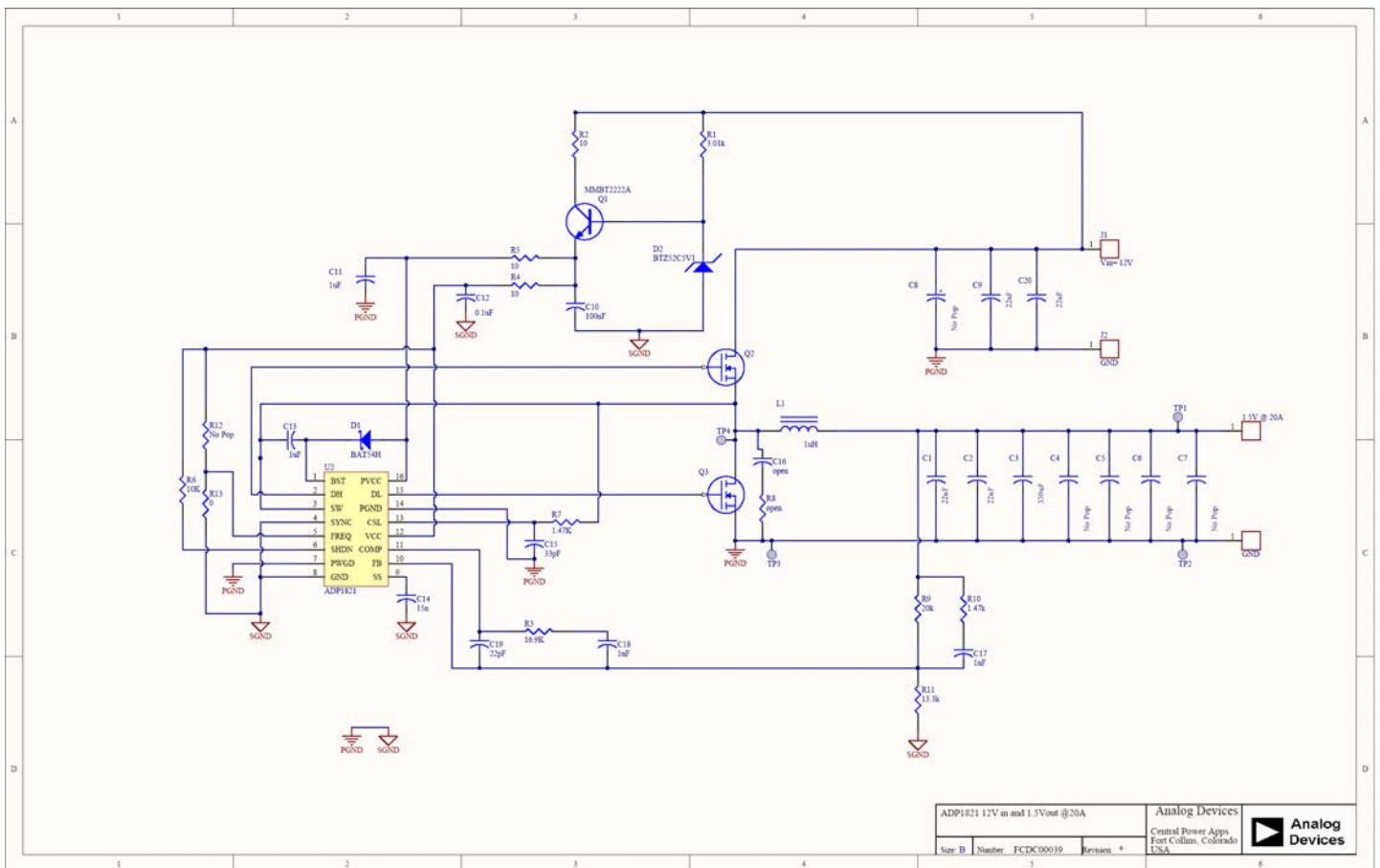


Figure 2. Schematic: 12 V->1.5 V @ 20 A, 1.2 V @ 20 A

**BILL OF MATERIALS****Table 1.**  $V_{OUT1} = 1.5\text{ V}$ 

Description	Designator	Qty	Manufacturer	MFR#
Capacitor Ceramic X5R 22u 1210 16V	C1, C2, C9, C20	4	Murata	GRM32ER61A226K
Capacitor POSCAP 330u D case 2.5V	C3	1	Sanyo	2TPF330M7
Capacitor Ceramic X7R 1u 0603 16V	C11	1	Murata	GRM188R61A105K
Capacitor Ceramic COG 680p 0402 50V	C17, C18	2	Vishay	Generic
Capacitor Ceramic X7R 100n 16V	C10, C13, C14, C12	4	Vishay	Generic
Capacitor Ceramic COG 22p 0402 50V	C19	1	Vishay	Generic
Capacitor Ceramic COG 33p 0402 50V	C15	1	Vishay	Generic
Inductor 4.0uH 11.2mm x 10.5mm x 4.8mm	L1	1	TDK	SPM12550T-1R0M220
Single N-Channel MOSFET TDSO-8 30V	Q2	1	Infineon	BSC057N03LS
Single N-Channel MOSFET TDSO-8 30V	Q3	1	Infineon	BSC016N03LS
1% Thick Film 3.01k 0402	R1	1	Vishay	Generic
5% Thick Film 10 Ohms 1206	R2	1	Vishay	Generic
5% Thick Film 10 Ohms 0402	R4, R5	2	Vishay	Generic
Not Populated	R12	1	Vishay	Generic
1% Thick Film 10.0k 0402	R6	1	Vishay	Generic
0 Ohm jumper 0402	R13	1	Vishay	Generic
Not Populated	R8	1	Vishay	Generic
1% Thick Film 1.47k 0402	R7, R10	2	Vishay	Generic
1% Thick Film 20.0k 0402	R9	1	Vishay	Generic
1% Thick Film 13.3k 0402	R11	1	Vishay	Generic
1% Thick Film 16.9k 0402	R3	1	Vishay	Generic
1 channel 300k to 600k PWM	U2	1	Analog Devices	ADP1821
Diode Schottky 200mA SOD-323 40V	D1	1	Diodes inc	BAT54
Diode Zener 5.1V, SOD123	D2	1	Diodes inc	BTZ52C5V1
NPN Transistor SOT-23	Q1	1	Vishay	MMBT2222A

**Table 2.**  $V_{OUT2} = 1.2\text{ V}$ 

Description	Designator	Qty	Manufacturer	MFR#
Capacitor Ceramic X5R 22u 1210 16V	C1, C2, C9, C20	4	Murata	GRM32ER61A226K
Capacitor POSCAP 330u D case 2.5V	C3	1	Sanyo	2TPF330M7
Capacitor Ceramic X7R 1u 0603 16V	C11	1	Murata	GRM188R61A105K
Capacitor Ceramic COG 680p 0402 50V	C17, C18	2	Vishay	Generic
Capacitor Ceramic X7R 100n 16V	C10, C13, C14, C12	4	Vishay	Generic
Capacitor Ceramic COG 22p 0402 50V	C19	1	Vishay	Generic
Capacitor Ceramic COG 33p 0402 50V	C15	1	Vishay	Generic
Inductor 4.0uH 11.2mm x 10.5mm x 4.8mm	L1	1	TDK	SPM12550T-1R0M220
Single N-Channel MOSFET TDSO-8 30V	Q2	1	Infineon	BSC057N03LS
Single N-Channel MOSFET TDSO-8 30V	Q3	1	Infineon	BSC016N03LS
1% Thick Film 3.01k 0402	R1	1	Vishay	Generic
5% Thick Film 10 Ohms 1206	R2	1	Vishay	Generic
5% Thick Film 10 Ohms 0402	R4, R5	2	Vishay	Generic

# Preliminary Technical Data

**FCDC 00039**

Not Populated	R12	1	Vishay	Generic
1% Thick Film 10.0k 0402	R6	1	Vishay	Generic
0 Ohm jumper 0402	R13	1	Vishay	Generic
Not Populated	R8	1	Vishay	Generic
1% Thick Film 1.47k 0402	R7, R10	2	Vishay	Generic
1% Thick Film 20.0k 0402	R9	1	Vishay	Generic
1% Thick Film 20.0k 0402	R11	1	Vishay	Generic
1% Thick Film 16.9k 0402	R3	1	Vishay	Generic
1 channel 300k to 600k PWM	U2	1	Analog Devices	ADP1821
Diode Schottky 200mA SOD-323 40V	D1	1	Diodes inc	BAT54
Diode Zener 5.1V, SOD123	D2	1	Diodes inc	BTZ52C5V1
NPN Transistor SOT-23	Q1	1	Vishay	MMBT2222A

## POWERING THE ADP1821 REFERENCE DESIGN

The ADP1821 Reference Design is supplied fully assembled.

### INPUT POWER SOURCE

1. Before connecting the power source to the ADP1821 Reference Design, make sure that it is turned off. If the input power source includes a current meter, use that meter to monitor the input current.
2. Connect the positive terminal of the power source to the VIN terminal on the evaluation board, and the negative terminal of the power source to the GND terminal just below the VIN terminal.
3. If the power source does not include a current meter, connect a current meter in series with the input source voltage.
4. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (–) of the power source to the GND terminal just below the VIN terminal on the board, and the negative lead (–) of the ammeter to the VIN terminal on the board.

### OUTPUT LOAD

1. Although the ADP1821 Reference Design can sustain the sudden connection of the load, it is possible to damage the load if it is not properly connected.
2. Make sure that the board is turned off before connecting the load.
  - a) If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board with the positive (+) load connection to the  $V_{OUT}$  terminal and negative (–) load connection to the GND terminal just above the  $V_{OUT}$  terminal.
  - b) If an ammeter is used, connect it in series with the load; connect the positive (+) ammeter terminal to the evaluation board  $V_{OUT}$  terminal, the negative (–) ammeter terminal to the positive (+) load terminal, and the negative (–) load terminal to the evaluation board GND terminal just above the  $V_{OUT}$  terminal.

Once the load is connected, make sure that it is set to the proper current before powering the ADP1821 Reference Design.

### INPUT AND OUTPUT VOLTMETERS

Measure the input and output voltages with voltmeters.

1. Connect the voltmeter measuring the input voltage with the positive (+) lead connected to Vin and the negative lead (–) connected to Gnd (measure across C8).
2. Connect the voltmeter measuring the  $V_{OUT1}$  with the positive lead (+) connected to TP1 and the negative lead (–) connected to TP2.
3. Make sure to connect the voltmeters to the appropriate evaluation board terminals and not to the load or power source themselves.
4. If the voltmeters are not connected directly to the evaluation board at these Kelvin connection test points, the measured voltages will be incorrect due to the voltage drop across the leads connecting the evaluation board to both the source and load.

### TURNING ON THE EVALUATION BOARD

Once the power source and loads are connected to the ADP1821 Reference Design, the board can be powered for operation. Slowly increase the input power source voltage until the input voltage exceeds the minimum input operating voltage of 10 V. If the load is not already enabled, enable the load and check that it is drawing the proper current and that the output voltage maintains voltage regulation.



# TYPICAL PERFORMANCE CHARACTERISTICS

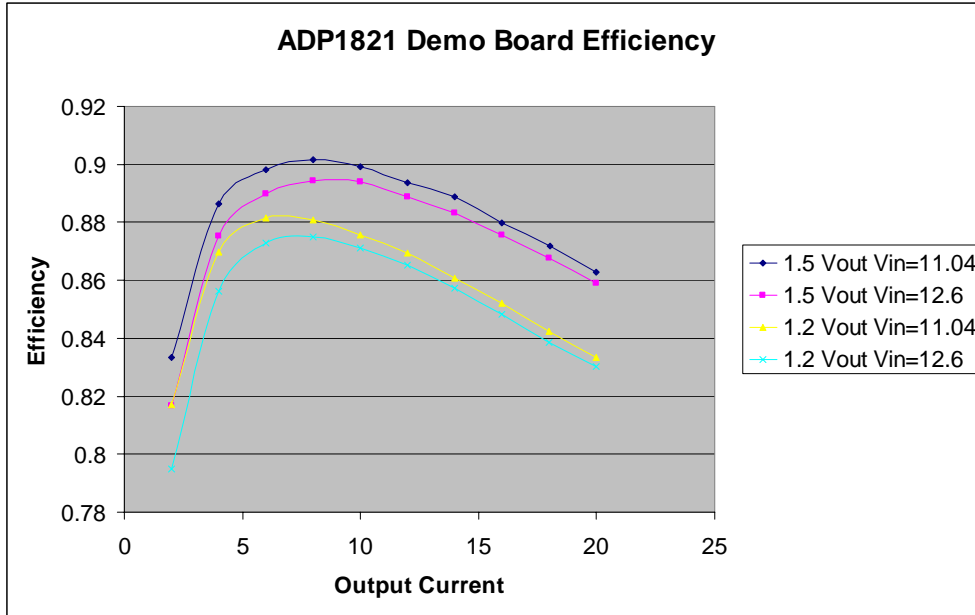


Figure 3. ADP1821 demo board efficiency for each output

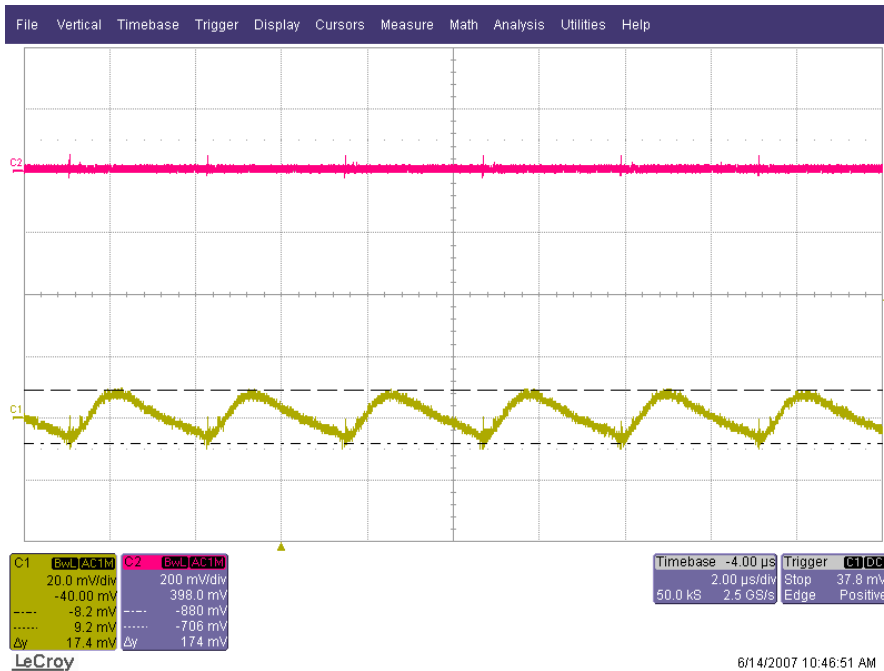


Figure 4. Voltage Ripple; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$  @ 12.6 V



Figure 5. Voltage Ripple; Ch1 = 1.2 V @ 20 A, Ch2 =  $V_{IN}$  @ 12.6 V

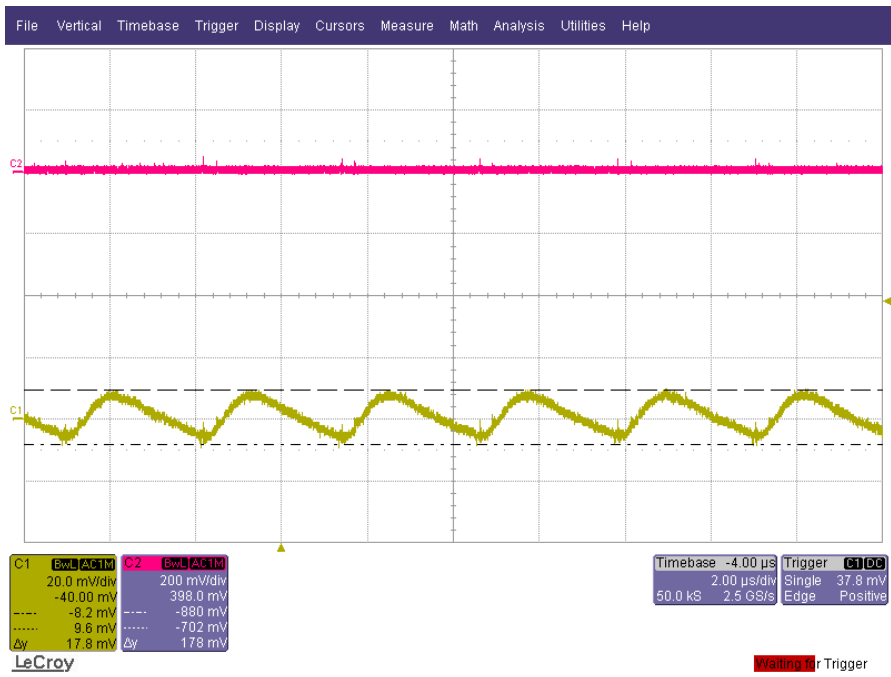


Figure 6. Voltage Ripple; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$  @ 11.04 V



Figure 7. Voltage Ripple; Ch1 = 1.2V @ 20 A, Ch2 =  $V_{IN}$  @ 11.04 V



Figure 8. Load Transient; Ch1 = 1.2V @ 5-15 A 1 A/us, Ch2 =  $V_{IN}$  @ 11.04 V

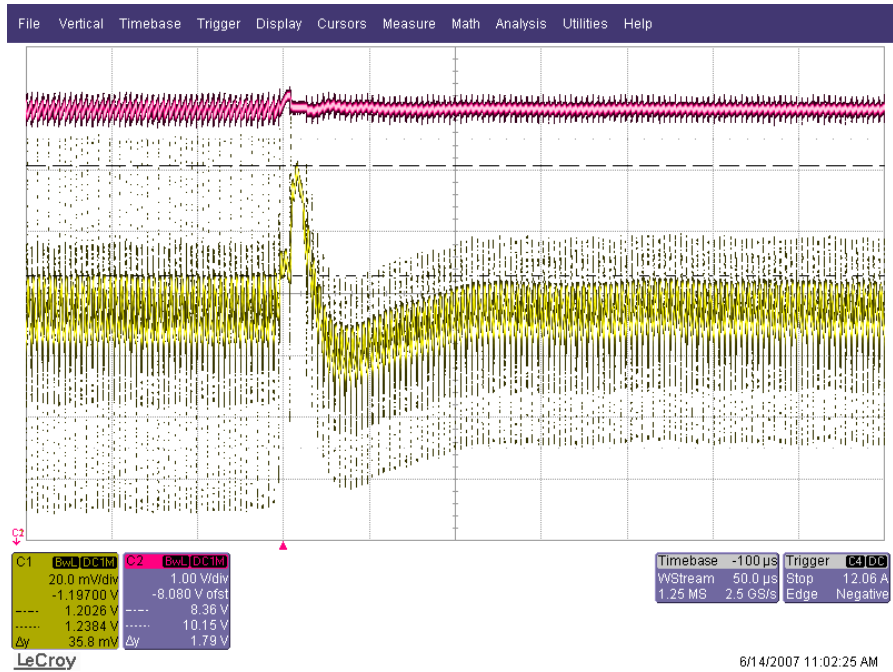


Figure 9. Load Transient; Ch1 = 1.2V @ 15-5 A 1 A/us, Ch2 =  $V_{IN}$  @ 11.04 V

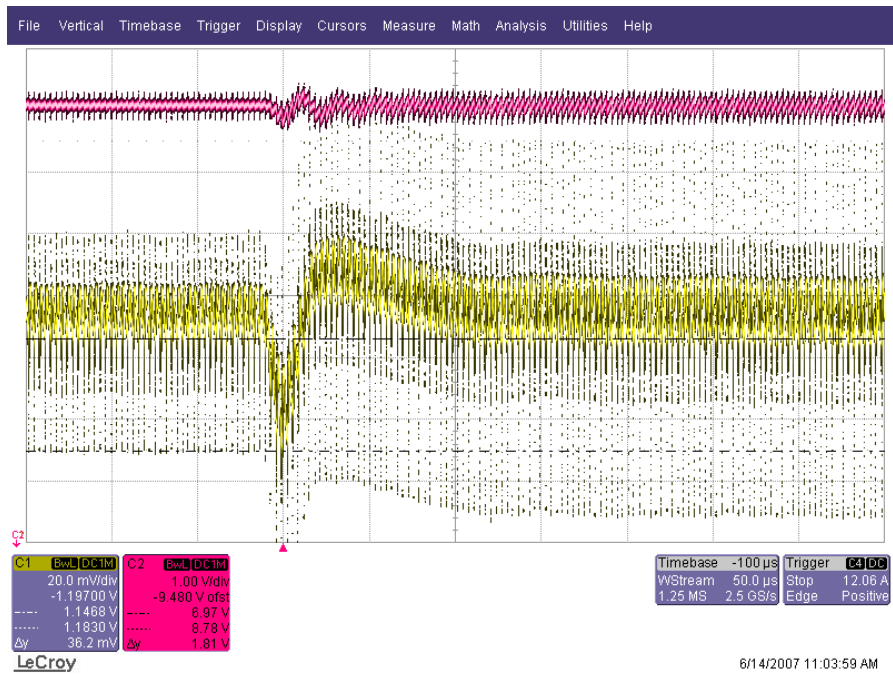


Figure 10. Load Transient; Ch1 = 1.2V @ 5-15 A 1 A/us, Ch2 =  $V_{IN}$  @ 12.6 V

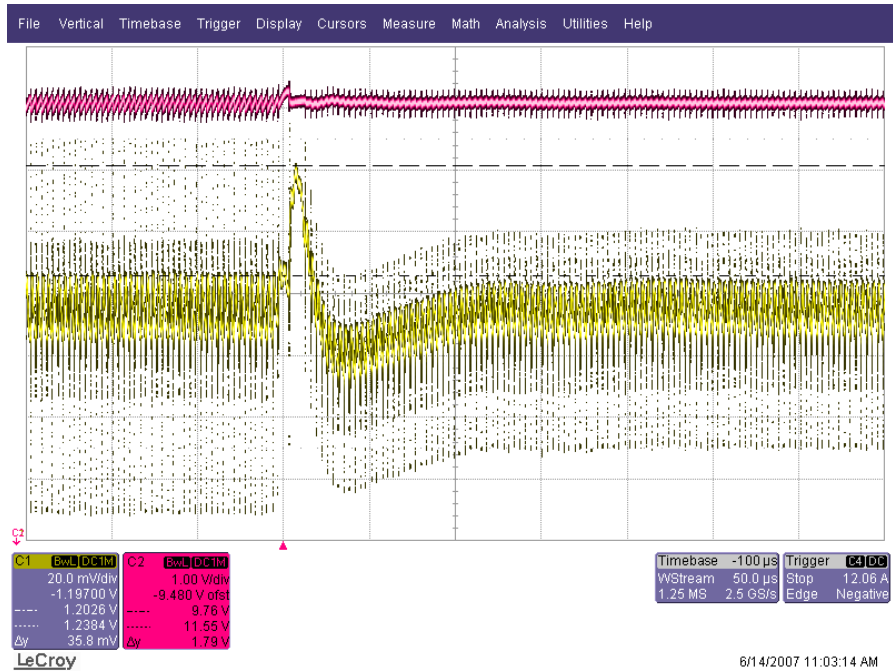


Figure 11. Load Transient; Ch1 = 1.2 V @ 15-5 A 1 A/us, Ch2 =  $V_{IN}$  @ 12.6 V

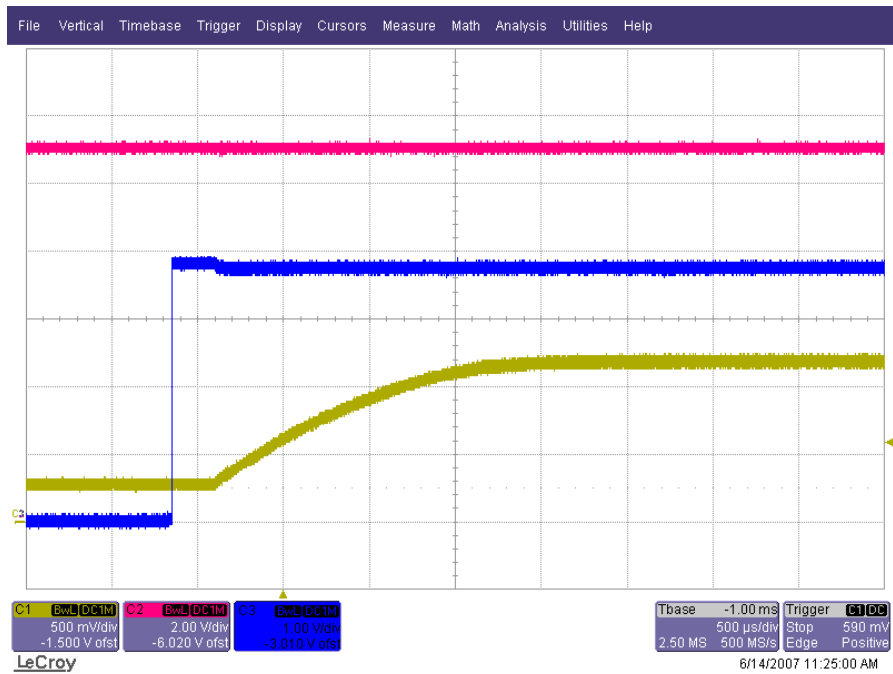


Figure 12. Output Enable; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$  @ 11.04 V, Ch3 = Enable

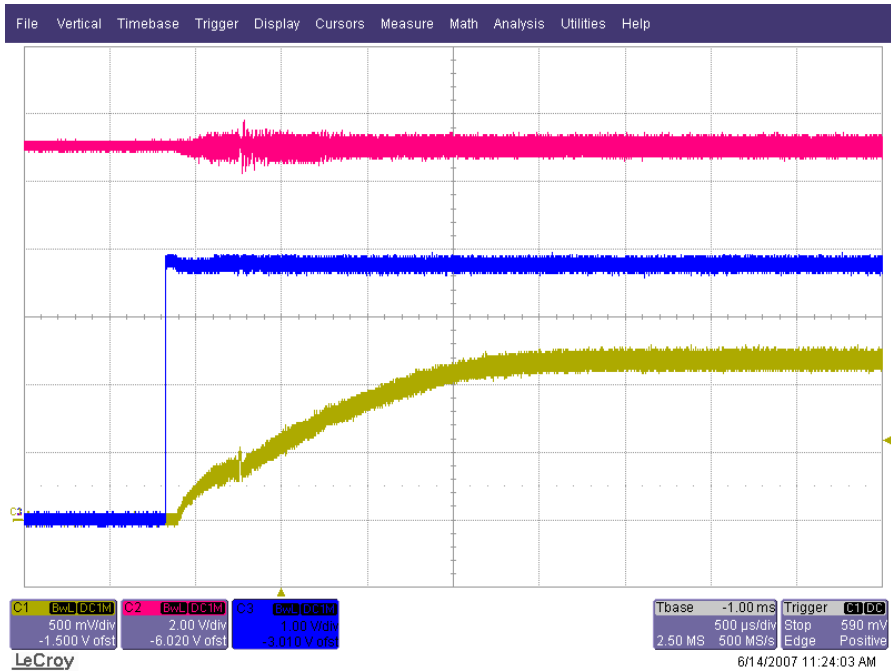


Figure 13. Output Enable; Ch1 = 1.2 V @ 20 A, Ch2 =  $V_{IN}$  @ 11.04 V, Ch3 = Enable

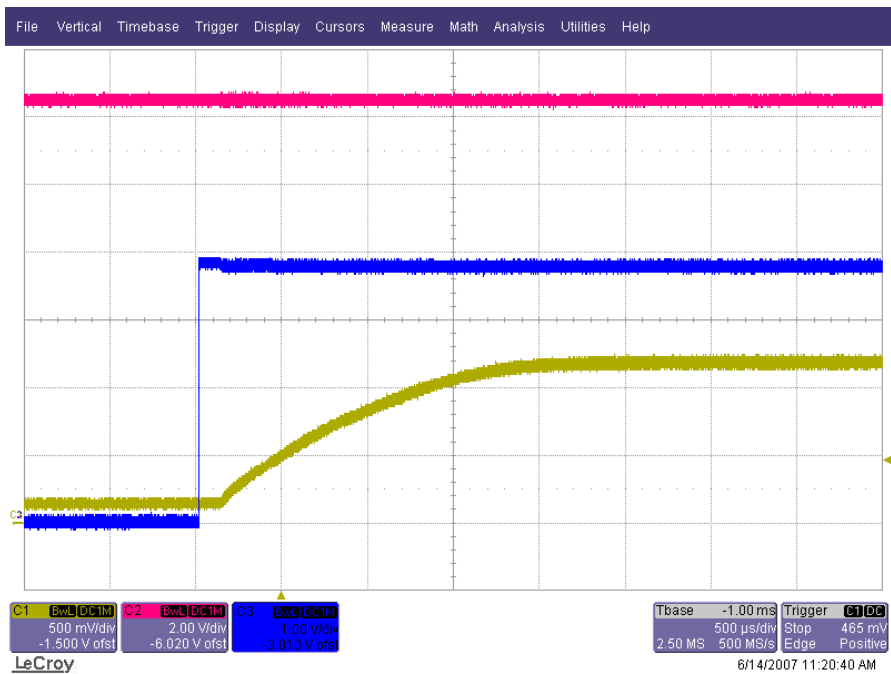


Figure 14. Output Enable; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$  @ 12.6 V, Ch3 = Enable

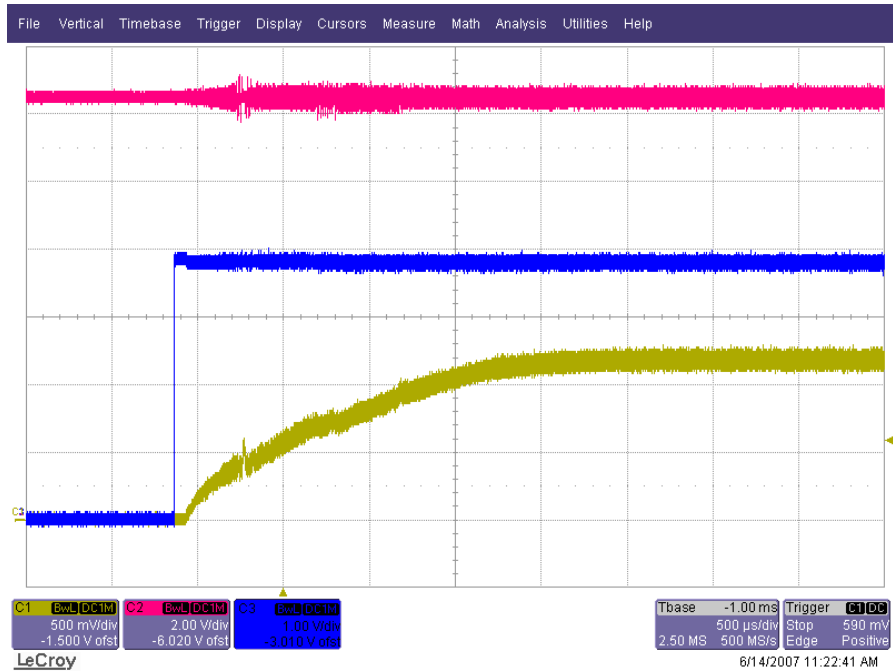


Figure 15. Output Enable; Ch1 = 1.2 V @ 20 A, Ch2 =  $V_{IN}$  @ 12.6 V, Ch3 = Enable

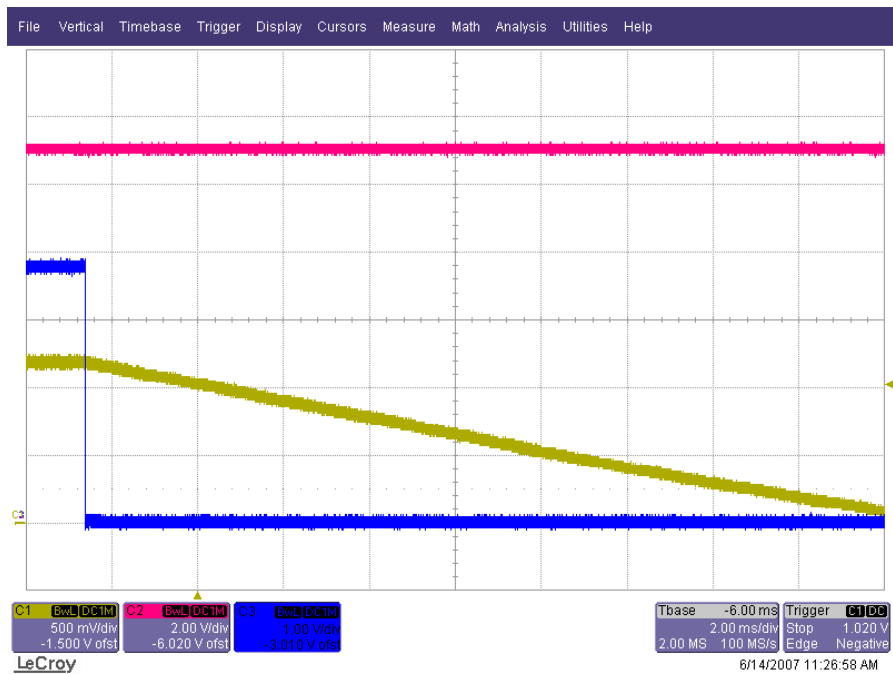


Figure 16. Output Disable; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$  @ 11.04 V, Ch3 = Enable



Figure 17. Output Disable; Ch1 = 1.2V @ 0A, Ch2 =  $V_{IN}$  @ 12.6 V, Ch3 = Enable

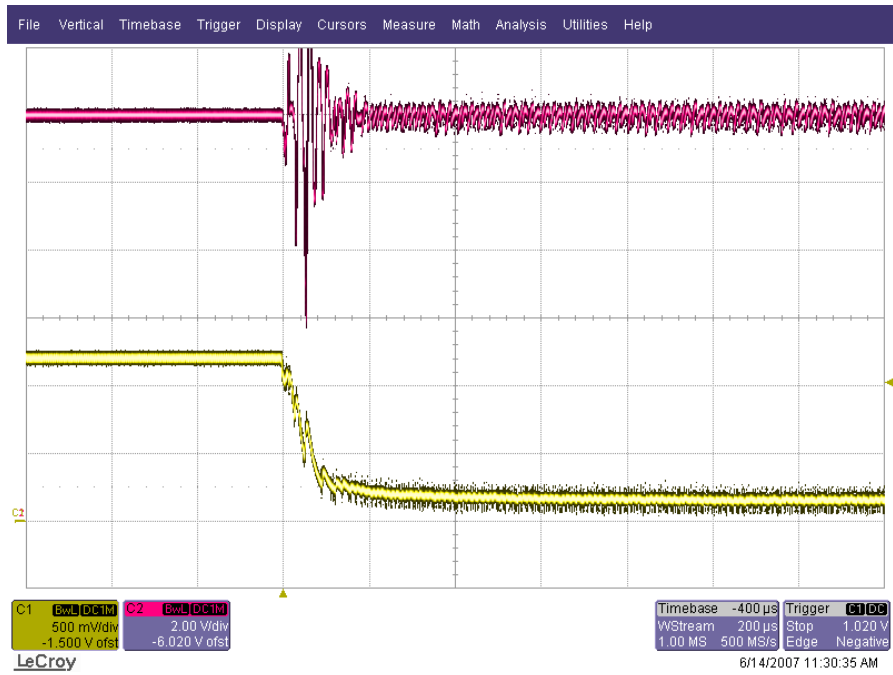


Figure 18. Output Shorted; Ch1 = 1.2V @ 0A, Ch2 =  $V_{IN}$  @ 12 V



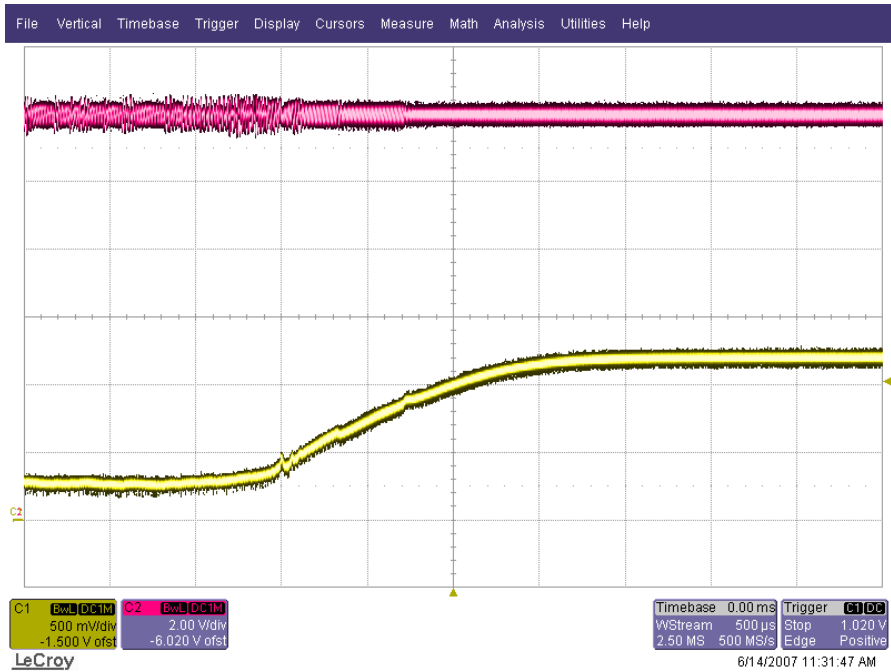


Figure 19. Output Short Removed; Ch1 = 1.2 V @ 20 A, Ch2 =  $V_{IN}$  @ 12 V,

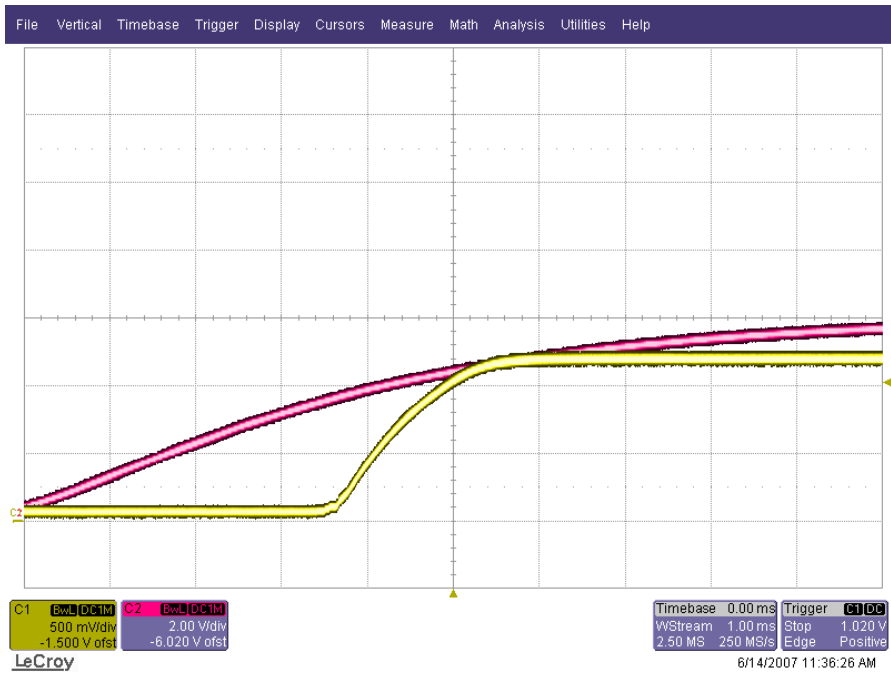


Figure 20.  $V_{IN}$  Ramped On; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$

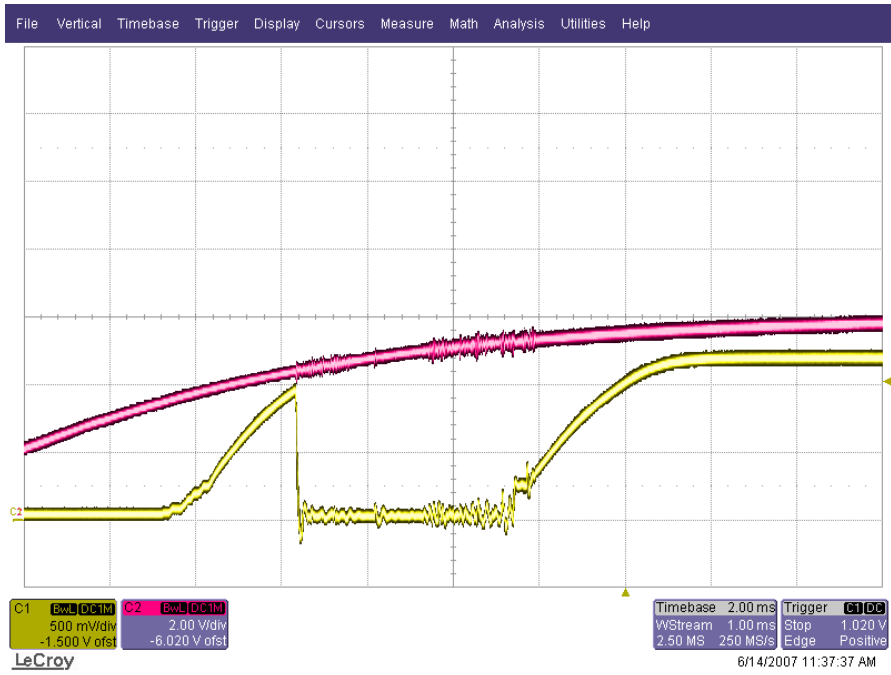


Figure 21.  $V_{IN}$  Ramped On; Ch1 = 1.2 V @ 10 A, Ch2 =  $V_{IN}$

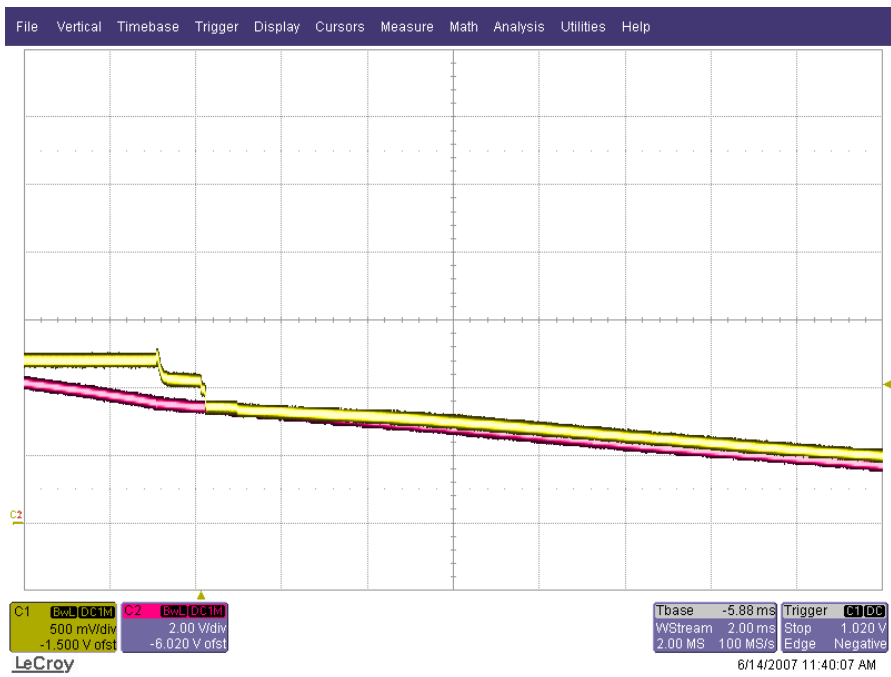


Figure 22.  $V_{IN}$  Ramped Off; Ch1 = 1.2 V @ 0 A, Ch2 =  $V_{IN}$

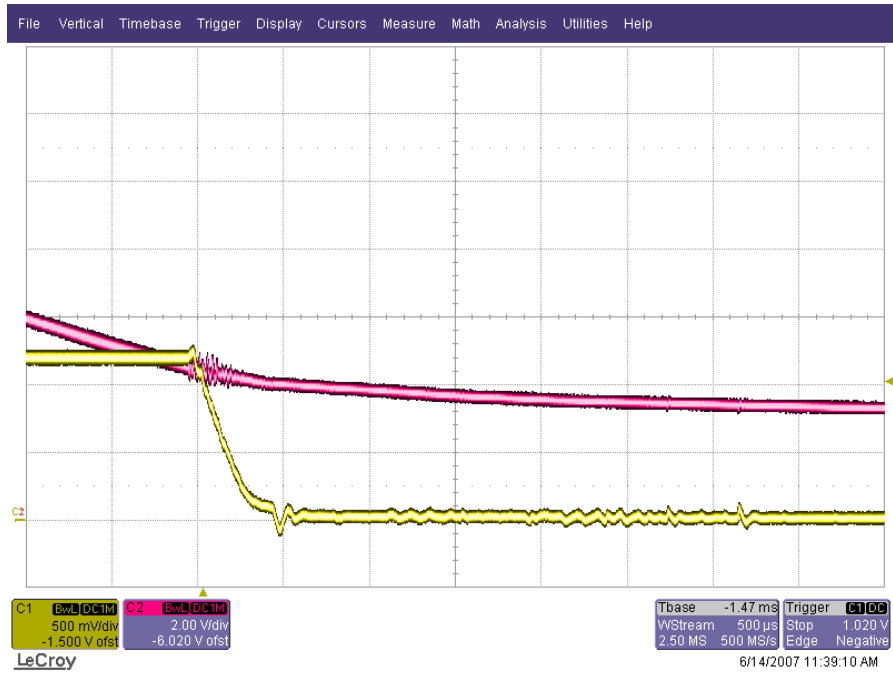


Figure 23.  $V_{IN}$  Ramped Off; Ch1 = 1.2V @ 10 A, Ch2 =  $V_{IN}$

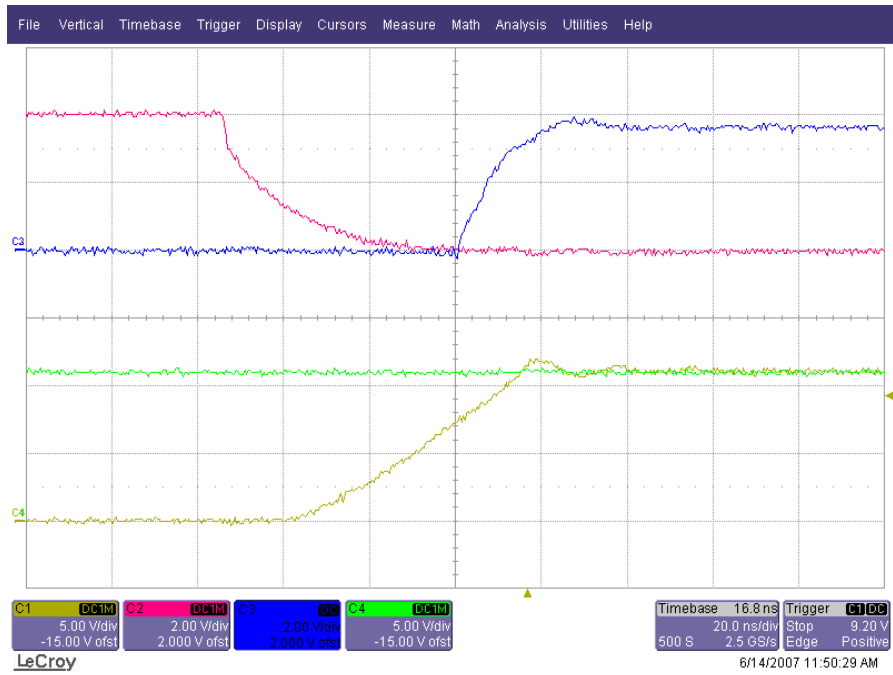


Figure 24. 1.2V @ 0A Rising Switchnode; Ch1 =  $V_{ds}$  low, Ch2 =  $V_{gs}$  low, Ch3 =  $V_{gs}$  high, Ch4 =  $V_{IN}$  @ 11.04V

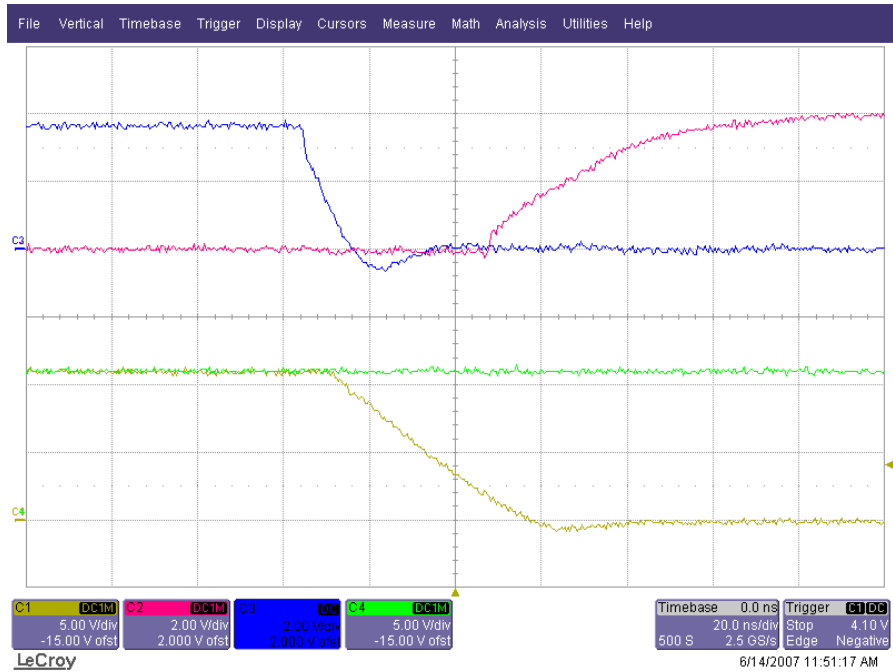


Figure 25. 1.2V @ 0A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V

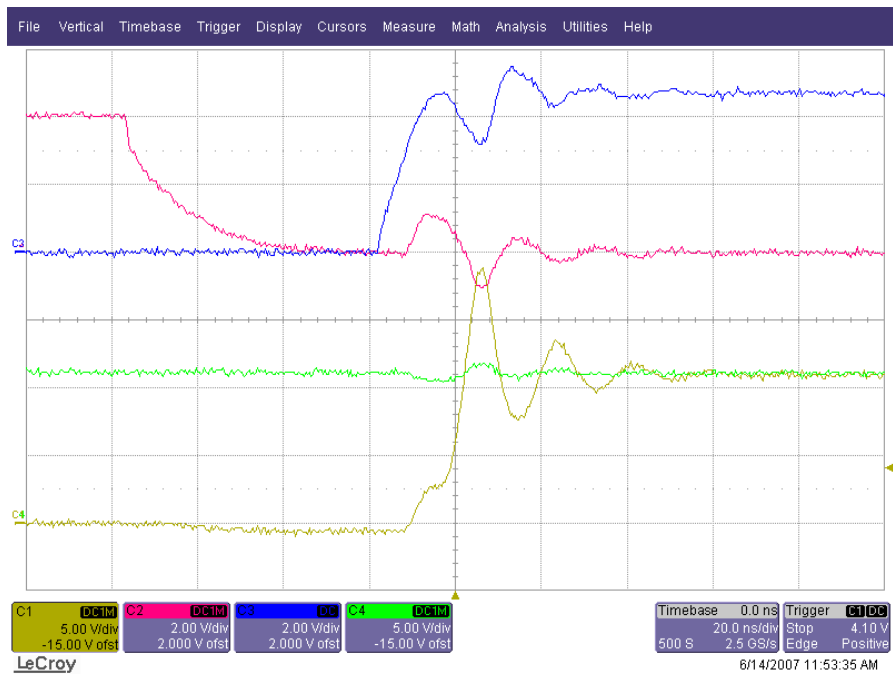


Figure 26. 1.2V @ 20A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V

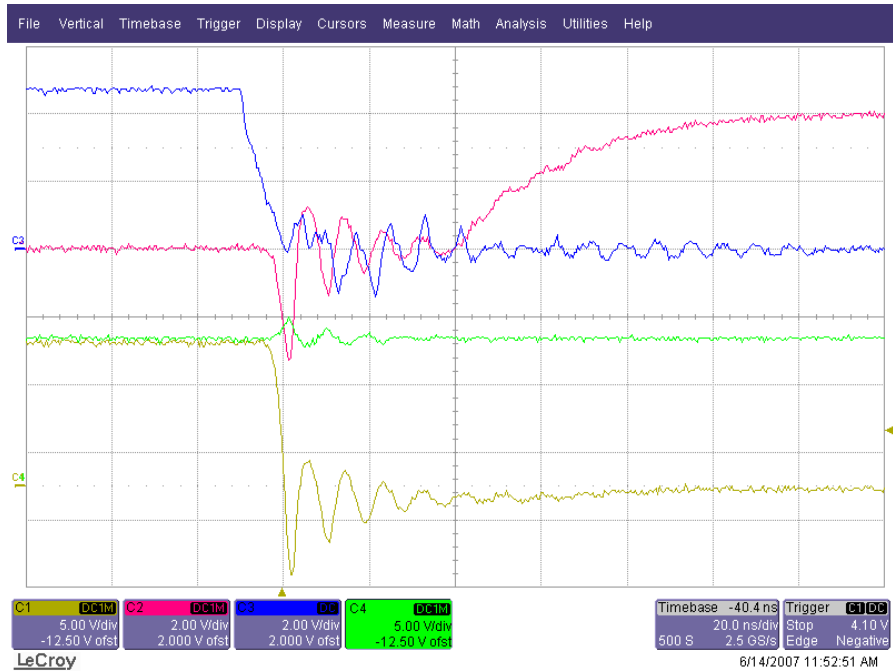


Figure 27. 1.2 V @ 20 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V

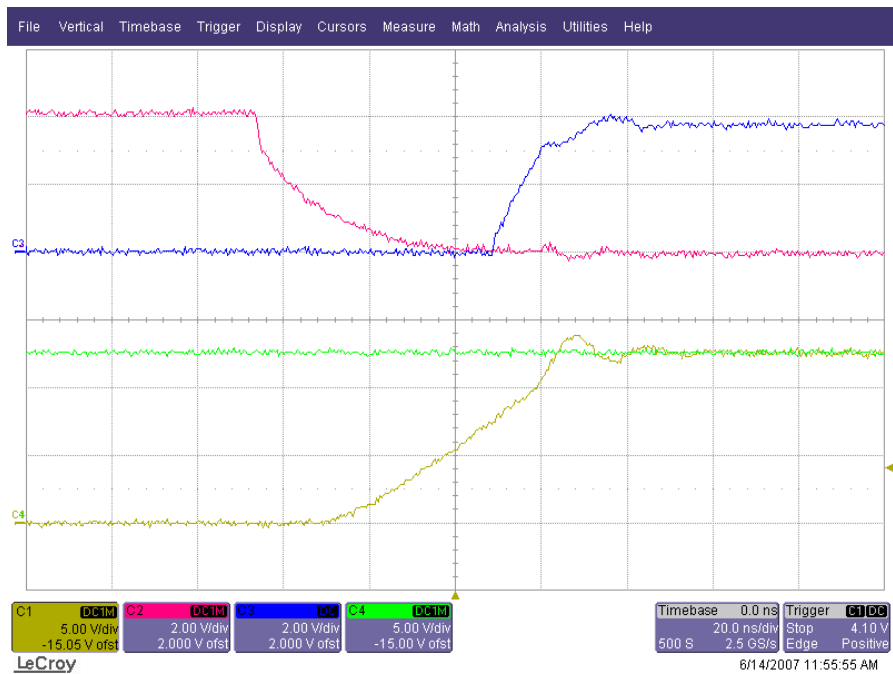


Figure 28. 1.2 V @ 0 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 12.6 V

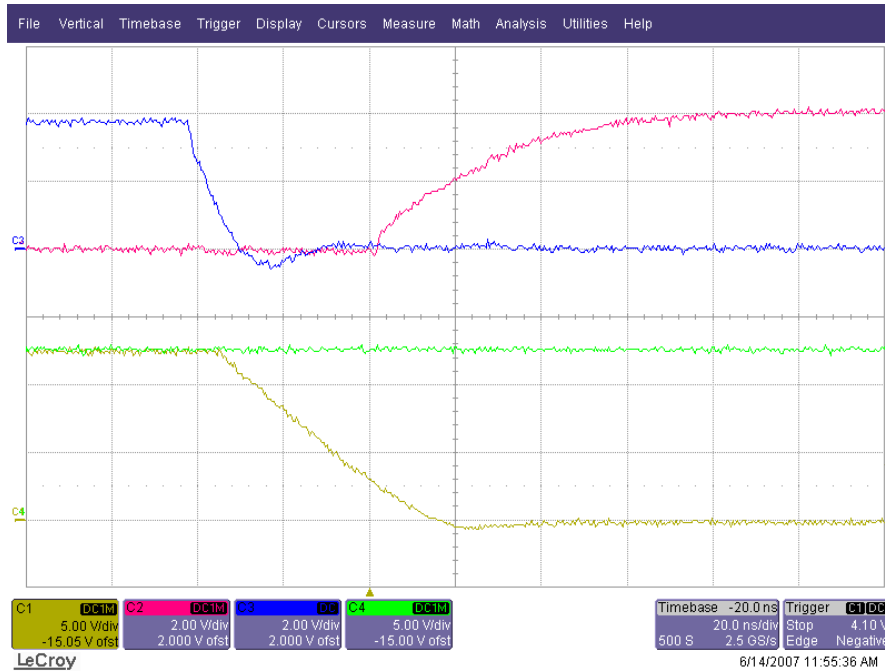


Figure 29. 1.2 V @ 0 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 12.6 V

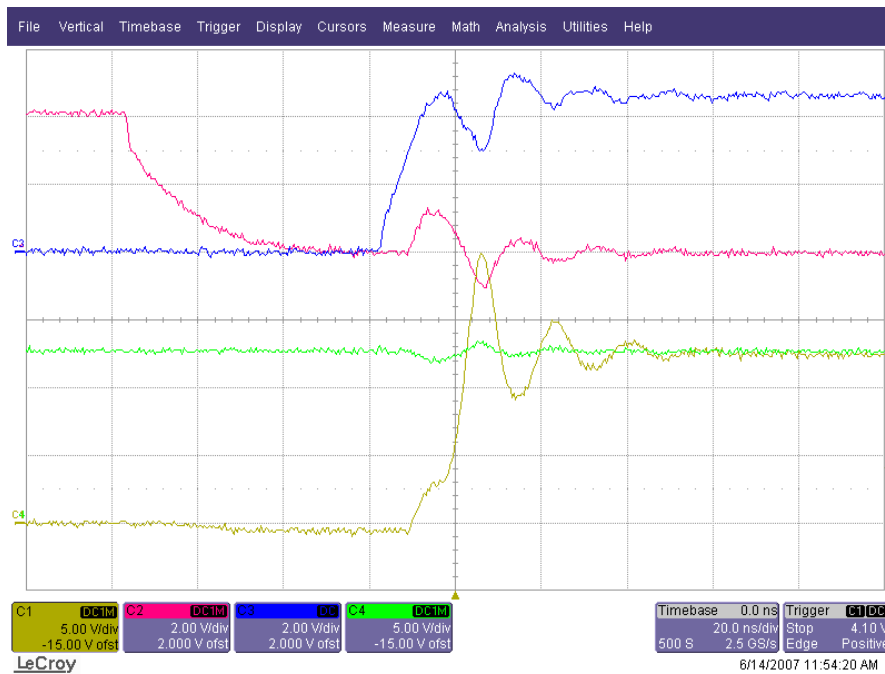


Figure 30. 1.2 V @ 20 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V

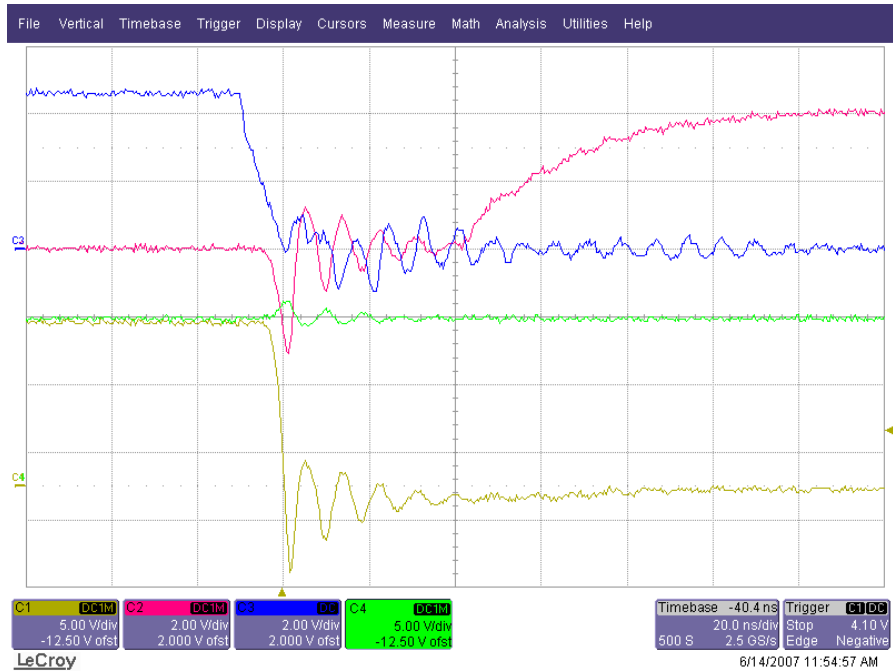


Figure 31. 1.2 V @ 20 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 =  $V_{IN}$  @ 11.04 V

## NOTES

This ADP1821 Reference Design uses a board that was originally laid out for a supply creating 17.04 V @ 5.2 A. For this reason, it is not ideally designed for 20 A. The board copper loss at 20 A is not desirable but all other circuit functionality is properly verified by this design.

©2007 Analog Devices, Inc. All rights reserved.  
Trademarks and registered trademarks are the  
property of their respective owners.

EB



[www.analog.com](http://www.analog.com)



