ADP1821 Reference Design

Preliminary Technical Data **FCDC00093**

FEATURES

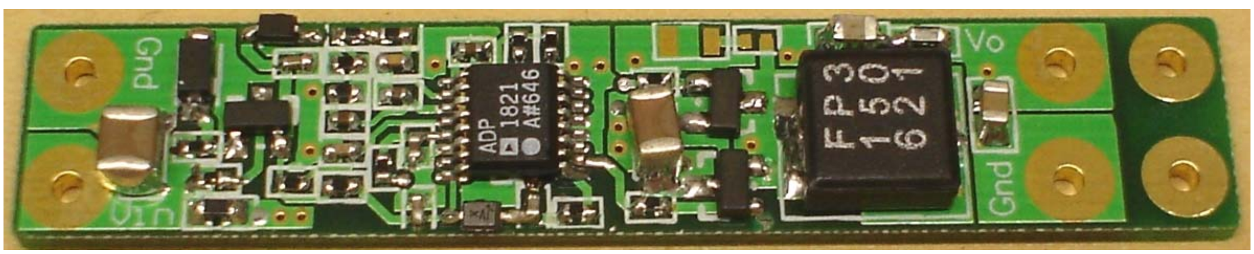
Single Output Voltage: 5.0 V
Output Current: 1.4 A
Input voltage: 9 V to 20 V
Ripple <1% ppk of Output Voltage
Transient step ±5%, 50% max load

ADP1821 REFERENCE DESIGN DESCRIPTION

This ADP1821 Reference Design uses a 9 to 20 V input voltage to generate a 5.0 V output voltage (V_{OUT1}) with a maximum output current of 1.4 A,

The output voltage ripple is less than 1% peak-to-peak of the DC output voltage. The output voltage deviates less than 5% upon a 50% (0.7 A) load step and load release. The switching is externally set to 300 kHz on the ADP1821.

Figure 1. ADP1821 Demo Board



Rev. 2

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REVISION HISTORY

12/21/2007—Revision 1: Initial Version

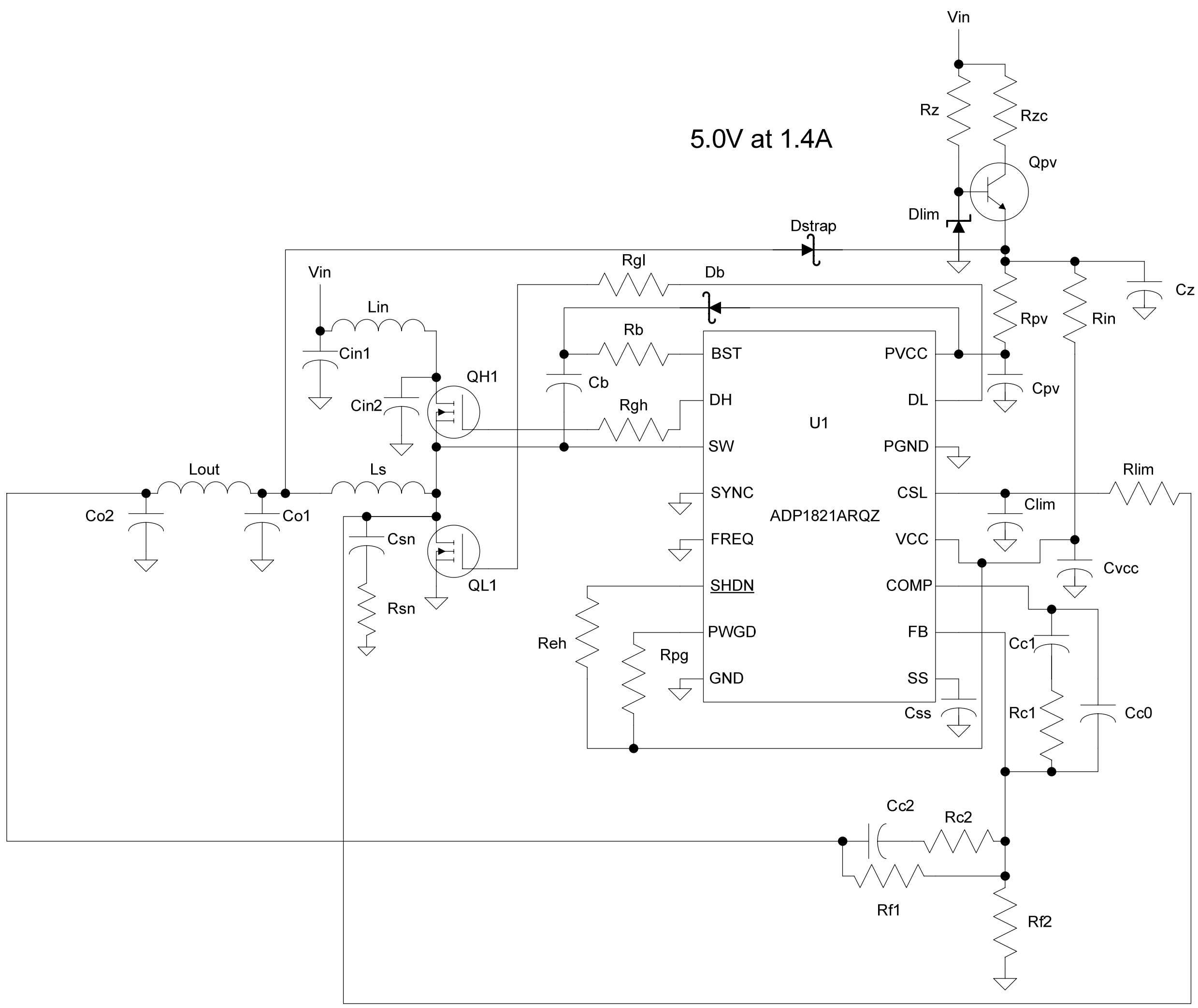
1/18/2008—Revision 2: Updated for new hardware, including lab data and scope shots (minor BOM changes)

GENERAL DESCRIPTION

The ADP1821 is a versatile and inexpensive, synchronous, pulse width-modulated (PWM), voltage-mode, step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V. The ADP1821 can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The ADP1821 is well suited for a wide range of high power applications, such as DSP and processor core power in telecom, medical imaging, high performance servers, and industrial applications. It operates from a 3.0 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V. The ADP1821 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise-sensitive applications, it can be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1.2 MHz. The ADP1821 includes soft start protection to limit the inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing. The ADP1821 operates over the −40°C to +85°C temperature range and is available in a 16-lead QSOP.

SCHEMATIC

Figure 2. Schematic: 20V ->5V@1.4A



BILL OF MATERIALS

Table 1. V_{OUT1}

Description	Designator	Qty	Manufacturer	MFR#
Capacitor Ceramic X5R 10u 0805 6.3V	Co1, Co2	2	Murata	GRM21BR60J106K
Capacitor Ceramic X7R 22u 1210 25V	Cin1, Cin2	2	Murata	GRM32DR71E106K
Capacitor Ceramic X7R 1.0n 0402 50V	Csn	1	Vishay	Generic
Capacitor Ceramic X7R 33n 0402 16V	Css	1	Vishay	Generic
Capacitor Ceramic X7R 4.7n 0402 50V	Cc1	1	Vishay	Generic
Capacitor Ceramic COG 22p 0402 50V	Cc0	1	Vishay	Generic
Capacitor Ceramic COG 820p 0402 50V	Cc2	1	Vishay	Generic
Capacitor Ceramic X7R 100n 0402 16V	Cz, Cpv, Cb, Cvcc	4	Vishay	Generic
Capacitor Ceramic COG 33p 0402 50V	Clim	1	Vishay	Generic
Inductor 100 Ohms 0603 1.7A	Lin	1	Taiyo Yuden	BKP1608HS101
Zero Ohm jumper Thick Film 0603	Lout	1	Vishay	Si2316ds
Inductor 15.0uH 6.7mm x 7.25mm x 3mm	Ls	1	Coiltronic	FP3-150-R
Single N-Channel MOSFET SOT-23 30V	QH1, QL1	2	Vishay	Si2316ds
Zero Ohm jumper Thick Film 0402	Rb, Reh	2	Vishay	Generic
5% Thick Film 10 Ohms 0402	Rin, Rpv, Rzc	3	Vishay	Generic
1% Thick Film 6.3k 0402	Rz	1	Vishay	Generic
5% Thick Film 15 Ohms 0402	Rgh	1	Vishay	Generic
5% Thick Film 3.0 Ohms 0402	Rgl	1	Vishay	Generic
5% Thick Film 3.0 Ohms 0805	Rsn	1	Vishay	Generic
1% Thick Film 20.0k 0402	Rf1	1	Vishay	Generic
1% Thick Film 2.74k 0402	Rf2	1	Vishay	Generic
1% Thick Film 1.50k 0402	Rc2	1	Vishay	Generic
1% Thick Film 4.22k 0402	Rc1	1	Vishay	Generic
1% Thick Film 100k 0402	Rpg	1	Vishay	Generic
1% Thick Film 5.62k 0402	Rlim	1	Vishay	Generic
1 channel 300k to 600k PWM	U1	1	Analog Devices	ADP1821
Diode Schottky 200mA SOD-323 30V	Db, Dstrap	2	Diodes inc	BAT54
Diode Zener 5.1V, SOD123	Dlim	1	Diodes inc	BTZ52C5V1
NPN Transistor SOT-23	Qpv	1	Vishay	MMBT2222A

ASSEMBLY DRAWING

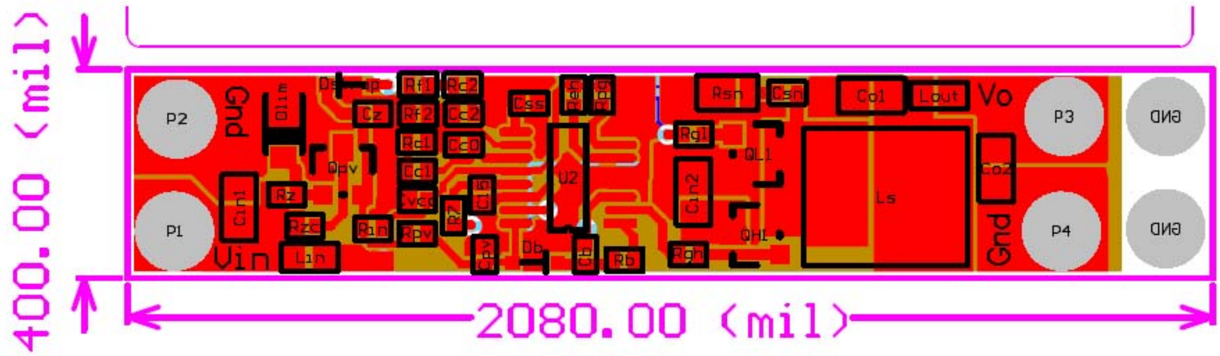


Figure 3. Top Assembly Drawing for 1829 Demo Board

POWERING THE ADP1821 REFERENCE DESIGN

The ADP1821 Reference Design is supplied fully assembled.

INPUT POWER SOURCE

1. Before connecting the power source to the ADP1821 Reference Design, make sure that it is turned off. If the input power source includes a current meter, use that meter to monitor the input current.
2. Connect the positive terminal of the power source to the VIN terminal on the evaluation board, and the negative terminal of the power source to the GND terminal next to the VIN terminal.
3. If the power source does not include a current meter, connect a current meter in series with the input source voltage.
4. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (−) of the power source to the GND terminal on the board, and the negative lead (−) of the ammeter to the VIN terminal on the board.

OUTPUT LOAD

1. Although the ADP1821 Reference Design can sustain the sudden connection of the load, it is possible to damage the load if it is not properly connected.
2. Make sure that the power source is turned off before connecting the load.
   a) If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board with the positive (+) load connection to the V_O terminal and negative (−) load connection to the GND terminal next to V_O.
   b) If an ammeter is used, connect it in series with the load; connect the positive (+) ammeter terminal to the evaluation board V_O terminal, the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board GND terminal next to V_O.

Once the load is connected, make sure that it is set to the proper current before powering the ADP1821 Reference Design.

INPUT AND OUTPUT VOLTMETERS

Measure the input and output voltages with voltmeters.

1. Connect the voltmeter measuring the input voltage with the positive (+) lead connected to the VIN terminal on the test board and the negative lead (−) connected to the GND terminal next to VIN.
2. Connect the voltmeter measuring V_{OUT} with the positive lead (+) connected to the V_O terminal and the negative lead (−) connected to the adjacent GND terminal.
3. Make sure to connect the voltmeters to the appropriate evaluation board test points and not to the load or power source themselves.
4. If the voltmeters are not connected directly to the evaluation board at these connection points, the measured voltages will be incorrect due to the voltage drop across the leads connecting the evaluation board to both the source and load.

TURNING ON THE EVALUATION BOARD

Once the power source and loads are connected to the ADP1821 Reference Design, the board can be powered for operation. Slowly increase the input power source voltage until the input voltage exceeds the minimum input operating voltage of 9 V. If the load is not already enabled, enable the load and check that it is drawing the proper current and that the output voltage maintains voltage regulation.

TYPICAL PERFORMANCE CHARACTERISTICS

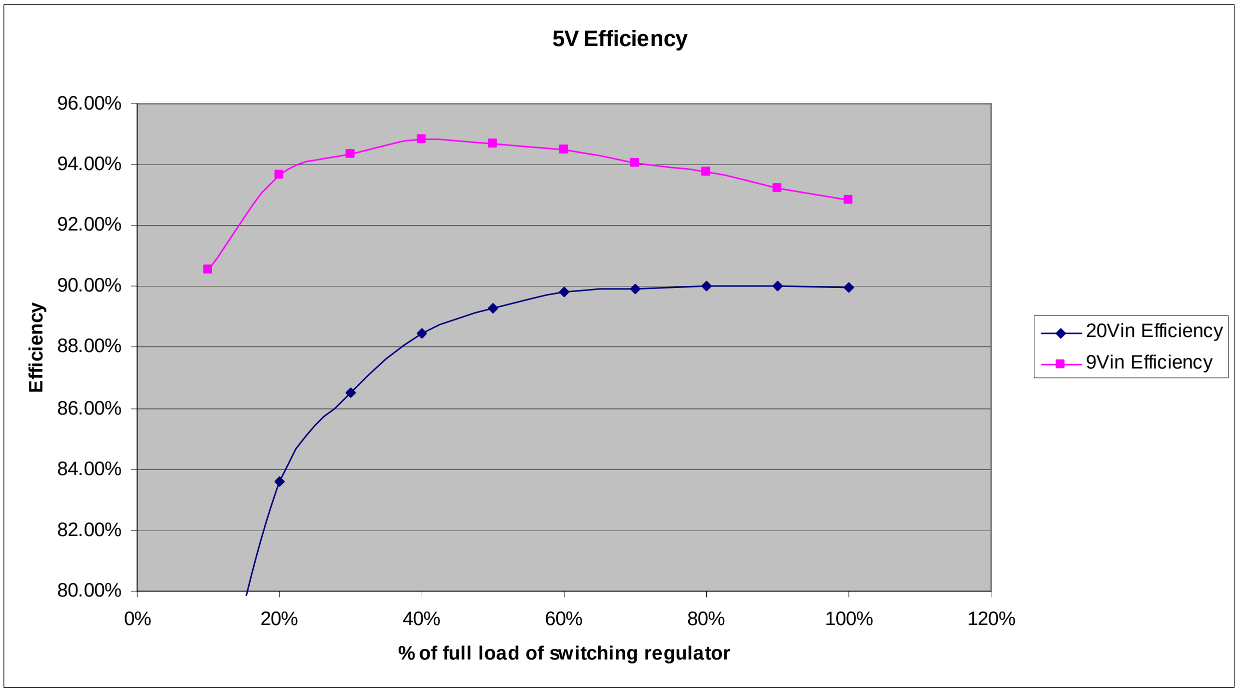
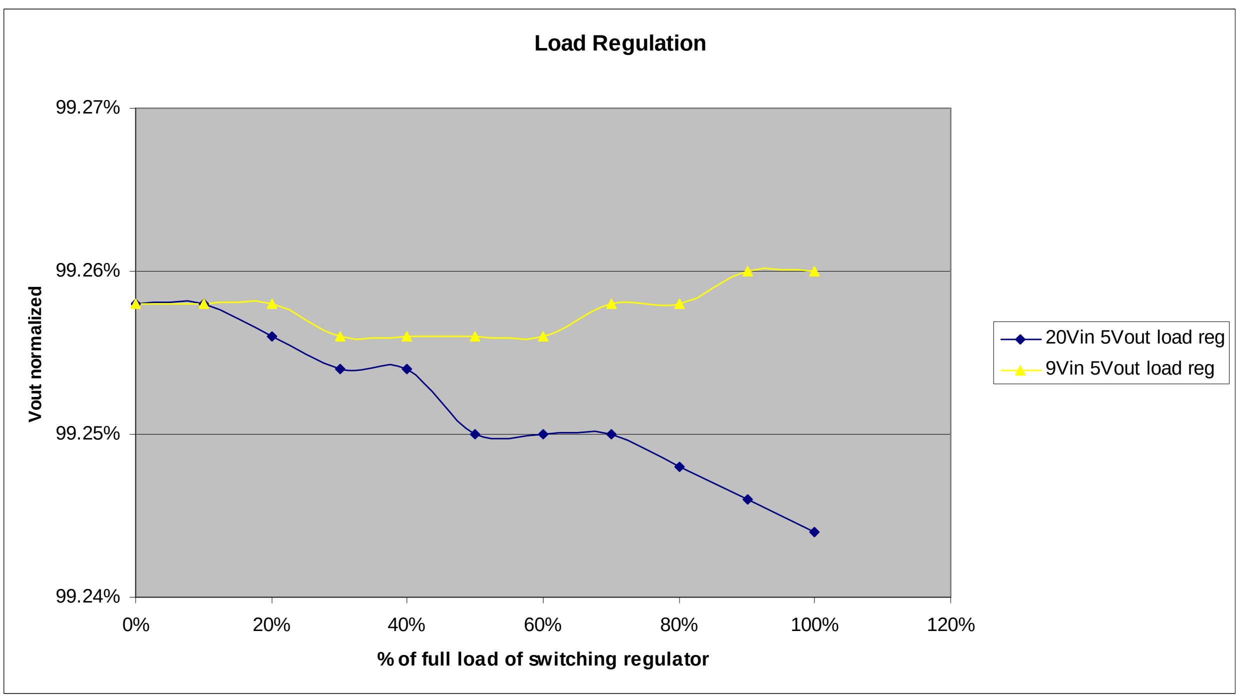


Figure 4. Efficiency



Normalized Load Regulation

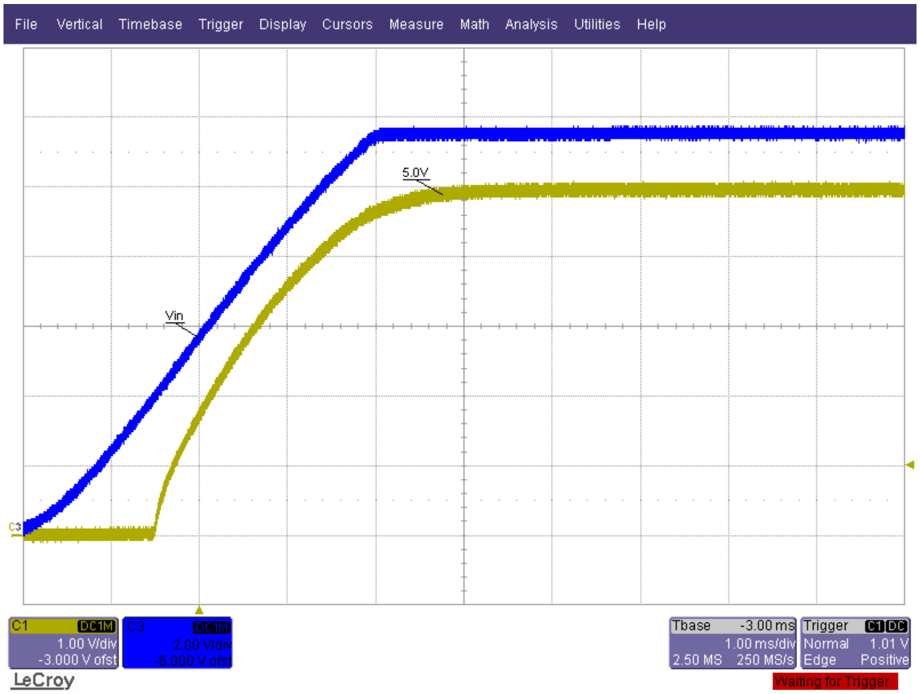


Figure 5. Switching regulator turn on at no load: Ch1 = 5.0 V, Ch3 = Vin

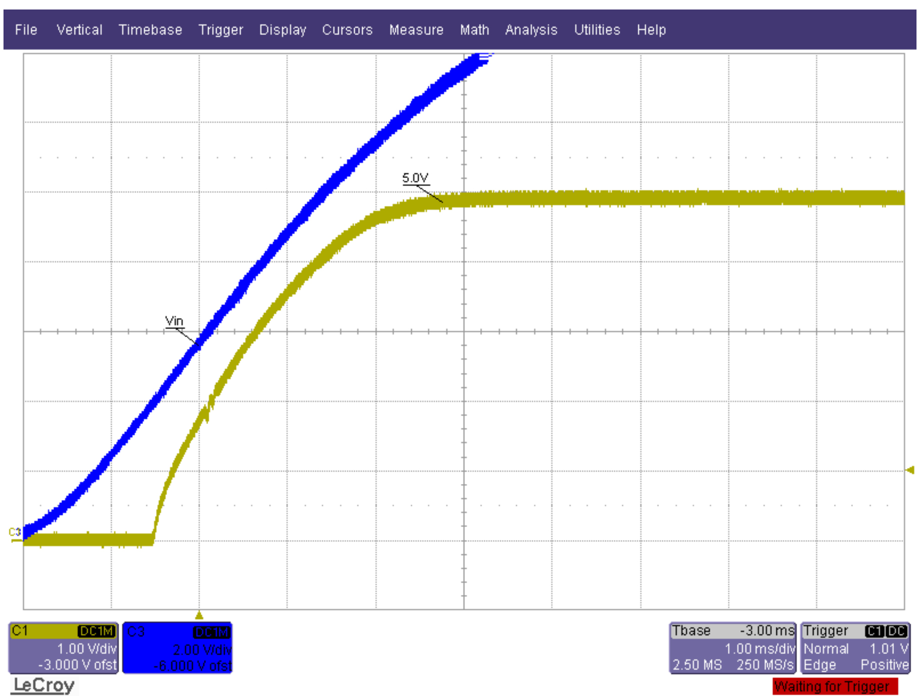


Figure 6. Switching regulator turn on at full load: Ch1 = 5.0 V, Ch3 = Vin

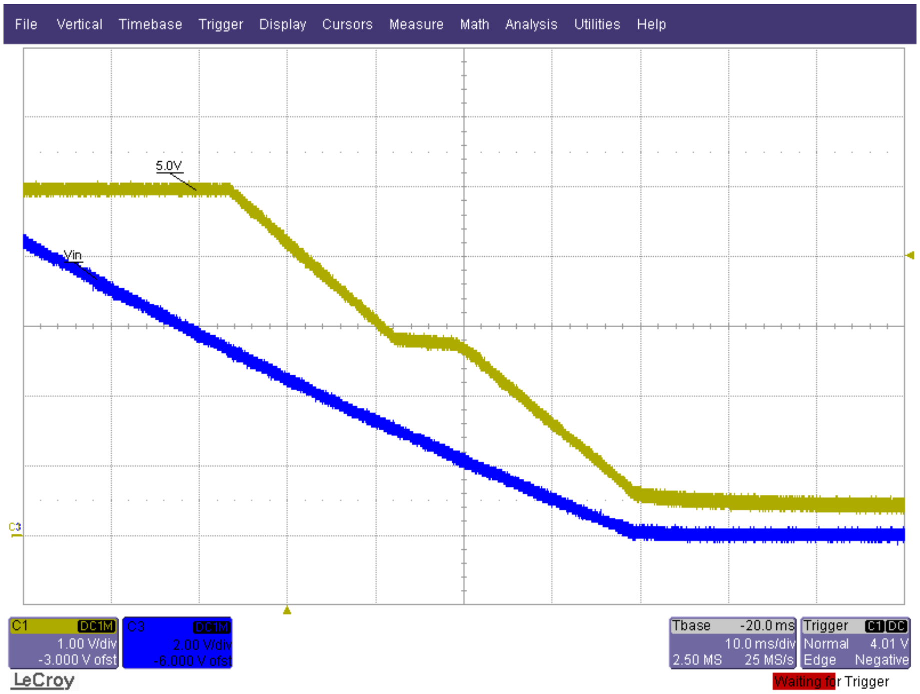


Figure 7. Switching regulator turn off at no load: Ch1 = 5.0 V, Ch3 = Vin

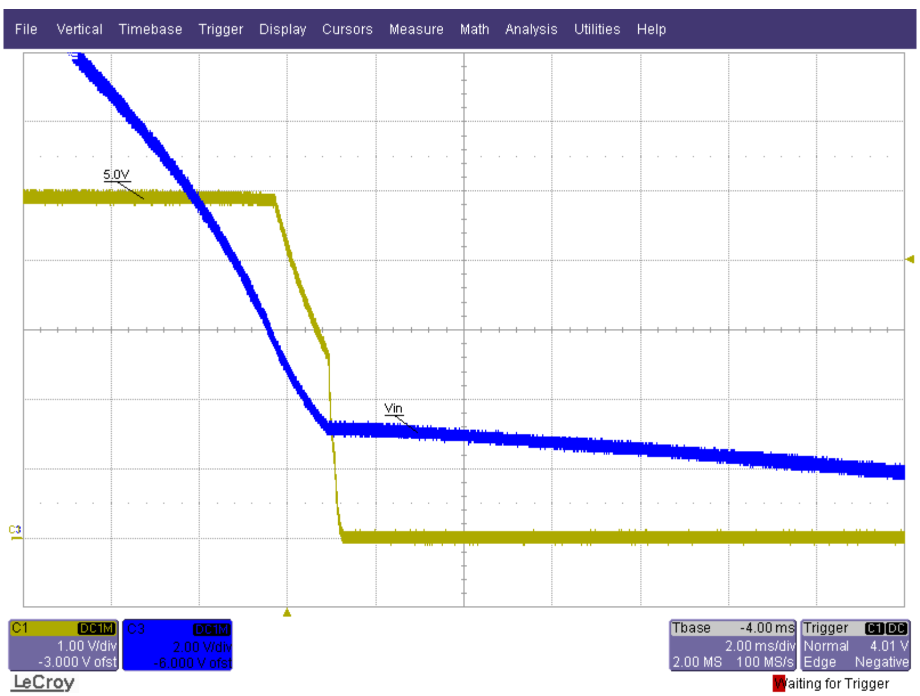


Figure 8. Switching regulator turn off at full load: Ch1 = 5.0 V, Ch3 = Vin

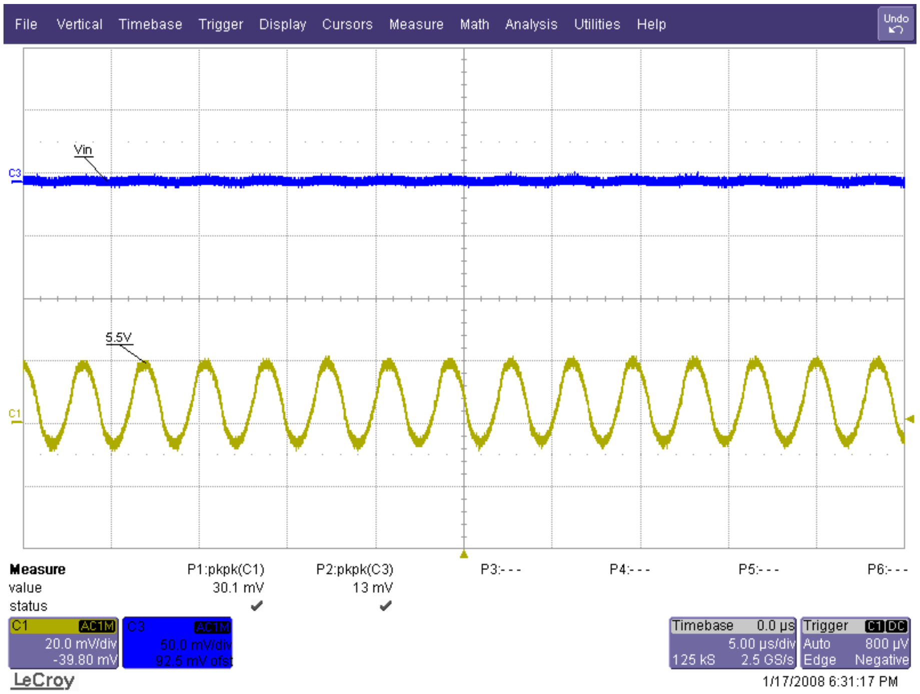


Figure 9. Switching regulator ripple and noise at no load: Ch1 = 5.0 V, Ch3 = Vin @ 9.0 V

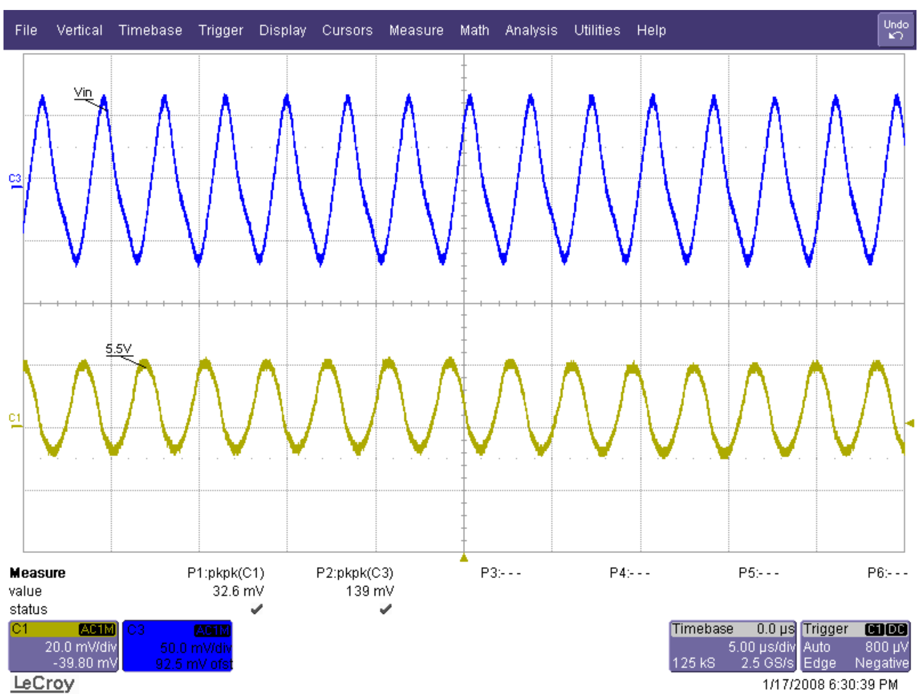


Figure 10. Switching regulator ripple and noise at full load: Ch1 = 5.0 V, Ch3 = Vin @ 9.0 V

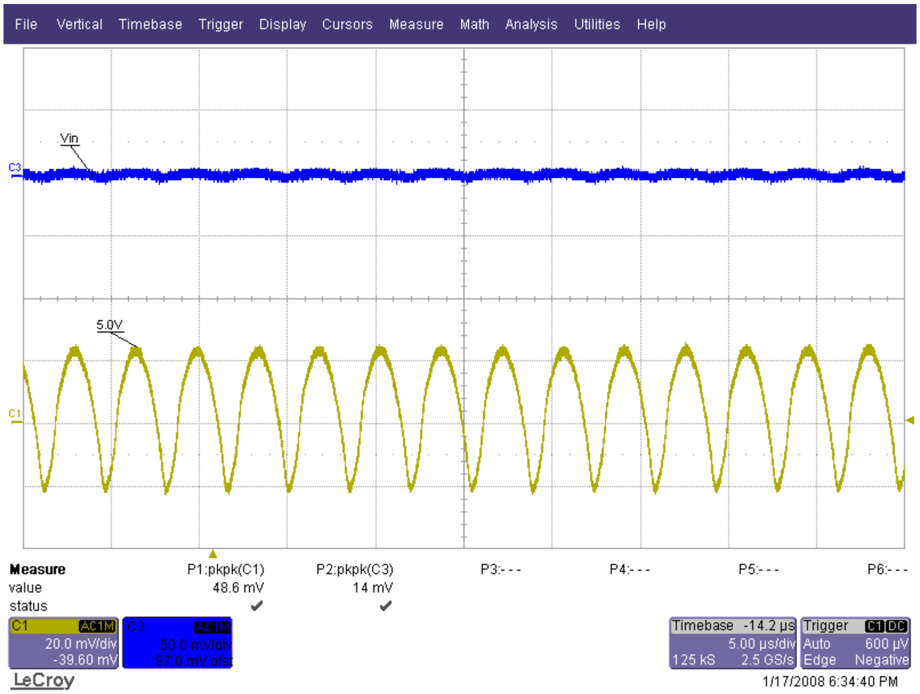


Figure 11. Switching regulator ripple and noise at no load: Ch1 = 5.0 V, Ch3 = Vin @ 20.0 V

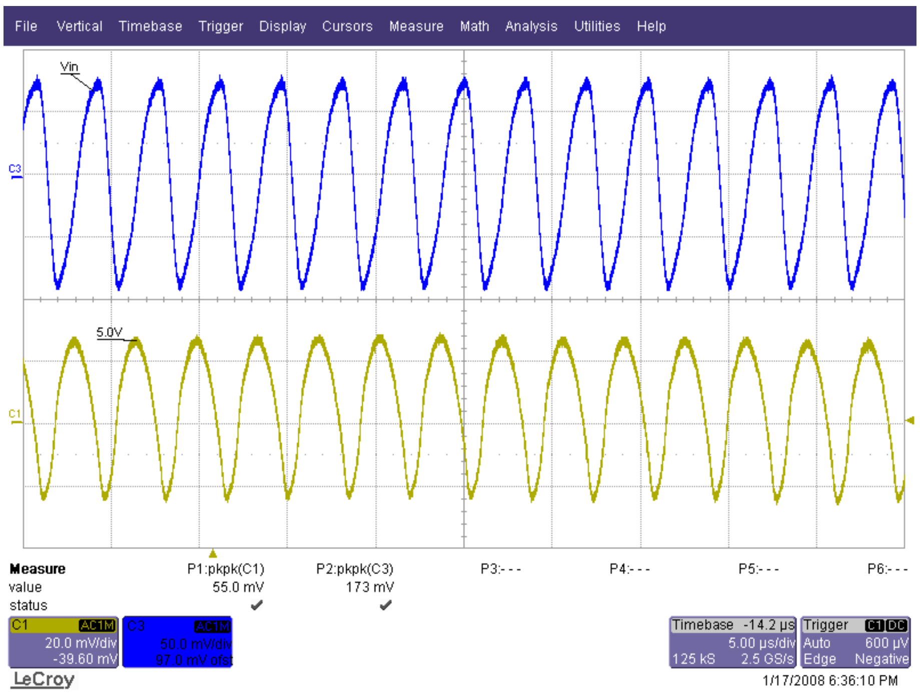


Figure 12. Switching regulator ripple and noise at full load: Ch1 = 5.0 V, Ch3 = Vin @ 20.0 V

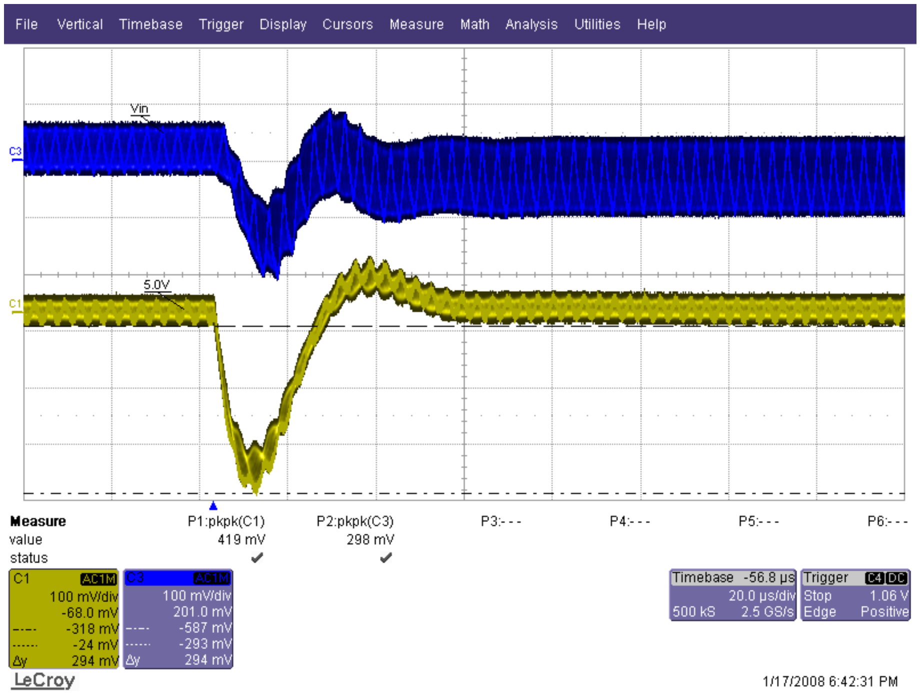


Figure 13. Transient 50% to 100% load: Ch1 = 5.0 V, Ch3 = Vin @ 9.0 V

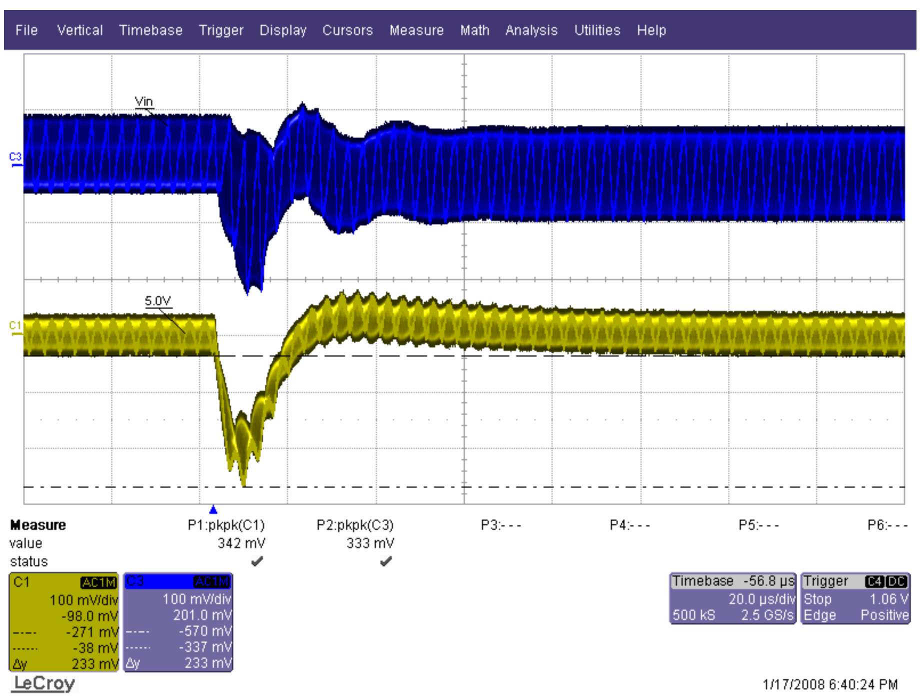


Figure 14. Transient 50% to 100% load: Ch1 = 5.0 V, Ch3 = Vin @ 20.0 V

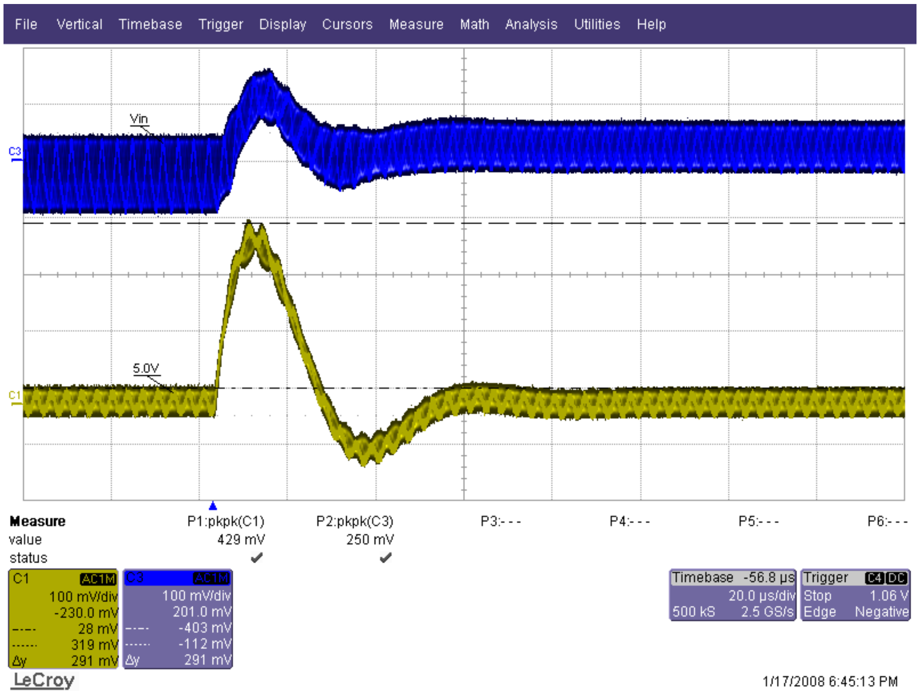


Figure 15. Transient 100% to 50% load: Ch1 = 5.0 V, Ch3 = Vin @ 9.0 V

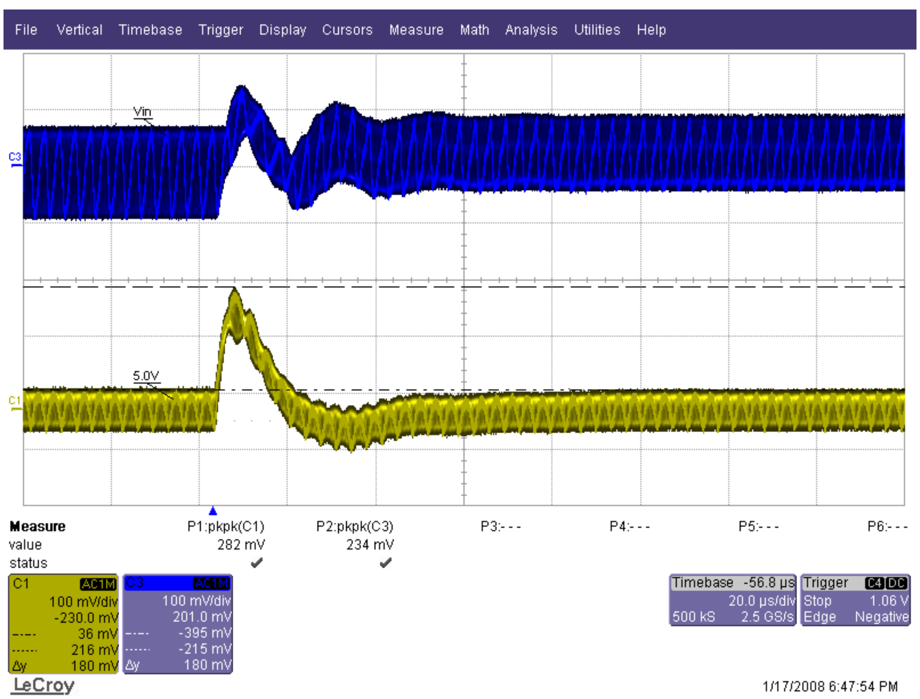


Figure 16. Transient 100% to 50% load: Ch1 = 5.0 V, Ch3 = Vin @ 20.0 V

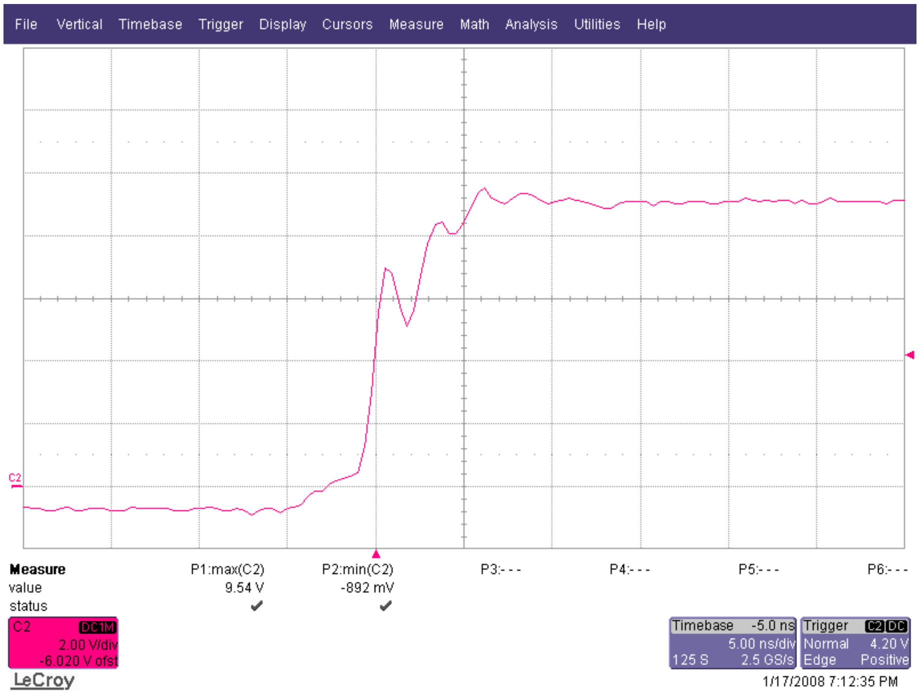


Figure 17. Switchnode Rising 100% load Vin @ 9 V: Ch2 = Drain to Source of QL1

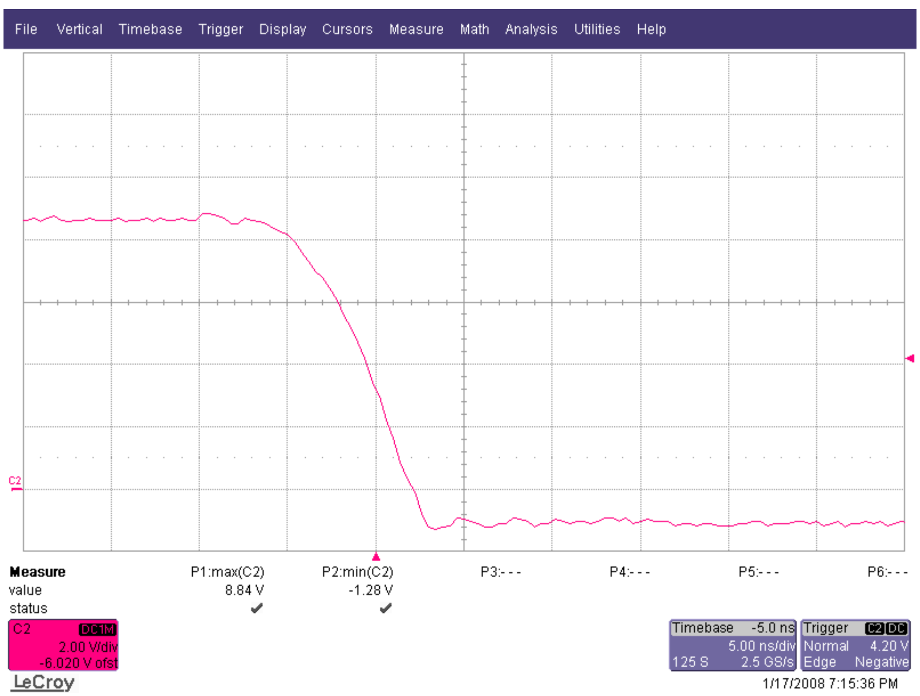


Figure 18. Switchnode Falling 100% load Vin @ 9 V: Ch2 = Drain to Source of QL1

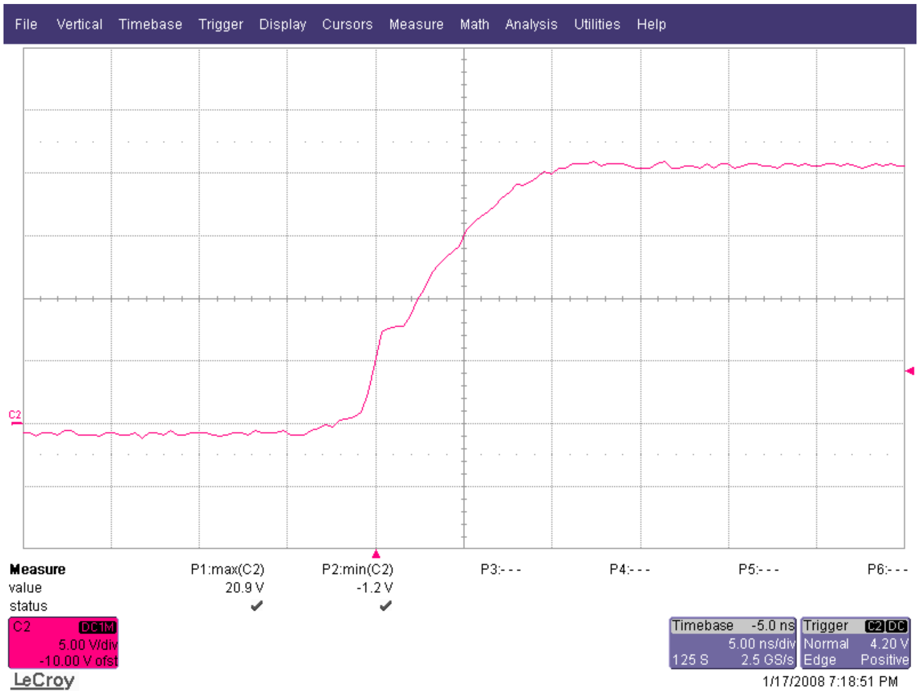


Figure 19. Switchnode Rising 100% load Vin @ 20 V: Ch2 = Drain to Source of QL1

Figure 20. Switchnode Falling 100% load Vin @ 20 V: Ch2 = Drain to Source of QL1

NOTES

The unnamed terminals adjacent to Vo and GND can be used to connect a common mode choke to the output. Simply move the Vout and GND connections to the dummy terminals and connect the common mode choke between Vo and GND and the dummy terminals.

Lout was meant to be populated with a low inductance ferrite bead. If it is necessary to populate this component to meet EMI then the loop compensation may need to be adjusted to guarantee stability.