

Evaluating the **ADP1972** Buck or Boost, PWM Controller for Battery Test Solutions

FEATURES

Evaluation board for testing the features of the **ADP1972**
Standalone open-loop capability
FAULT and COMP inputs compatible with the **AD8450-EVALZ**
Compatible for testing with full external customer solutions
Input voltage range: 6 V to 60 V
On-board 5 V low dropout (LDO) regulator
Selective buck or boost mode
Adjustable frequency from 50 kHz to 300 kHz
Synchronization output or input with adjustable phase shift
Programmable maximum duty cycle
Maximum internal duty cycle: 98%
Programmable soft start
Peak hiccup current limit protection
Input voltage UVLO protection
Jumper for enable/shutdown control

EVALUATION KIT CONTENTS

ADP1972-EVALZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

Power supplies
Digital multimeters
Oscilloscope
Signal generator

ONLINE RESOURCES

Documents

[ADP1972](#) data sheet
[ADP1972-EVALZ](#) user guide
[AD8450](#) data sheet

Design and integration files

Schematics, layout files, and bill of materials
Frequently asked questions (FAQs) and troubleshooting

GENERAL DESCRIPTION

The **ADP1972-EVALZ** is an open-loop evaluation board that can be used to test the features of the **ADP1972**. The **ADP1972** is a constant frequency, voltage mode, pulse-width modulation (PWM) controller for buck or boost, dc-to-dc, asynchronous battery charge and discharge applications. When connected to external, high voltage field effect transistors (FET); a half bridge driver; and an external control device, such as the **AD8450-EVALZ**, the **ADP1972-EVALZ** can be used to evaluate the **ADP1972** in a complete closed-loop application.

This user guide includes input/output descriptions, setup instructions, the schematic, and the printed circuit board (PCB) layout drawings for the **ADP1972-EVALZ** evaluation board.

The **ADP1972-EVALZ** can be used to test internal features such as precision enable, pin selective battery charge or recycle mode operation, internal and external frequency synchronization control with programmable phase shift, PWM duty cycle control, programmable maximum duty cycle, and programmable peak hiccup current limit. Additional protection features that can be evaluated include soft start, input voltage undervoltage lockout (UVLO), fault signaling, and thermal shutdown (TSD).

Complete specifications for the **ADP1972** are available in the **ADP1972** data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

11/14—Revision 0: Initial Version

TYPICAL SETUP FOR OPEN-LOOP EVALUATION

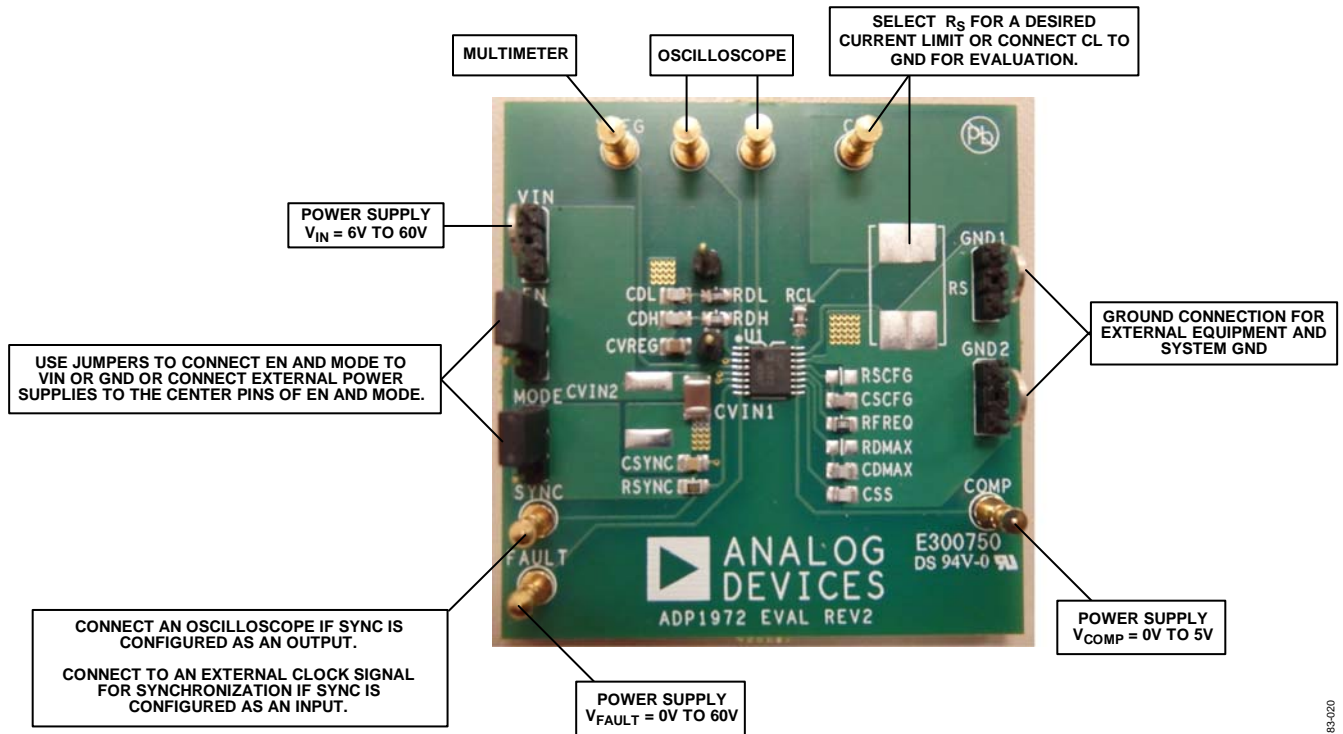


Figure 1.

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EVALUATION BOARD SETUP PROCEDURES

The [ADP1972-EVALZ](#) has many features that are customizable via the resistors and capacitors on the evaluation board. Other features are observable by adjusting the voltages applied to several of the pins. Most features can be initially observed without making any physical changes to the board, with the exception of R_S . If no R_S is added, CL must be shorted to GND for most tests. If testing the current-limit functionality, R_S must be mounted to the evaluation board. The steps in the following sections describe how to use the [ADP1972-EVALZ](#) evaluation board.

QUICK START STEPS

To begin using the evaluation board, connect the external equipment as described in the following sections.

GNDx Test Loop

The GND1 and GND2 test loops are the power ground connection for the device via the GND pin and the external bypass capacitors. Connect the ground connections from the external equipment to this bus.

VIN Test Loop

Connect an external power supply from to VIN to GND1 or GND2. The VIN test loop connects the positive input supply voltage to the VIN pin. Connect the power supply to this bus and keep the wires as short as possible to minimize the EMI transmission.

EN Test Bus

The EN test bus is used to enable/disable the [ADP1972](#) via the EN pin. Use one of the following methods to control the [ADP1972](#). Do not leave the EN pin floating.

- Use a jumper to connect the top two pins of the EN test bus. This jumper connects EN to VIN and enables the [ADP1972](#) (see Figure 2).

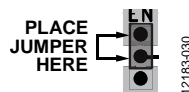


Figure 2. Enabled Jumper Position

- Use a jumper to connect the bottom two pins of the EN test bus. This jumper connects EN to GND and disables the [ADP1972](#) (see Figure 3).

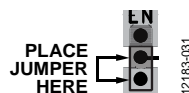


Figure 3. Disabled Jumper Position

- Alternatively, connect a voltage between 0 V and 60 V to the center pin of the EN test bus for independent control of the EN pin voltage (see Figure 4). The [ADP1972](#) is enabled when $V_{EN} \geq 1.25$ V (typical).



Figure 4. EN Pin Direct Connection

VREG Test Point

Connect a multimeter from VREG to GNDx. When $V_{EN} \geq 1.25$ V (typical), VREG rises to 5 V (typical).

MODE Test Bus

The MODE test bus is used to set the [ADP1972](#) in buck or boost mode. Do not leave the MODE pin floating.

The state of the MODE pin can only be changed when the [ADP1972](#) is disabled via the EN pin or disabled due to a fault condition.

- Use a jumper to connect the top two pins of the MODE bus. This jumper connects MODE to VREG and places the [ADP1972](#) in buck/charge mode (see Figure 5).

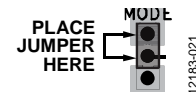


Figure 5. Enabled Jumper Position

- Use a jumper to connect the bottom two pins of the MODE test bus. This jumper connects MODE to GND and places the [ADP1972](#) in boost/recycle mode (see Figure 6).

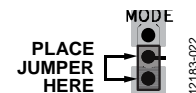


Figure 6. Disabled Jumper Position

- Alternatively, connect a voltage between 0 V and 5.5 V to the center pin of the MODE test bus for independent control of the MODE pin voltage (see Figure 7). The MODE pin is logic high when $V_{MODE} \geq 1.20$ V (typical).

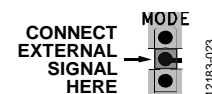


Figure 7. MODE Pin Direct Connection

FAULT Test Point

Connect FAULT to VIN or apply an external voltage between 0 V and 60 V. If SYNC is configured as an output, when $V_{FAULT} \geq 1.2$ V (typical), a square wave is visible on the SYNC pin operating at the frequency set by R_{FREQ} .

SYNC Test Point

If SYNC is configured as an output, connect an oscilloscope to SYNC. The SYNC signal is visible when $V_{EN} \geq 1.25$ V (typical) and $V_{FAULT} \geq 1.2$ V (typical).

If SYNC is configured as an input, connect a signal with f_{SW} between 50 kHz and 300 kHz, with $V_{SYNC(HIGH)} \geq 1.2$ V (typical) and $V_{SYNC(LOW)} \leq 1.05$ V (typical).

COMP Test Point

Connect an external power supply to COMP. See Figure 8 for the relationship between V_{COMP} and the switching duty cycle of DH and DL.

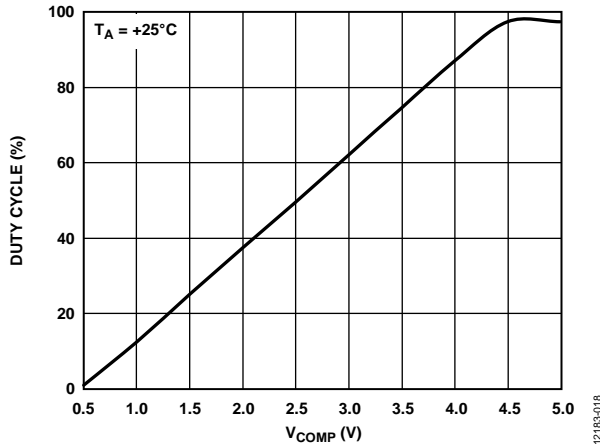


Figure 8. Duty Cycle vs. V_{COMP} , $R_{FREQ} = 100$ k Ω , No Load on DL, DH, or DMAX

DL and DH Test Point

Connect the DH and DL pins to an oscilloscope. To observe a signal on DH or DL, enable the ADP1972 via the EN pin by setting $V_{EN} \geq 1.25$ V (typical), $V_{FAULT} \geq 1.2$ V (typical), and $V_{COMP} \geq 0.5$ V (typical).

If $V_{MODE} \leq 1.05$ V (typical), the ADP1972 is in boost/recycle mode, and a square wave is visible on the DL pin.

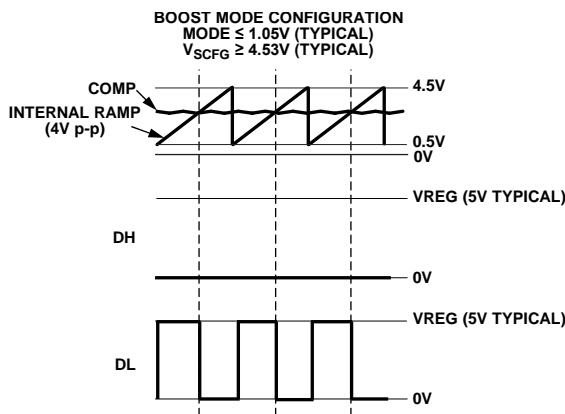


Figure 9. Signal Diagram for Boost Configuration

If $V_{MODE} \geq 1.20$ V (typical), the ADP1972 is in buck/charge mode, and a square wave is visible on the DH pin.

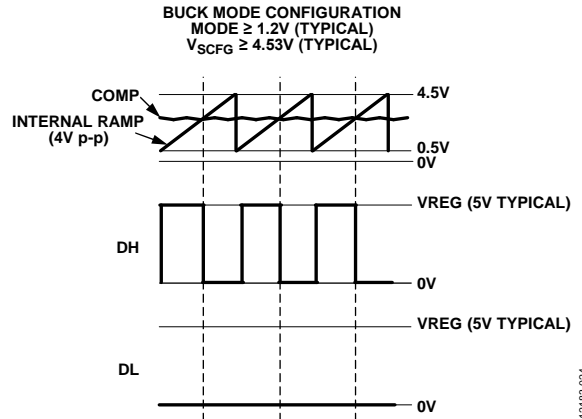


Figure 10. Signal Diagram for Buck Configuration

CL Test Point

Unless testing the current limit, connect CL to GND1 or GND2. If testing the current, see the Current Limit section and Selecting R_s to Set the Current Limit section in the ADP1972 data sheet for more information.

ADJUSTING THE ADP1972-EVALZ COMPONENTS FOR YOUR APPLICATION

For more detailed guidance in selecting the components to customize the features of the ADP1972, consult the ADP1972 data sheet.

Phase Shift Resistor (R_{SCFG})

If a phase shift from SYNC to DH and DL is desired, select R_{SCFG} for the desired time delay using Figure 11 as reference.

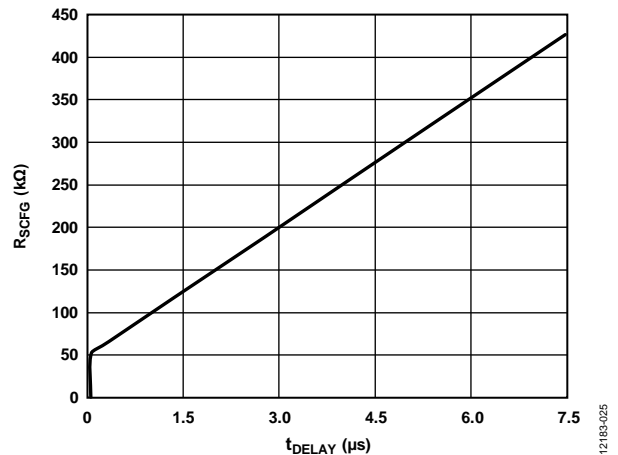


Figure 11. R_{SCFG} vs. Phase Delay, $R_{FREQ} = 100$ k Ω

Frequency Set Resistor (R_{FREQ})

To set the switching frequency when using the ADP1972 as a master device, see Figure 12 for reference. When operating the ADP1972 as a slave device, consult the ADP1972 data sheet.

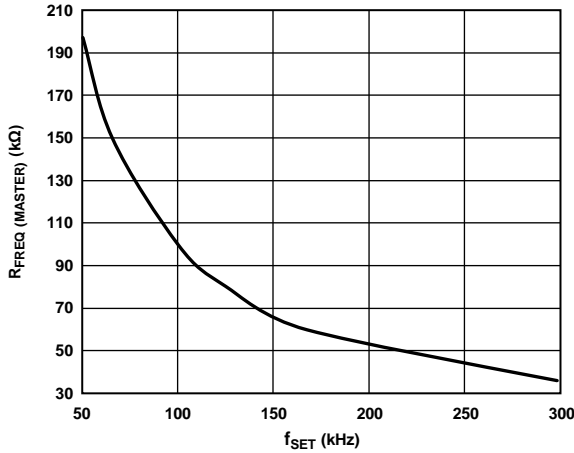


Figure 12. $R_{FREQ(MASTER)}$ vs. Switching Frequency (f_{SET})

Maximum Duty Cycle Resistor (R_{DMAX})

To customize the maximum duty cycle of the DH and DL pins for the ADP1972, use Figure 13 to select R_{DMAX} .

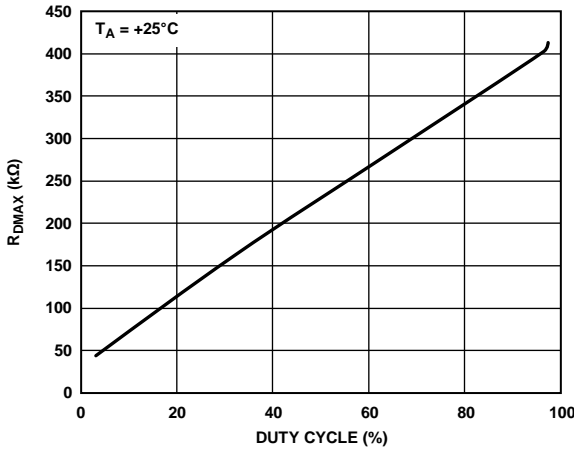


Figure 13. R_{DMAX} vs. Duty Cycle, $R_{FREQ} = 100\text{ k}\Omega$, $V_{COMP} = 5\text{ V}$

Current Limit Set Resistor (R_S)

If testing the current limit in an application, use the following equation to set the current limit:

$$I_{PK} \text{ (mA)} = \frac{100 \text{ mV}}{R_S} \tag{1}$$

where:

I_{PK} is the desired peak current limit in mA.

R_S is the sense resistor used to set the peak current limit in Ω .

When the ADP1972 is configured to operate in buck/charge mode, the internal current-limit reference is set to 300 mV (typical). When the ADP1972 is configured to operate in boost/recycle mode, the internal current-limit reference is set to 500 mV (typical). The external resistor, R_{CL} , is needed to offset the current properly to detect the peak in both buck and boost operation. Set the value of R_{CL} to 20 k Ω . In operation, the equations for setting the peak current are as follows.

For buck/charge mode, the equation is

$$V_{REF(BUCK)} = I_{CL} \times R_{CL} - I_{PK} \times R_S \tag{2}$$

For boost/recycle mode, the equation is

$$V_{REF(BOOST)} = I_{CL} \times R_{CL} + I_{PK} \times R_S \tag{3}$$

where:

$V_{REF(BUCK)} = 300\text{ mV}$, typical.

$V_{REF(BOOST)} = 500\text{ mV}$, typical.

$I_{CL} = 20\text{ }\mu\text{A}$, typical.

$R_{CL} = 20\text{ k}\Omega$.

The ADP1972 is designed so that the peak current limit is the same in both the buck mode and boost mode of operation. A tolerance of 1% or better for the R_{CL} and R_S resistors is recommended.

Soft Start Capacitor (C_{SS})

The ADP1972-EVALZ comes with a 1 nF capacitor on the evaluation board.

A C_{SS} capacitor is not required for the ADP1972. When the C_{SS} capacitor is not used, the internal 5 μA (typical) current source pulls the SS pin voltage to VREG, and there is no soft start control. Use the following equation to calculate the delay time before switching is enabled (t_{REG}).

$$t_{REG} = \frac{0.52}{I_{SS}} \times C_{SS} \tag{4}$$

where $I_{SS} = 5\text{ }\mu\text{A}$, typical.

APPLICATION SPECIFIC ADP1972 CONTROL

When integrated in a battery test solution, the ADP1972 can be controlled with external control signals from other devices in the application. The FAULT pin allows an external device to signal the ADP1972 when an external fault occurs. The COMP pin allows an external device to control the PWM output signals on the DH and DL pins. The SYNC and SCFG pins can be used to synchronize the ADP1972 to an external clock signal or to implement the ADP1972 as a master clock. The EN and MODE pins provide logic control to turn the ADP1972 on or off and to transition the system between boost/recycle mode and buck/charge mode.

EVALUATION BOARD HARDWARE

TYPICAL APPLICATION CIRCUIT

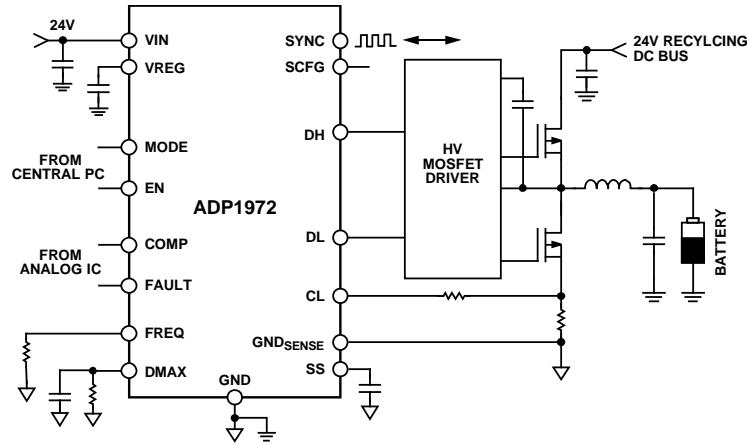


Figure 14. ADP1972 Typical Application Circuit

Table 1. Input Pins that Require External Power Supplies or External Control Signals

Power Supply	Connector	Voltage Range (V)	Purpose
V_{IN}^1	VIN	6 to 60	Supplies power to the ADP1972 internal control circuitry.
V_{EN}^1	EN	0 to 60	Supplies logic signal to enable operation of the ADP1972.
V_{MODE}^1	MODE	0 to 5.5	Supplies logic signal to select boost/recycle mode or buck/charge mode.
V_{FAULT}^2	FAULT	0 to 60	Supplies the signal to indicate when a fault condition has occurred in the application external to the ADP1972.
V_{COMP}^3	COMP	0.5 to 5.0	Supplies the error signal that is compared internally to the liner ramp to produce the PWM signal.
V_{SYNC}	SYNC	0 to 5.5	Supplies the external synchronization waveform when the ADP1972 is a slave device, and SYNC is configured as an input.

¹ V_{IN} can also be used to supply V_{EN} and V_{MODE} via jumper connections. Alternatively, EN and MODE can be powered with separate power supplies.

² When used with the AD8450, the FAULT signal is supplied by the FAULT pin (Pin 46) of the AD8450.

³ When used with the AD8450, the COMP signal is supplied by the VCTRL pin (Pin 59), the error amplifier output of the AD8450.

Table 2. Output Pins to Observe with Ammeter or Oscilloscope

Output Signal	Connector	Signal	Recommended Equipment	Expected Measurement
V_{VREG}^1	VREG	5 V dc	Ammeter or oscilloscope	When $V_{IN} > 6 V$, V_{VREG} rises to 5 V.
V_{DL}	DL	0 V to VREG square wave	Oscilloscope	When MODE is logic low, a square wave is visible on DL. When mode is logic high, $V_{DL} = 0 V$.
V_{DH}	DH	0 V to VREG square wave	Oscilloscope	When MODE is logic high, a square wave is visible on DH. When mode is logic low, $V_{DH} = 0 V$.
V_{SYNC}	SYNC	0 V to VREG square wave	Oscilloscope	When SYNC is configured as an output, the SYNC pin outputs a clock signal programmed by R_{FREQ} .
I_{CL}	CL	Magnitude dependent on R_s triangle wave	Oscilloscope	The current rises and falls with the duty cycle of DH and DL.

¹ V_{VREG} provides the logic high signal for the MODE pin when a jumper is placed on the top two pins of the MODE test bus.

EVALUATION BOARD SCHEMATIC AND LAYOUT

SCHEMATIC

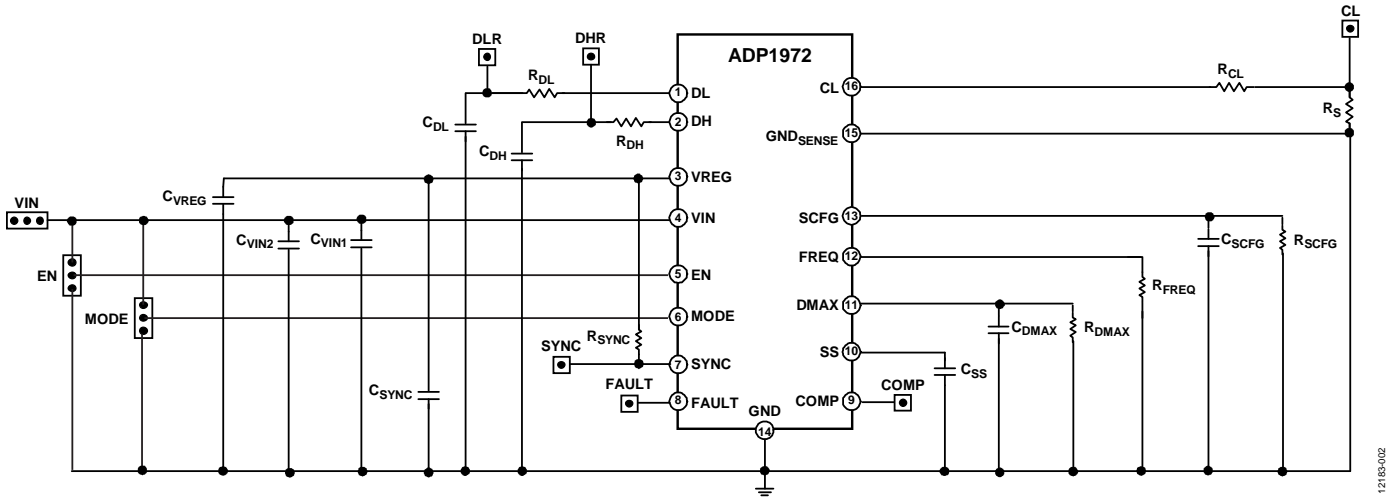


Figure 15. ADP1972 Evaluation Board Schematic

PCB LAYOUT

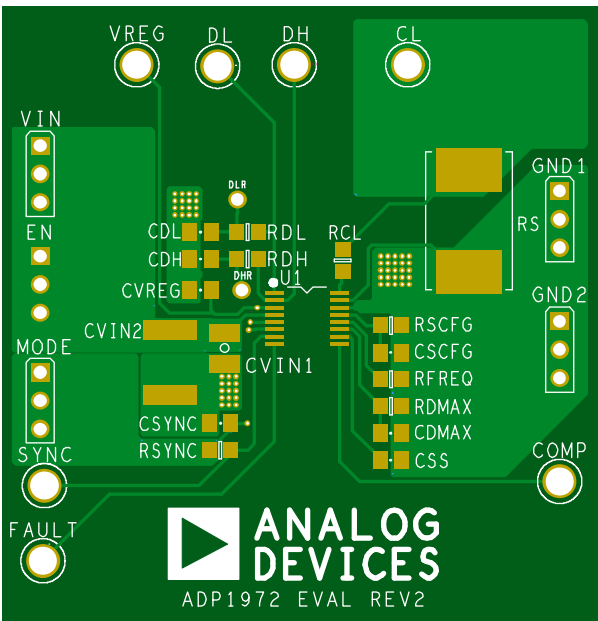


Figure 16. ADP1972 Evaluation Board PCB Top Layer

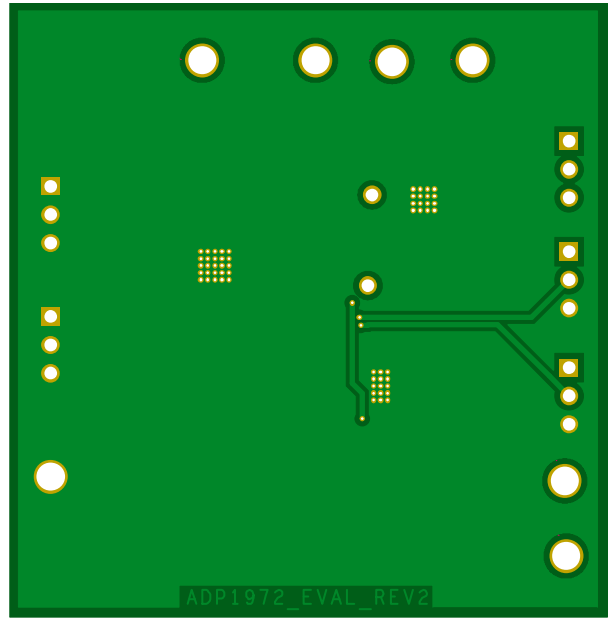


Figure 17. ADP1972 Evaluation Board PCB Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Manufacturer ¹	Part Number
1	U1	ADP1972 buck or boost, PWM controller	Analog Devices, Inc.	ADP1972ARUZ-RL
2	CDL, CDH	Bypass capacitors for logic DL and DH pins, 1000 pF, 10 V, 0805	Kemet	C0805C102K8RACTU
2	RDL, RDH	Signal integrity resistor, 20 Ω , 0805, $\pm 1\%$	Vishay Dale	CRCW080520R0FKEA
1	CVREG	Bypass capacitor for internal LDO, 1 μ F, 6.3 V, 0805	TDK Corporation	CGJ4J2X7R0J105K125AA
1	CVIN1	Input voltage bypass capacitor, 4.7 μ F, 100 V, 10%, X7S, 1210	TDK Corporation	C3225X7S2A475K200AB
	CVIN2	Input voltage bypass capacitor	Open	
1	CSYNC	SYNC pin bypass capacitor, 0.1 μ F, 6.3 V, 0805	Kemet	C0805C104K9RACTU
1	RSYNC	SYNC pin resistor, 1 k Ω , 0805, $\pm 1\%$	Vishay Dale	CRCW08051K00FKEA
1	RCL	Current limit offset sense resistor, 20 k Ω , 0805, $\pm 1\%$	Vishay Dale	CRCW080520K0FKEA
	RS	Current limit set resistor	Open	
1	RSCFG	Synchronization pin control resistor	Open	
2	CSCFG, CDMAX	SCFG and DMAX pin bypass capacitors, 47 pF, 50 V, 0805	Kemet	C0805C470J5GACTU
1	RFREQ	Frequency set resistor, 100 k Ω , 0805, $\pm 1\%$	Vishay Dale	CRCW0805100KFKEA
1	RDMAX	Maximum duty cycle set resistor	Open	
1	CSS	External soft start capacitor, 1000 pF	Kemet	C0805C102K8RACTU
3	VIN, GND1, GND2	Test point loop connectors	Aavid Thermalloy	125800D00000G
2	EN, MODE	Headers, 0.100 inches, single, straight, 3-pin	Sullins Connector Solutions	PBC03SAAN ²
2	DLR, DHR	Headers, 0.100 inches, single, straight, 1-pin	Sullins Connector Solutions	PBC01SAAN ²
7	VREG, DL, DH, CL, COMP, SYNC, FAULT	Single-end, double turret	Keystone Electronics	1502-2
2	EN, MODE	Connector, jumper, shorting, gold	Sullins Connector Solutions	SSC02SYAN

¹ Equivalent substitutions may be made for all passive components and connectors.

² Alternatively, PBC36SAAN can be purchased and cut as necessary.

RELATED LINKS

Resource	Description
ADP1972	Buck or boost, PWM controller for battery test solutions
AD8450	Precision analog front end and controller for battery test/formation systems

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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