Circuits from the Lab Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN282.

Devices Connected/Referenced	
ADV7611	Low Power 165 MHz HDMI Receiver
ADV7125	Triple 8-Bit High Speed Video DAC
SSM2604	Low Power Audio Codec
ADuC7020	Analog Microcontroller
ADP2301	Step-Down Switching Regulator

USB Powered DVI/HDMI-to-VGA Converter (HDMI2VGA) with Audio Extraction

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a complete solution for the conversion of HDMI/DVI to VGA (HDMI2VGA) with an analog audio output. It uses the low power ADV7611 high-definition multimedia interface (HDMI) receiver capable of receiving

video streams up to 165 MHz. The circuit is powered from a USB cable and works for resolutions up to 1600 × 1200 at 60 Hz.

The circuit uses extended display identification data (EDID) content to ensure that the video stream from the HDMI/digital visual interface (DVI) source is at the highest possible resolution supported by the HDMI source, converter, and video graphics adapter (VGA) display.
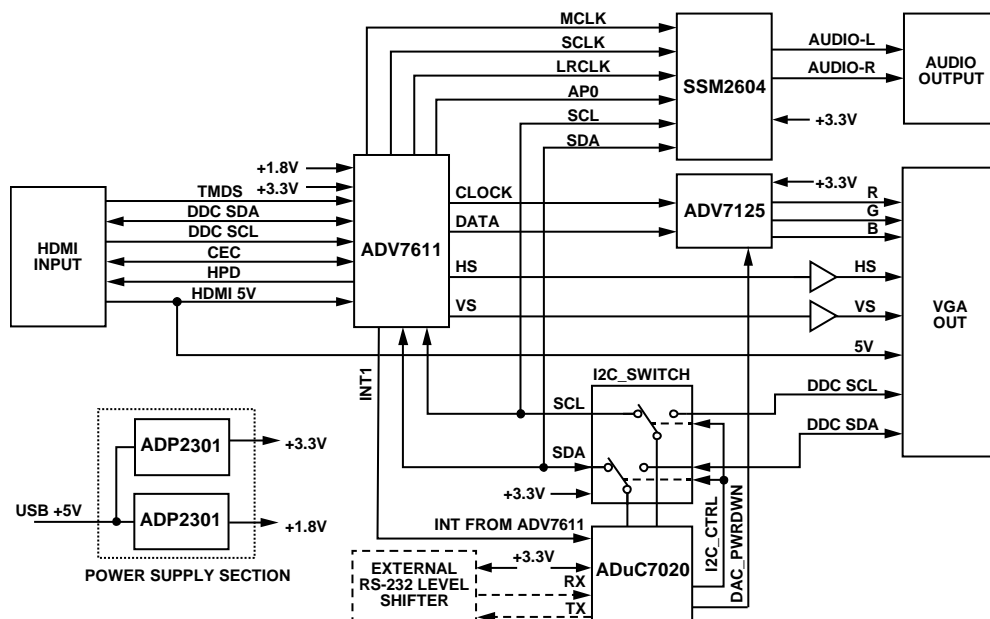

Figure 1. HDMI-to-VGA (HDMI2VGA) Converter Block Diagram (Simplified Schematic: All Connections Not Shown)

Rev. 0

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The HDMI receiver can also be used for video adjustments, such as brightness or contrast, and the audio codec can be used to set the volume of the audio output.

There are numerous benefits of this circuit. The highly integrated video receiver allows video adjustments without the need for additional field-programmable gate arrays (FPGAs). A simple I^2C write can adjust brightness, contrast, or change the audio volume. Built-in EDID memory reduces the count of the parts and the real estate. Step-down switching regulators allow the circuit to be powered from a USB port. By using industry-standard interchip connections, direct connections can be made between the receiver, codec, and video digital-to-analog converter (DAC). The circuit was built on a 2-layer printed circuit board (PCB), and it works up to UXGA resolutions (1600×1200 at 60 Hz).

CIRCUIT DESCRIPTION

The ADV7611 provides the receiving solution for the HDMI inputs and has a 5 V cable detect, a hot plug detect line assertion, and DDC lines that are used for EDID purposes. The ADV7611 incorporates an internal EDID RAM that provides display capabilities for the HDMI source. The built-in color space converter (CSC) in this circuit converts any HDMI color space to an 8-bit RGB444 word suitable for driving the ADV7125 video DAC input. This covers conversion of the following colorspaces: RGB, YCrCb (601 and 709), XVYCC (601 and 709), and others specified by the HDMI specification. The ADV7611 is also capable of any conversion between the 444 and 422 sampling schemes.

The ADV7125 video DAC converts the digital receive stream to a VGA-compatible analog signal.

Audio processing within the converter starts with the ADV7611 that has a built-in audio packet extraction block. The part can output virtually any HDMI standard; however, the backend SSM2604 audio codec only accepts an I^2S stream carrying linear pulse-code modulation (LPCM) audio with a 44.1 kHz or 48 kHz sampling rate. To ensure such an I^2S stream is sent, the ADV7611 must provide an HDMI source with the appropriate EDID content that only indicates the LPCM capability.

The audio line output signal impedance is 100 Ω, and an additional power amplifier stage is required for headphone or speaker connection.

The circuit is controlled with an ADuC7020 microcontroller. The ADuC7020 uses I^2C SDA and SCL lines that are connected via an ADG736 switch to either of the VGA display data channel (DDC) lines or to the main I^2C bus. The switch allows separating the main I^2C bus from VGA I^2C DDC lines to minimize risk of any potential conflicts (in case the monitor shares DDC I^2C with other devices or failure of VGA DDC lines). The main I^2C bus contains the ADV7611 and the SSM2604 I^2C slave devices.

The ADuC7020 also has universal asynchronous receiver-transmitter (UART) lines. They are used along with a serial programming button (connected to P0.0) and reset button to program the on-chip flash memory with an executable. In normal operation, the UART interface can also be used as a debug output or terminal during software development. It requires an additional level shifter (for example, ADM3202) to connect to the PC using the RS232 standard. The ADuC7020 is also connected to the INT1 and $\overline{RESET}$ pins of ADV7611 and to the $\overline{PSAVE}$ pin of the ADV7125 to allow for video DAC control.

The board uses two ADP2301 step-down switching regulators to power the board from a 5 V USB power supply. The highly efficient regulators provide the 3.3 V and 1.8 V to the devices on the board.

Initializing Board

When the board is first powered up, it reads back the VGA EDID from the monitor, programs the ADV7611 for receiving the HDMI stream, and programs the SSM2604 to output the I^2S audio through its DAC.

Setting the EDID Content

The HDMI2VGA converter ensures that the proper video standard, acceptable by the video display, is sent over the HDMI link. The HDMI specification requires the HDMI source to check for supported HDMI sink video modes prior to sending the video stream. Once the HDMI source has read the EDID content, it can only choose standards supported by the video display, ideally the one preferred by the display. The EDID content is therefore critical to ensure that output video is acceptable to the display.

The audio standard is handled in a similar manner. The audio standards supported by the HDMI sink are listed in the EDID content. The HDMI source must send an audio stream that matches one of those listed in the EDID content.

The ADuC7020 is used to read the VGA content to determine the capabilities of the monitor. The VGA EDID of a typical monitor does not list audio capabilities and may contain video resolutions that are not supported by the ADV7611 (for example, pixel rates above 165 MHz and VESA 1920×1200 at 60 Hz).

Therefore, it is important to ensure that the EDID content transmitted to the HDMI source only contains video modes commonly supported by the ADV7611 and the VGA display.

EDID Preparation for the ADV7611

The initial source of the new EDID information sent to the HDMI source contains retrieved and modified EDID from the VGA monitor. Once retrieved, the VGA EDID has the following bytes copied to the internal ADuC7020 RAM for modifications. Once they are modified, they are provided to the HDMI source (via the ADV7611 internal EDID).

- Bytes[0:19], header information
- Bytes[19:24], basic display information
- Bytes[25:34], chromacity coordinates
- Bytes[35:37], established bitmap settings (all are supported by the ADV7611)

Byte 20 of the EDID (video input parameters) is modified to 0 to indicate that the HDMI2VGA converter is a digital video input.

Bytes[38:54] of the EDID contain standard timing information. To ensure that none of the modes listed exceeds the maximum pixel clock frequency of 165 MHz, each of the modes listed in the STD timing information block are calculated for pixel clock frequency using the following:

$$PCLK = (X\ Resolution + 1) \times (Y\ Resolution + 1) \times Vertical\ Refresh\ Rate$$

The previous equation estimates the minimum pixel frequency that must be used to transmit video. The estimate is based on the assumption that video contains only one horizontal sync pulse of only one pixel width per line and only one line of vertical blanking interval (VBI) per frame. In real-world applications, this type of video is not used, and the estimate is only an approximation. For accurate PCLK values, use look-up tables based on the actual VESA standards.

If the calculated PCLK frequency exceeds 165 MHz, the video mode is dropped from the EDID.

The next part of the EDID (Bytes[54:125]) is occupied by four blocks of descriptors ([54:71], [72:89], [90:107], and [108:125]). The application checks all four descriptors and identifies two types of descriptors:

- A detailed timing descriptor (at least one of the first two bytes is different than zero) for the pixel clock frequency
- A monitor range descriptor (the first two bytes are zero, and the fourth byte equals 253) for the maximum pixel clock frequency supported by the monitor

The detailed timing descriptor (DTD) indicates the native video timing for a monitor. The first two bytes contain the value of the pixel clock frequency. If it exceeds 165 MHz, the entire descriptor is replaced with a DTD block appropriate for a 640 × 480 at 60 Hz video mode.

The monitor range descriptor contains information about the maximum PCLK frequency that the monitor can handle. If it exceeds 165 MHz, it is set equal to 165 MHz.

The last block of the standard EDID contains two bytes

- Byte 126 gives the number of additional EDID blocks. The application overwrites this byte with a 1 to provide an additional EDID.
- Byte 127 is a checksum byte.

The additional EDID block (CEA-861 type) is 128 bytes long and contains information about the audio capabilities as well as describes 640 × 480 pixels as a supported video standard. The main purpose of this block is to inform the HDMI source about the audio capabilities: stereo LPCM, 44.1 kHz, 48 kHz, and 32 kHz, with front left and front right speakers. The CEA-861 block also contains additional information about supported video standards, such as YCbCr444 and YCbCr422, along with standard RGB.

For more details, refer to the C source code in the design support files at http://www.analog.com/CN0282-DesignSupport.

Detection of HDMI Source and VGA Display

The 5 V signal from the HDMI cable signal is used to notify the VGA monitor of incoming video. The ADuC7020 does not check for a VGA connection, assuming there is one. Monitor detection can be implemented by reading back the EDID content. IF there is no I²C acknowledge, it can be assumed that the monitor is not connected.

HDMI source detection is not required. Once the ADV7611 is programmed for receiving HDMI content, it works every time the cable is connected and when the input video standard is changed. When a cable disconnects, the HDMI receiver generates a blue screen at the last received video resolution.

HDMI source detection is done by the ADV7611. The status of the connection can be determined by reading back Register 0x6F in the IO Map (Device Address 0x98). Refer to the Hardware User Guide (UG-180).

Limitations of HDMI2VGA Converter

It is necessary to consider data content protection. The standard VGA signal is a nonencrypted video signal that can be recorded using an analog recorder and played back without any content protection mechanism in place. Therefore, a VGA video is not safe for copyrighted materials. Because the HDMI-to-VGA converter does not allow content protection of an originally copyrighted video stream, it should not be allowed to receive it.

The ADV7611 solves this problem. It has been released in two silicon versions: the ADV7611 and the ADV7611-P. The ADV7611 allows for decryption of encrypted content, and the ADV7611-P does not have that capability, and it can only receive unencrypted video content. The HDMI2VGA converter must use the ADV7611-P.

The circuit shown in Figure 1 can be modified and adapted to receive encrypted content within existing VGA monitors as long as it is modified in a way that does not allow the user to have easy access to the decrypted video stream.

Layout Considerations

Careful routing of the connections between the ADV7611BSWZ-P and the ADV7125BCPZ allow the circuit to be constructed on a 2-layer board. The board has been proven to work for video streams with a pixel clock frequency to 165 MHz. The bottom layer of the PCB is primarily a single solid ground plane, with a few traces routed to the bottom layer. Numerous vias connecting the top and bottom layer grounds minimize ground bounce due to current transient characteristics on boards with high speed signals. A photo of the top of the PCB is shown in Figure 2. For a complete schematic, bill of materials (BOM), and layout details, refer to the design support files http://www.analog.com/CN0282-DesignSupport.

When used in an actual system, a 4-layer PCB offers some advantages. The HDMI compliance testing requires that all transition-minimized differential signaling (TMDS) lines coming into the HDMI receiver have 100 Ω ± 10% characteristic impedance. Maintaining trace characteristic impedance is generally an easier process with a 4-layer PCB than a 2-layer PCB. Additionally, 4-layer PCBs provide more options for avoiding electromagnetic interference (EMI)/radio frequency interference (RFI) effects and achieving electromagnetic compliance (EMC).

High speed digital signals that have fast rising and falling edges create a risk for EMI/RFI effects. High speed signals exist on the board mainly on the pixel bus link that connects the ADV7611 output with the ADV7125 DAC input. In some cases, series resistors can be added to these lines to minimize EMI/RFI effects by slowing down the fast edges. In the 2-layer layout, the connection between the ADV7611 and the ADV7125 is relatively short; therefore, no series resistors are required.

To minimize the impact of the EMI/RFI emission, the option of setting the drive strength of the pixel bus drivers and the audio output is given. Drive strength reduction is accomplished within the ADV7611. For additional details, refer to Drive Strength Selection section of the UG-180 User Guide.
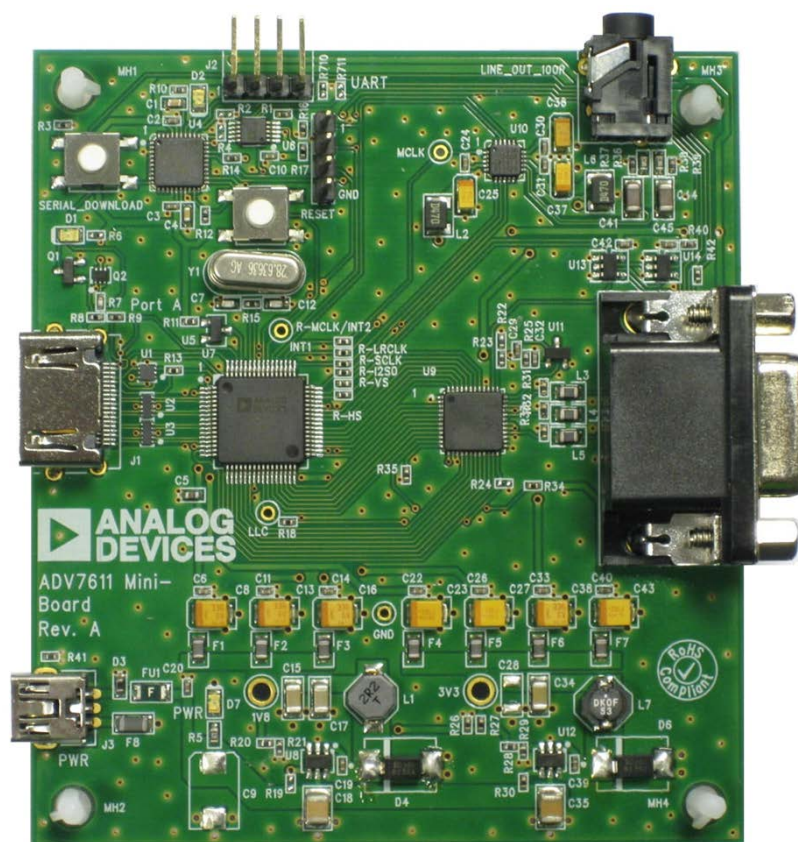

Figure 2. HDMI-to-VGA (HDMI2VGA) Converter with Audio Extraction, 2-Layer PCB

Evaluation and Test

The circuit has been tested using the following HDMI sources:

- DVD-S97 DVD/CD player (640 × 480p)
- Dell E6520 laptop (1280 × 1024 or 1600 ×1200 VGA monitor resolution)
- Blu-ray Panasonic DMP-BDT100 (640 × 480p)
- Quantum Data 882 video generator (UXGA 1600 × 1200 at 60 Hz, 8 bpp)

The circuit has been tested using the following VGA monitors:

- Dell 1908FP (1280 ×1024 at 60 Hz maximum)
- Dell 2007FP (1600 ×1200 at 60 Hz maximum)
- Sun Microsystems GDM-5010PT monitor

During evaluation of the board, a UART connector (EVAL-ADuC-CABLE1Z) was used for both programming the evaluation board and displaying the debug information and EDID content of the VGA monitors. The EVAL-ADuC-CABLE1Z is an RS-232 level shifter that allows interfacing between LVTTL and RS-232 logic levels.

Testing requires connecting cables as shown in Figure 3 (VGA, HDMI, audio output, and USB) and pressing the reset button.

Consumer video players (DVD or Blu-ray) usually do not support VESA video resolutions such as XGA, SXGA, or UXGA. During the tests, those sources output standard VGA.

The Dell E6520 laptop can be used as a video source that natively supports VESA standards and properly reads back content provided by the HDMI2VGA converter. It outputs either 1280 × 1024 at 60 Hz for the Dell 1908FP monitor or 1600 × 1200 at 60 Hz for the Dell 2007FP monitor.

Both video players provide LPCM audio content as per EDID and were decoded and output from the audio codec without any problems.
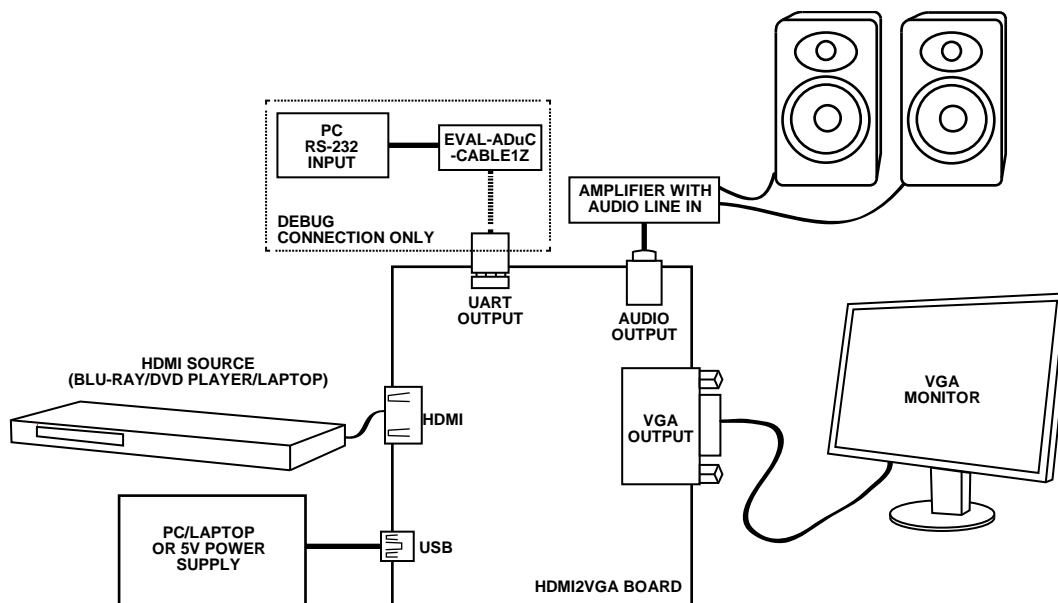

Figure 3. Test Setup Block Diagram

LEARN MORE

CN-0282 Design Support Package:
http://www.analog.com/CN0282-DesignSupport

ADV7611 Design Support File on Engineer Zone:
http://ez.analog.com/docs/DOC-1745

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout.* Analog Dialogue 39-09, September 2005.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND".* Analog Devices, Inc., 2009.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices, Inc., 2009.

Howard Johnson, Martin Graham, *High-Speed Digital Design*, Prentice Hall, ISBN-10: 0133957241, ISBN-13: 978-0133957242.

Howard Johnson, Martin Graham, High Speed Signal Propagation, Prentice Hall, ISBN-10: 013084408X, ISBN-13: 978-0130844088.

VESA EDID Specification

CEA861 Specification

HDMI 1.4b Specification

Data Sheets and Evaluation Boards

ADV7611 Datasheet

ADV7125 Datasheet

ADuC7020 Datasheet

ADP2301 Datasheet

SSM2604 Datasheet

UG-180, User Guide for ADV7611

REVISION HISTORY

7/12—Revision 0: Initial Release

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ANALOG DEVICES