

## Designing an Inverting Power Supply Using the [ADP2441/ADP2442](#) Synchronous Step-Down DC-to-DC Regulators

by Kevin Tompsett and Ricky Yang

### INTRODUCTION

Applications such as bipolar amplifiers, optical modules, CCD bias, and OLED displays usually require a negative output voltage from a positive input voltage. Designers of power management systems need versatile switching controllers and regulators that allow them to solve these power management challenges. The [ADP2441/ADP2442](#) switching regulators from Analog Devices, Inc., provide synchronous buck functionality. This ranges from a 36 V input voltage down to 0.6 V output voltage at up to 1 A with a switching frequency range from 300 kHz to 1 MHz.

Although targeted for synchronous step-down applications, the versatility of the [ADP2441/ADP2442](#) allows these parts to realize an inverting buck boost topology, which can generate a negative output voltage from a positive input voltage, without additional cost, component count, or solution size.

These parts utilize synchronous topology, which gives higher efficiency at a full load and lower noise at a light load operation than an asynchronous part. If higher efficiency at a low load is desired, the [ADP2441](#) has a pulse skip mode (PSM). The [ADP2442](#) can operate in forced constant current mode (CCM) for lower noise at low load or with PSM enabled.

This application note describes how to implement the [ADP2441/ADP2442](#) in a synchronous inverting buck boost topology to generate negative output voltages from positive input power supplies. In addition, some design challenges and possible solutions are addressed. For a faster design time, the [ADIsimPower](#) design tool can be used. This tool uses far more sophisticated design equations and methods to create a robust design that meets the requirements under all conditions almost instantaneously. It is available for download via the [ADIsimPower](#) product page or directly via [ADP244x Inverting Buck Boost Designer](#).

## TABLE OF CONTENTS

Introduction .....	1	Input Capacitor Selection.....	5
Revision History .....	2	Compensation Selection.....	6
Buck Boost Topology Basics .....	3	Enable Signal Level Shifting.....	6
Implementation with the ADP2441/ADP2442.....	3	Reduce $V_{OUT}$ Over Shoot Before Start Up .....	7
Output Voltage Setting.....	4	Conclusion.....	8
Inductor Selection .....	4	References.....	8
Ramp Compensation .....	4	Related Links.....	8
Output Capacitor Selection.....	5		

## REVISION HISTORY

7/14—Revision 0: Initial Version

**BUCK BOOST TOPOLOGY BASICS**

The simplified buck boost topology is shown in Figure 1. The topology consists of an inductor, two power switches operating out of phase from one another, and input/output capacitors.

Figure 2 and Figure 3 show the current flow path during the on time and off time, respectively. During the on time, Switch S1 is on, S2 is off, and the current is flowing from the input capacitor, charging the inductor while the output capacitor provides energy to the load. During off time, Switch S1 is off, Switch S2 is on, and the current flows from the inductor to the load while charging the output capacitor.

Note that the current flows from ground to  $V_{OUT}$ , which results in negative output voltage.

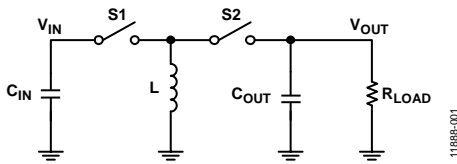


Figure 1. Buck Boost Topology

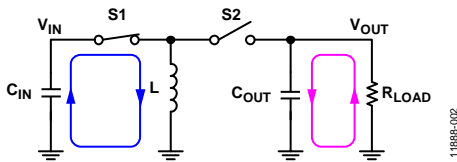


Figure 2. Current Flow Path During On Time

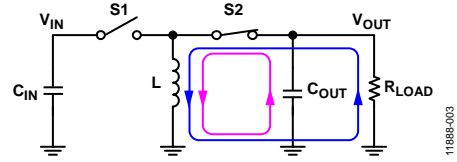


Figure 3. Current Flow Path During Off Time

The steady state conversion ratio can be written per Equation 1 by applying the principles of inductor voltage-second balance and capacitor charge balance on the topology. The dc inductor current value,  $I_L$ , in CCM is specified in Equation 2, and the inductor ripple current,  $\Delta I_L$ , is shown in Equation 3.

$$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D} \tag{1}$$

$$I_L = \frac{I_{OUT}}{1-D} \tag{2}$$

$$\Delta I_L = \frac{-V_{OUT} \times (1-D)}{L \times f_{SW}} \tag{3}$$

**IMPLEMENTATION WITH THE ADP2441/ADP2442**

To implement the buck boost topology inverting power supply application by using the ADP2441/ADP2442 synchronous buck regulator, take into consideration some design restrictions as listed in Table 1.

Table 1. Design Restrictions

Voltage and Current	Device Parameters	ADP2441/ADP2442
$V_{IN\_MIN}$	$V_{UVLO}$	4.5 V
$V_{IN\_MAX} +  V_{OUT} $	$V_{MAX}$	20 V
$I_{L\_PEAK}$ ( $I_{L\_peak} \neq I_{OUT}$ )	$I_{OCP}$	1.2 A/1.2 A

The minimum input voltage of the buck boost circuit must be higher than the UVLO voltage of the ADP2441/ADP2442, which has the typical value of 4.5 V to get the regulator to work. The sum of the maximum input voltage and the absolute value of the output voltage must be lower than the maximum operation input voltage of the regulators,  $V_{MAX}$ , which has the typical value of 20 V. In addition, make sure the inductor peak current is smaller than the OCP trigger point of the regulator with accommodation for inductance tolerance.

To convert the synchronous buck regulator into the buck boost topology, the inductor and output capacitor are connected similar to the buck topology. Note that the ground and the output voltage points are reversed as shown in Figure 4.

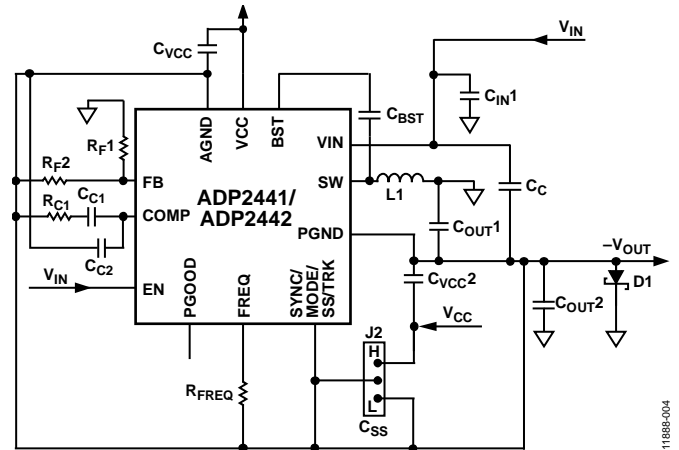


Figure 4. Inverting Buck Boost Topology Implemented with the ADP2441/ADP2442

## OUTPUT VOLTAGE SETTING

The output voltage is set by an external resistive divider. The resistor values are calculated using

$$R_{TOP} = R_{BOTTOM} \times \frac{|V_{OUT}| - 0.6}{0.6} \quad (4)$$

To limit the output voltage accuracy degradation due to the FB bias current (0.1  $\mu$ A maximum) to less than 0.5% (maximum), ensure that  $R_{BOTTOM} < 30 \text{ k}\Omega$ .

Table 2 lists the recommended resistor divider for various output voltages.

**Table 2. Resistor Divider for Difference Output Voltage**

V <sub>OUT</sub> (V)	R <sub>TOP</sub> $\pm$ 1% (k $\Omega$ )	R <sub>BOTTOM</sub> $\pm$ 1% (k $\Omega$ )
-1.2	10	10
-1.8	20	10
-2.5	47.5	15
-3.3	10	2.21
-5	22	3
-12	28	1.47
-15	35.7	1.5

## INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, and inductor ripple current. Using a smaller inductance leads to a faster transient response, but degrades efficiency due to a larger inductor ripple current. Using a larger inductance value leads to a smaller ripple current and better efficiency, but results in a slower transient response.

As a guideline, the inductor ripple current ( $\Delta I_L$ ) is typically set to 30% of the maximum inductor average current,  $I_{AVG}$ . The inductor value is calculated using the following equation:

$$L = \frac{V_{IN} \times D}{K_{RP} \times I_{AVG} \times f_{SW}} \quad (5)$$

where:

$V_{IN}$  is the input voltage.

$D$  is the duty cycle:

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + V_{IN}} \quad (6)$$

$K_{RP}$  is the chosen current ripple percentage. A good rule of thumb is around 30%.

$I_{AVG}$  is the average inductor current:

$$I_{AVG} = \frac{I_{OUT}}{1 - D} \quad (7)$$

$f_{SW}$  is the switching frequency.

## RAMP COMPENSATION

As with all current mode converters, the ADP2441/ADP2442 in an inverting buck boost topology require ramp compensation to assure current mode stability. The ADP2441/ADP2442 use an innovative adaptive ramp scheme that is dependent on duty cycle. This results in an ideal ramp compensation amplitude

over a wider range of duty cycle than could be achieved with the old style fixed ramp compensation that many chips use. To choose an inductor that will be current-mode stable first, choose an inductor using Equation 5. Then check that  $Q_n$  calculated using Equation 8 is between 0.2 and 0.9 at both minimum and maximum  $V_{IN}$ . Equation 8 is based on Ridley's work in his *An Accurate and Practical Small-Signal Model for Current-Mode Control* paper (see the References section).

$$Q_n = 1/(\pi \times (0.5 - D + 0.33 \times f_{SW} \times L/(D \times V_{IN})) \quad (8)$$

where:

$f_{SW}$  is the switching frequency.

The peak inductor current is calculated by adding the dc component and half of the peak-to-peak inductor ripple current.

$$I_{PEAK} = I_{AVG} + \frac{I_{AVG} \times K_{RP}}{2} \quad (9)$$

The peak inductor current is also the peak current in the internal power switch, which is the sense element used to determine whether to induce current limit. To avoid premature current limit, the peak inductor current should not exceed the OCP threshold current,  $I_{OCP}$ , of the devices.

Taking into account this maximum peak inductor current, the application space of the ADP2441/ADP2442 in the inverting buck boost topology for common input voltages at 600 kHz switching frequency is shown in Figure 5 with the assumption that the peak-to-peak inductor ripple current is 40% of the inductor average current.

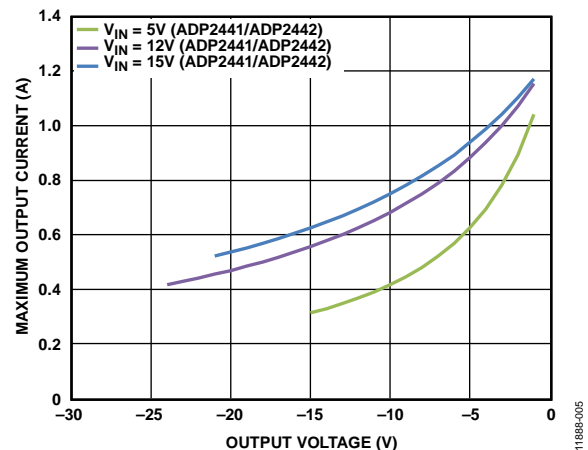


Figure 5. Application Space for Common Input Voltage at  $f_{SW} = 600 \text{ kHz}$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a steep saturation characteristic, the saturation current rating of the inductor should be higher than the current limit threshold for the IC. This prevents the inductor from saturating during normal operation.

### OUTPUT CAPACITOR SELECTION

The output voltage of the inverting buck boost tends to be noisier than a buck converter. This is because unlike a buck converter, the output current is discontinuous in the inverting buck boost topology. The fast rise and fall times of Switch S2 result in noise spikes on the output voltage as the current in S2 is ramped up quickly from 0 to  $I_L$  and back to 0. This makes it very important to use low ESR, MLCC capacitors and good layout techniques to reduce parasitic inductance.

Equation 10 gives an estimated value of the minimum capacitance required to keep the output voltage ripple within an allowable range.

$$C_{OUT} \approx \frac{I_{OUT} \times D}{f_{SW} \times (\Delta V_{RIPPLE} - I_{PEAK} \times ESR)} \quad (10)$$

where:

$\Delta V_{RIPPLE}$  is the allowable output ripple voltage.

$ESR$  is the total equivalent series resistance of the output capacitors.

$I_{PEAK}$  is the inductor peak current.

To achieve as low output ripple voltage as possible, MLCC capacitors that have very low ESR values are recommended. The rms current rating of the selected output capacitors should be larger than the values calculated using Equation 11.

$$I_{RMS\_C_{OUT}} = \sqrt{\left(\frac{I_{OUT} \times D}{1-D}\right)^2 \times (1-D) + \frac{\Delta I_L^2}{12} \times (1-D) + I_{OUT}^2 \times D} \quad (11)$$

### INPUT CAPACITOR SELECTION

The input current is also discontinuous in the inverting buck boost topology. Therefore, the fast rise and fall times of Switch S1 result in noise spikes on the input rail as the current in S1 is ramped up quickly from 0 to  $I_L$  and back to 0. This makes it very important to use low ESR, MLCC capacitors, and good layout techniques to reduce parasitic inductance.

Equation 12 calculates the minimum input capacitance assuming energy depletion of the input capacitor during on time is no more than 5% of the input voltage.

$$C_{IN} = \frac{I_{AVG} \times D}{f_{SW} \times (0.05 \times V_{IN} - I_{PEAK} \times ESR_{C_{IN}})} \quad (12)$$

where:

$I_{AVG}$  is the average inductor current.

$ESR_{C_{IN}}$  is the equivalent series resistance of the input capacitors.

At least one 10  $\mu F$  ceramic capacitor is recommended; place it as close to PVIN pin as possible. The rms current of the selected input capacitor should be greater than the value calculated in Equation 13.

$$I_{RMS\_C_{IN}} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right) \times D + \frac{D^2 \times I_{OUT}^2}{1-D}} \quad (13)$$

Although the majority of the capacitance on the input voltage rail is referenced to system ground, an additional input decoupling capacitor placed from the input voltage to the GND pin of ADP2441/ADP2442 can reduce the output voltage ripple and improve the transient response as shown in Figure 6.

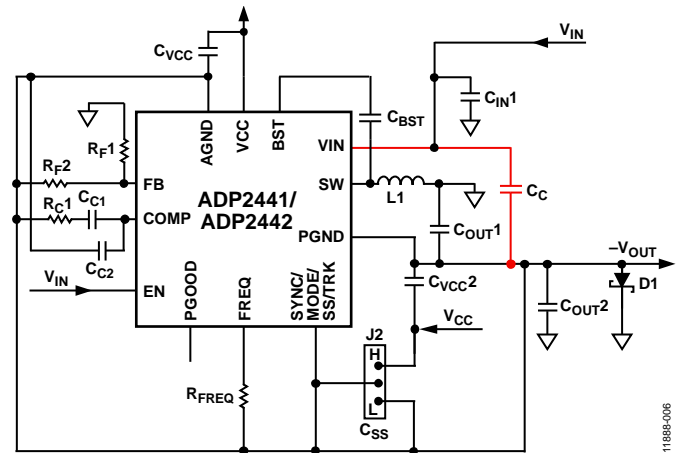


Figure 6. Inverting Buck Boost Topology with Input Decoupling Capacitor from  $V_{IN}$  to GND Pin

## COMPENSATION SELECTION

The control-to-output transfer function of the power stage in buck boost topology can be written in the form:

$$G_{VD}(s) = K \times \frac{\left(1 - \frac{s}{2 \times \pi \times f_{Z1}}\right) \times \left(1 + \frac{s}{2 \pi \times f_{Z2}}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)} \quad (14)$$

where:

$$K = \frac{R \times (1 - D)}{R_i \times (1 + D)}$$

$R$  is the load resistor.

$R_i$  is the current sense gain with a typical value of 0.49 V/A.

The transfer function  $G_{VD}(s)$  has one right-half-plane-zero (RHPZ),  $f_{Z1}$ ; one zero,  $f_{Z2}$ ; and one pole,  $f_p$ . The values of the zero and pole are:

$$f_{Z1} = \frac{(1 - D)^2 \times R}{2 \times \pi \times L \times D} \quad (15)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \quad (16)$$

$$f_p = \frac{1 + D}{2 \times \pi \times R \times C_{OUT}} \quad (17)$$

where:

$R_{ESR}$  is the equivalent series resistance of the output capacitor.

Use the following design guidelines to calculate the values of the compensation network components.

- Set the cross frequency,  $f_c$ , between  $f_p$  and  $1/3$  of  $f_{Z1}$

$$f_c = \sqrt{f_p \times f_{Z1}} \quad (18)$$

- Calculate the  $R_c$  value using the equation:

$$R_c = \frac{f_c \times |V_{OUT}|}{K \times f_p \times g_m \times 0.6} \quad (19)$$

where:

$g_m$  is the transconductance of the internal error amplifier with a typical value of 250  $\mu$ S.

- Place the compensation zero at  $1/2$  of the power stage pole,  $f_p$

$$C_{C1} = \frac{2 \times R \times C_{COUT}}{(1 + D) \times R_c} \quad (20)$$

- Place the compensation pole at the RHPZ  $f_{Z1}$

$$C_{C2} = \frac{D \times L}{(1 - D)^2 \times R \times R_c} \quad (21)$$

## ENABLE SIGNAL LEVEL SHIFTING

The ADP2441/ADP2442 have an EN pin to enable and disable the regulator. However, in the inverting buck boost application, the IC is referenced to the negative output voltage instead of the system ground. Once the chip is enabled, pulling the enable pin to ground will not turn the IC off because the voltage from the enable pin to AGND of the IC will be equal to  $V_{OUT}$ .

One of the possible solutions for this issue is to use NPN and PNP transistors and several resistors to level shift the enable level as shown in Figure 7.

Note that the precision enable feature of the ADP2441/ADP2442 is lost when the level shifting circuit is used. If the enable function is not needed, simply connect the EN pin to the input voltage as shown in Figure 4.

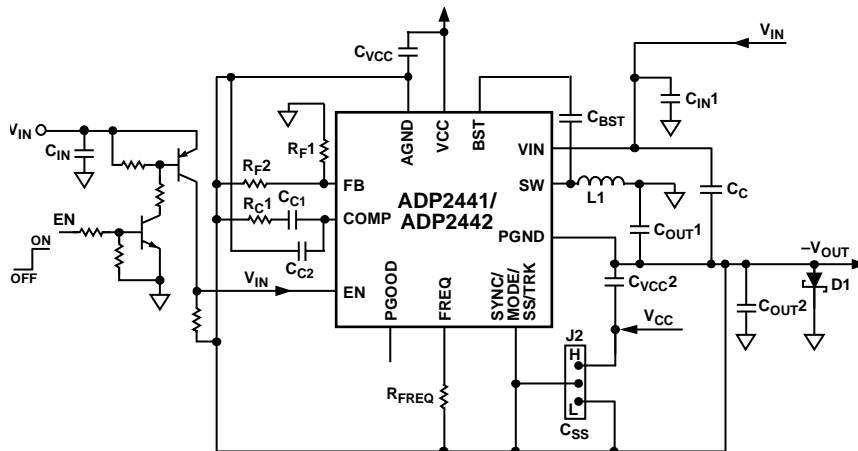


Figure 7. EN Level Shifting Circuit for Inverting Buck Boost Topology

**V<sub>OUT</sub> OVER SHOOT BEFORE STARTUP**

When using the synchronous buck regulator as an inverting buck boost topology, one common issue is that the output voltage starts off positive before the regulator is enabled as shown in Figure 8.

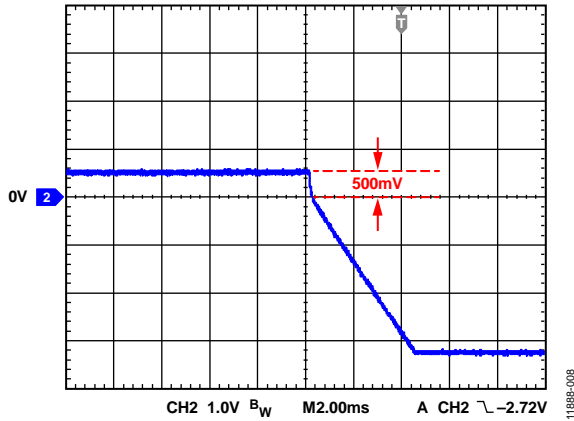


Figure 8. V<sub>OUT</sub> Ramps Up Before Startup

This positive output voltage is caused by the shutdown current of the regulator and any other chips connected to the negative rail, flowing from the PGND pin of the IC through the body diode of the low-side MOSFET and back to the system ground as shown in Figure 9. The body diode of the low-side MOSFET is that which clamps the V<sub>OUT</sub> at the forward voltage of the body diode with a typical value of around 500 mV.

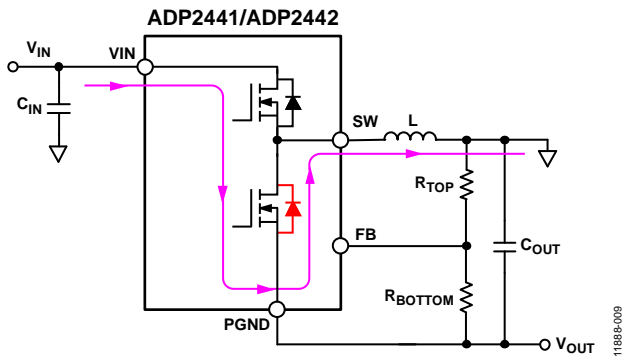


Figure 9. Current Flows Through Body Diode of Low Side MOSFET

Because V<sub>OUT</sub> is connected to the PGND pin of the regulator which is actually the reference point for the internal circuits like UVLO, the positive voltage shown in the PGND pin decreases the UVLO threshold voltage. The regulator may fail to start up when the input voltage is very close to the UVLO threshold voltage of the regulator, which has a typical value of 4.0 V.

This issue can be seen in all buck regulators when they are used to perform the inverting buck boost topology described herein and it is very hard to eliminate the issue completely. One solution is to put a Schottky diode on the output of the converter. This diode reduces the positive voltage somewhat and prevents any silicon diodes in the ADP2441/ADP2442 regulator or any load components from turning on and causing problems. Another solution is to reduce the resistance of the feedback resistor divider until the voltage drop across the resistor divider is lower than the forward voltage of the body diode of the low-side MOSFET. Then, the shutdown current flows through the resistor divider instead of the body diode as shown in Figure 10 and the positive voltage on the PGND pin can be reduced to an acceptable value.

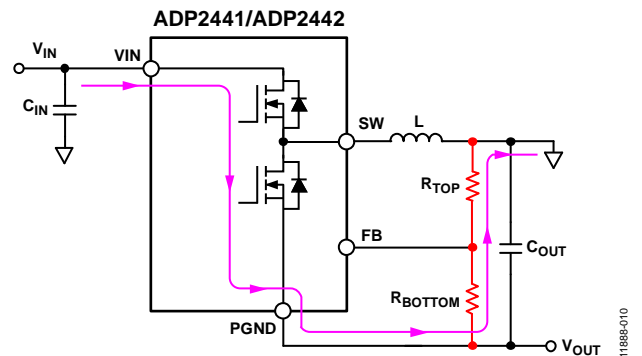


Figure 10. Current Flows Through the Feedback Resistor Divider

Figure 11 shows the result of reducing the resistance of the resistor divider. The positive V<sub>OUT</sub> voltage decreases from 500 mV to 180 mV.

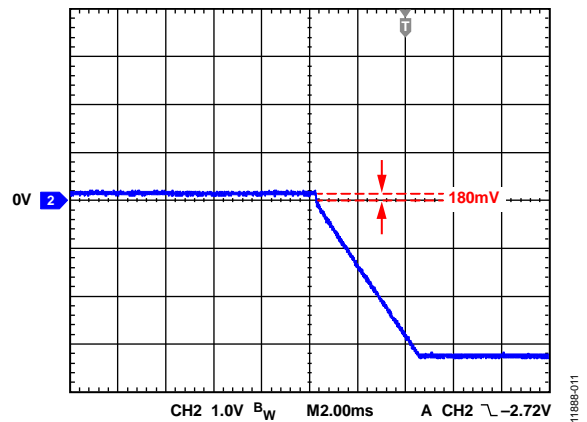


Figure 11. Reduce V<sub>OUT</sub> Ramp Up by Decreasing the Resistance of the Feedback Resistor Divider

The drawback of this solution is that the quiescent current of the system increases because the current flowing through the feedback resistor is higher. This increased quiescent current can reduce the efficiency at light loads quite a bit, though the actual power loss is quite small.

**CONCLUSION**

The [ADP2441/ADP2442](#) can be used successfully in the inverting buck boost topology resulting in a simple, inexpensive, and small solution for creating a negative rail. In addition to detailing all of the necessary design equations, this application note provides a simple EN level shifting circuit when the enable/disable functionality is needed. Also, the potential start-up issue inherent with the inverting buck boost topology is avoided with two simple solutions.

By following the design equations and suggestions in this application note, the system designer can ensure a robust design that satisfies all their requirements.

**RELATED LINKS**

Resources	Description
<a href="#">ADP2441</a>	Data Sheet, 36 V, 1 A, Synchronous Step-Down DC-to-DC Regulator
<a href="#">ADP2442</a>	Data Sheet, 36 V, 1 A, Synchronous Step-Down DC-to-DC Regulator with External Clock Synchronization
<a href="#">AN-1083</a>	Application Note, Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 Switching Regulators
<a href="#">AN-1168</a>	Application Note, Designing an Inverting Power Supply Using the ADP2384/ADP2386 Synchronous Step-Down DC-to-DC Regulators
<a href="#">ADP244x Inverting Buck Boost Designer</a>	ADIsimPower Design Tool

**REFERENCES**

R. B. Ridley. *An Accurate and Practical Small-Signal Model for Current-Mode Control*. Ridley Engineering Inc. 1999.