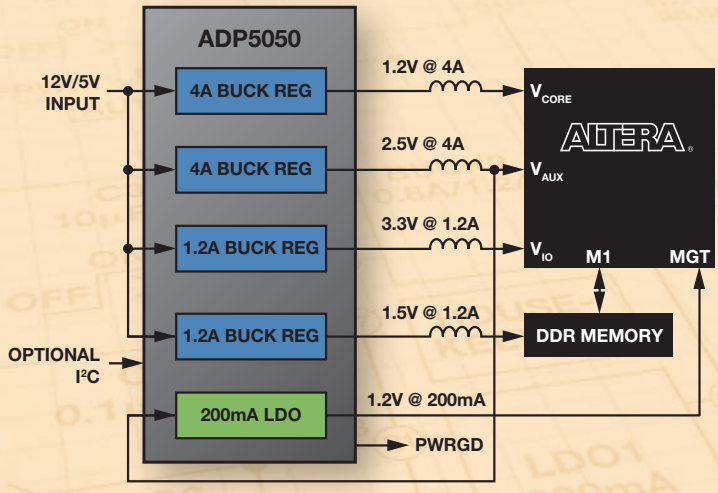
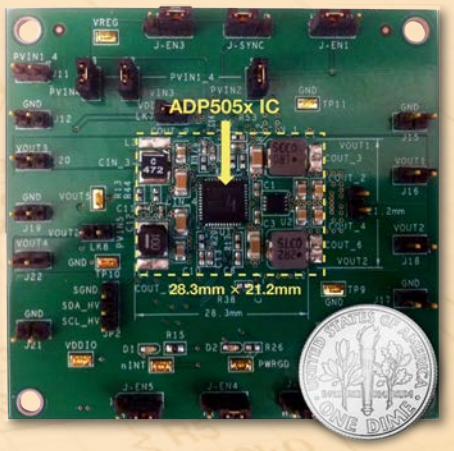
Integrated Power Solutions for Altera FPGAs

Modern high performance FPGA-based systems require an increasing number of dedicated rails supplying core, I/O, memory, PLL, and precision analog voltages. Typical FPGA-based systems today make use of standalone switching regulators and LDOs; but, as board area continues to shrink as end product form factors shrink, this complicates the task of designing more efficient power management solutions for powering FPGAs. Combining multiple switching regulators and LDOs into a single package enables very small, flexible, highly efficient power management solutions for powering FPGAs and precision analog components with the highest system reliability.

Ultrasmall 12 V/5 V Quad Buck + LDO in LFCSP



ADP505x Solution Size Only 28.3 mm × 21.2 mm



- *Fixed and Adjustable Output Voltages*
- *Wide Range of Switching Frequency Operation (250 kHz to 1.4 MHz)*
- *Resistor Programmable Current Limit on Buck 1 and Buck 2 (4 A, 2.5 A, 1.2 A)*
- *Simple Power Supply Sequencing*
- *Frequency Synchronization Input or Output*
- *LDO or POR/WDI Options*

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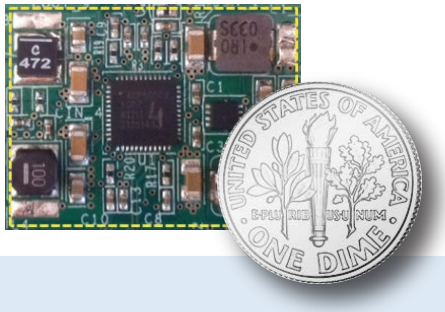
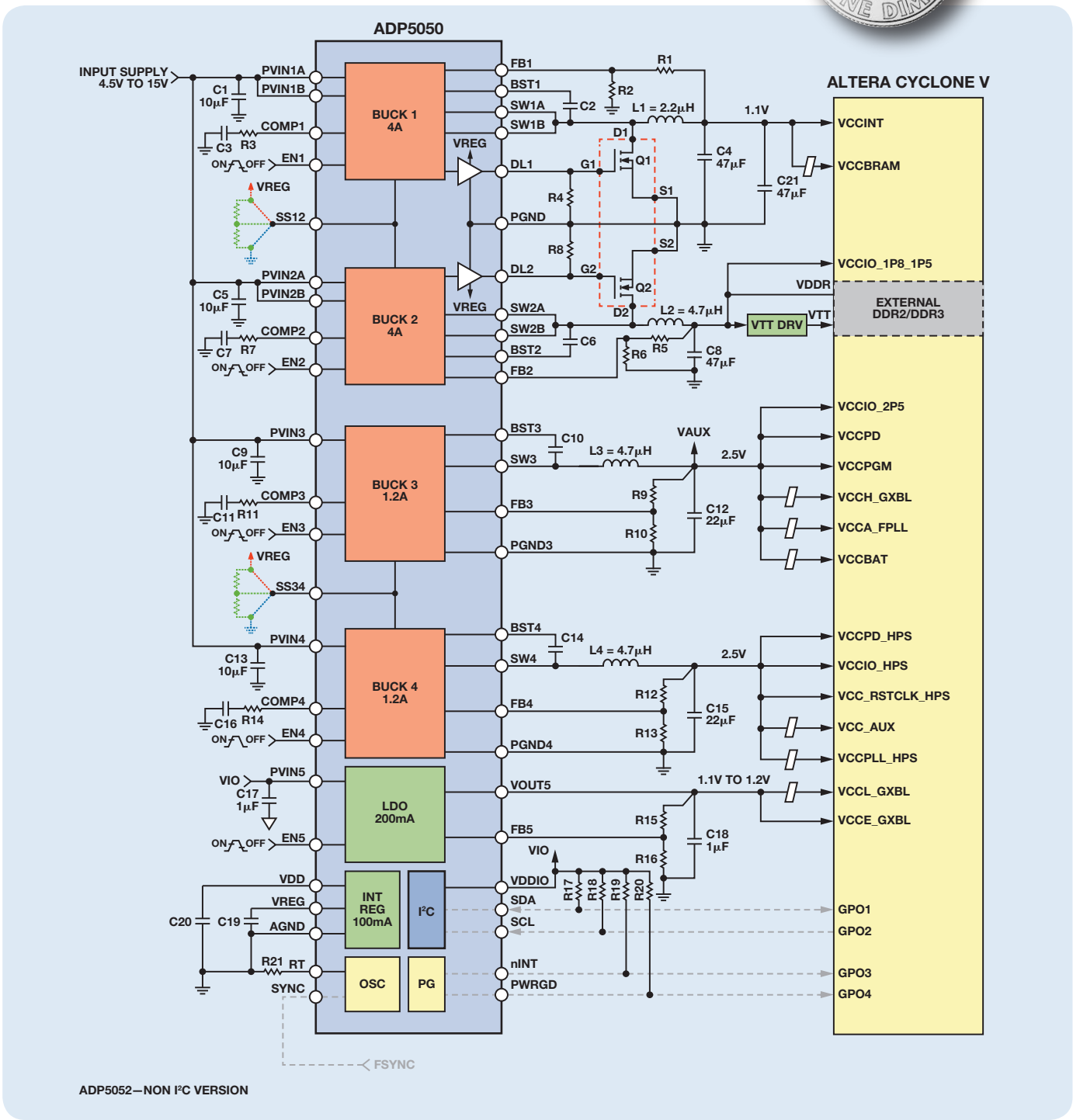
ANALOG DEVICES

ADP5050 Supply for Altera Cyclone V (GX/SX)

- Max board size: 588 mm²
  - Assumes 4 A, 4 A, 1 A, 1 A
- Min board size: 310 mm²
  - Assumes 3 A, 2 A, 1 A, 1 A
- Estimated BOM: $4.95 (1 kpcs)





ADP5052—NON I²C VERSION

PowerPlay Power Estimation—Use Case for Altera Cyclone V

Altera FPGA Selection		Power Estimation[1]															
Family	Logic Elements	Clock Low Speed	Low Speed Logic Used	Toggle Rate	Clock High Speed	High Speed Logic Used	Toggle Rate	DSP/ Instances	RAM Blocks	RAM Clock	Outputs	I/O Toggle Rate	Out Load	XCVR Freq	XCVR Channels	HSDI Freq	HSDI Channels
Cyclone IV/E	<115 k	100 MHz	33%	12.50%	400 MHz	17.00%	18.00%	36 × 36 mult/100	100	50 MHz	100	40 MHz	30 pF	N/A	N/A	N/A	N/A
		200 MHz	50%	12.50%	600 MHz	20.00%	12.50%	36 × 36 mult/200	300	50 MHz	200	40 MHz	30 pF	N/A	N/A	N/A	N/A
Cyclone IV/GX	<150 k	100 MHz	33%	12.50%	500 MHz	17.00%	12.50%	36 × 36 mult/100	350	200 MHz	200	50 MHz	30 pF	3.125 GHz	2 Tx/2 Rx	N/A	N/A
		200 MHz	50%	12.50%	600 MHz	20.00%	12.50%	36 × 36 mult/300	500	200 MHz	300	50 MHz	30 pF	3.125 GHz	2 Tx/2 Rx	N/A	N/A
Cyclone V/E	~300 k	100 MHz	44%	12.50%	600 MHz	12.00%	12.50%	27 × 27 mult/300	500	200 MHz	100	50 MHz	30 pF	N/A	N/A	1.25 GHz	8 Tx + 8 Rx
Cyclone V/GX	~300 k	100 MHz	50%	12.50%	600 MHz	20.00%	12.50%	27 × 27 mult/300	500	200 MHz	150	50 MHz	30 pF	3.125 GHz	6 Tx/6 Rx	1.25 GHz	8 Tx + 8 Rx
Cyclone V/SX	~110 k	100 MHz	50%	12.50%	600 MHz	20.00%	12.50%	27 × 27 mult/50	300	200 MHz	150	50 MHz	30 pF	3.125 GHz	6 Tx/6 Rx	1.25 GHz	8 Tx + 8 Rx

FPGA Power Consumption Derived from Spreadsheet[2]				
ICCINT + ICC	ICCIO	ICCA	ICCPD	ICCXCVR
1.36 A (@ 1.2 V)	0.033 A (@ 2.5 V)	0.039 A (@ 2.5 V)	0.018 A (@ 1.1 V)	N/A
2.154 A (@ 1.2 V)	0.055 A (@ 2.5 V)	0.039 A (@ 2.5 V)	0.048 A (@ 1.1 V)	N/A
2.27 A (@ 1.2 V)	0.04 A (@ 2.5 V)	0.042 A (@ 2.5 V)	0.031 A (@ 1.2 V)	0.231 A (@ 1.2 V)
3.92 A (@ 1.2 V)	0.04 A (@ 2.5 V)	0.039 A (@ 2.5 V)	0.032 A (@ 1.2 V)	0.231 A (@ 1.2 V)
2.87 A (@ 1.1 V)	0.032 A (@ 2.5 V)	0.04 A (@ 2.5 V)	0.014 A (@ 2.5 V)	N/A
3.67 A (@ 1.1 V)	0.045 A (@ 2.5 A)	0.058 A (@ 2.5 V)	0.015 A (@ 2.5 V)	0.225 A (@ 1.1 V)
1.49 A (@ 1.1 V)	0.042 A (@ 2.5 V)	0.128 A (@ 2.5 V)	0.007 A (@ 2.5 V)	0.225 A (@ 1.1 V)

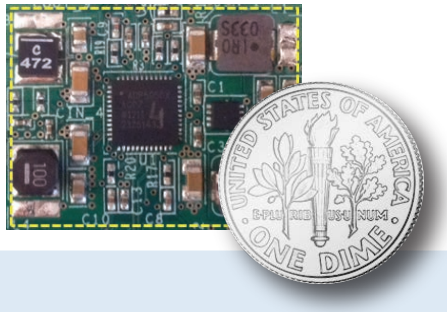
[1] Power requirement derived from Altera PowerPlay 12.1—the spreadsheet assumes at least 50% of resources occupation with 12.5% toggle rate. The core current is kept below the maximum driving capability of the suggested µPMU.
[2] The proposed µPMU supplies three to four FPGA rails: VCC, VCCA, VCCIO, and VCCPD from buck regulators while the transceiver (where applicable) is supplied from the LDO. One buck is dedicated to external DDR memories and the bus level. Only one I/O supply voltage is considered, and multiple I/O banks with different voltage levels can be supported.

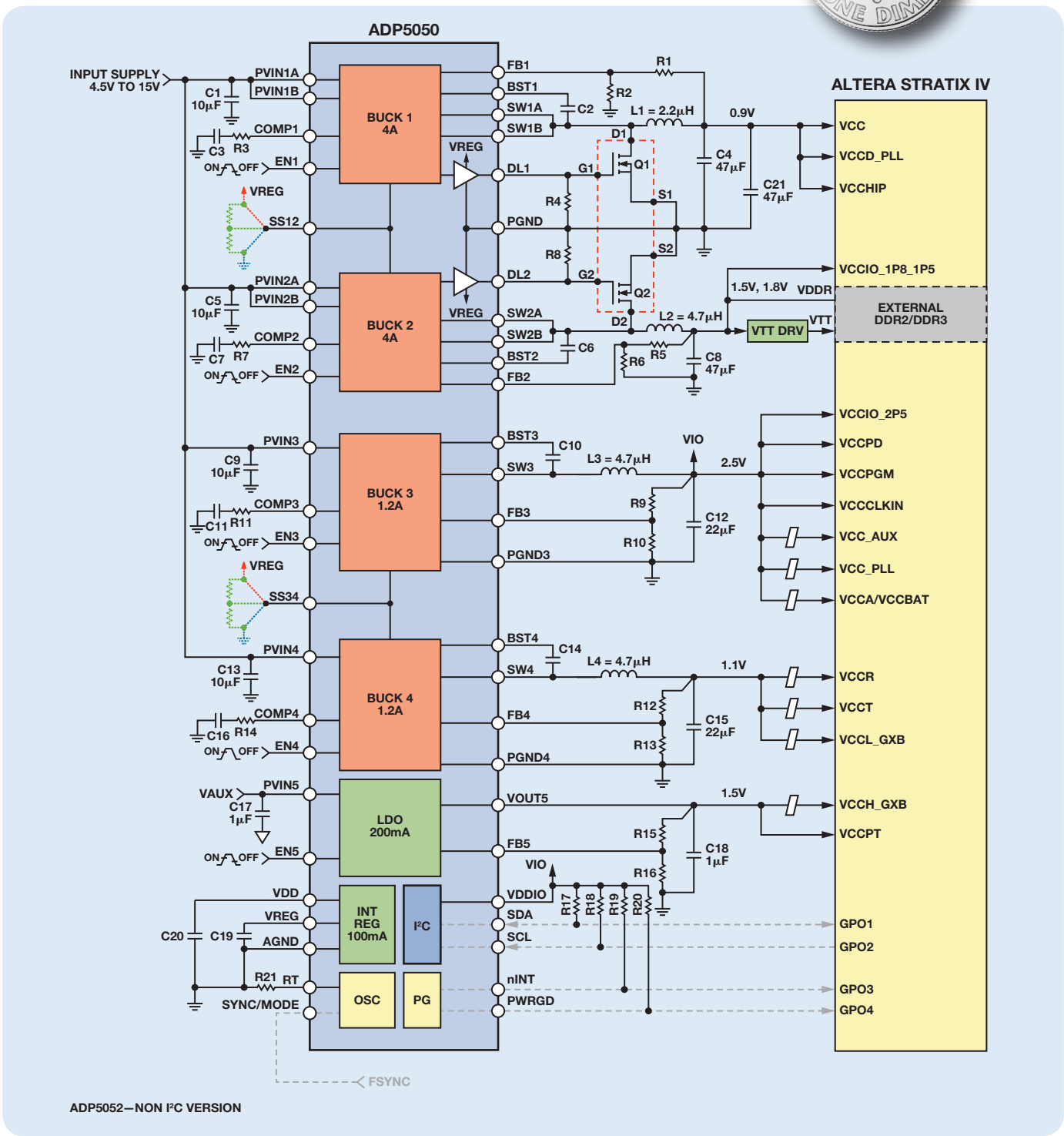
Bill of Materials for the ADP5050 Powering Altera Cyclone V

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	5-channel micro PMU	ADP5050ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
C17, C18, C19, C20	4	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C8, C21	3	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C12, C15	2	22 µF, X5R, 6.3 V	GRM188R60J226MEA0	Murata	0603	
C3, C7, C11, C16	4	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 23 A, 25 mΩ	Si7228DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 10 A, 20 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1	1	2.2 µH, 15.9 A, 12.7 mΩ	XAL6030-222ME	Coilcraft	6.0 × 6.0 × 3.0	
		2.3 µH, 6.4 A, 22 mΩ	NRS6045-2R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L2, L3, L4	3	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R21	1	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8	2	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R5, R6, R9, R10, R12, R13, R15, R16,	14	Resistor, 1%		Various	0402	Value depends on output voltage setting
R3, R7, R11, R14	4	10 kΩ, resistor, 5%		Various	0402	
R17, R18, R19, R20	4	10 kΩ, resistor, 5%		Various	0402	Optional for I²C interface

ADP5050 Supply for Altera Stratix IV

- Max board size: 588 mm²
  - Assumes 4 A, 4 A, 1 A, 1 A
- Min board size: 310 mm²
  - Assumes 3 A, 2 A, 1 A, 1 A
- Estimated BOM: $4.95 (1 kpcs)





ADP5052—NON I²C VERSION

PowerPlay Power Estimation—Use Cases for Altera Stratix IV, V, and Arria V

Altera FPGA Selection		Power Estimation[1]															
Family	Logic Elements	Clock Low Speed	Low Speed Logic Used	Toggle Rate	Clock High Speed	High Speed Logic Used	Toggle Rate	DSP/ Instances	RAM Blocks	RAM Clock	Outputs	I/O Toggle Rate	Out Load	XCVR Freq	XCVR Channels	HSDI Freq	HSDI Channels
Stratix III	<160 k	100 MHz	42%	12.50%	600 MHz	8.00%	18.00%	36 × 36 mult/20	120	50 MHz	200	40 MHz	30 pF	N/A	N/A	1.25 GHz	8Tx + 8Rx
	~200 k	100 MHz	35%	12.50%	400 MHz	8.00%	12.50%	36 × 36 mult/20	120	50 MHz	200	40 MHz	30 pF	N/A	N/A	1.25 GHz	8Tx + 8Rx
	~340 k	100 MHz	40%	12.50%	0.00%	0.00%	0.00%	36 × 36 mult/20	120	50 MHz	300	50 MHz	30 pF	N/A	N/A	1.25 GHz	8Tx + 8Rx
Stratix IV/E	~230 k	100 MHz	30%	12.50%	N/A	N/A	12.50%	36 × 36 mult/100	100	50 MHz	150	50 MHz	30 pF	N/A	N/A	1.25 GHz	8Tx + 8Rx
Stratix IV/GX	<150 k	200 MHz	42%	12.50%	600 MHz	8.00%	12.50%	36 × 36 mult/100	210	50 MHz	300	50 MHz	30 pF	4.25 GHz	2Tx/2Rx	1.25 GHz	8Tx + 8Rx
	~350 k	150 MHz	50%	12.50%	0.00%	0.00%	0.00%	36 × 36 mult/100	210	50 MHz	300	50 MHz	30 pF	4.25 GHz	2Tx/2Rx	1.25 GHz	8Tx + 8Rx
Stratix V/GX	~340 k	100 MHz	45%	12.50%	800 MHz	5.00%	12.50%	36 × 36 mult/100	400	100 MHz	500	50 MHz	30 pF	4.25 GHz	2Tx/2Rx	1.25 GHz	8Tx + 8Rx
Arria V	~840 k	100 MHz	45%	12.50%	800 MHz	5.00%	12.50%	36 × 36 mult/100	1000	100 MHz	500	100 MHz	30 pF	4.25 GHz	4Tx/4Rx	1.25 GHz	8Tx + 8Rx

FPGA Power Consumption Derived from Spreadsheet[2]				
ICCINT + ICC	ICCIO	ICCA	ICCD	ICCXCVR
3.45 A (@ 1.1 V)	1.0 A (@ 2.5 V)	0.014 A (@ 2.5 V)	0.04 A (@ 1.1 V)	N/A
3.20 A (@ 1.1 V) 2.26 A (@ 0.90 V)	1.5 A (@ 2.5 V)	0.015 A (@ 2.5 V)	0.048 A (@ 1.1 V)	N/A
3.90 A (@ 0.90 V)	1.6 A (@ 2.5 V)	0.015 A (@ 2.5 V)	0.048 A (@ 1.1 V)	N/A
1.95 A (@ 0.90 V)	0.23 A (@ 2.5 V)	0.001 A (@ 2.5 V)	0.028 A (@ 0.9 V)	N/A
2.80 A (@ 0.90 V)	0.23 A (@ 2.5 V)	0.018 A (@ 2.5 V)	0.035 A (@ 0.9 V)	0.725 A (@ 1.2 V)
3.30 A (@ 0.90 V)[3]	0.25 A (@ 2.5 A)	0.02 A (@ 2.5 V)	0.045 A (@ 0.9 V)	0.725 A (@ 1.2 V)
4.30 A (@ 0.85 V)[3]	0.37 A (@ 2.5 V)	0.014 A (@ 2.5 V)	0.15 A (@ 1.5 V)	0.725 A (@ 1.2 V)
6.52 A (@ 0.85 V)[3]	0.45 A (@ 2.5 V)	0.019 A (@ 2.5 V)	0.15 A (@ 1.5 V)	0.82 A (@ 1 V)

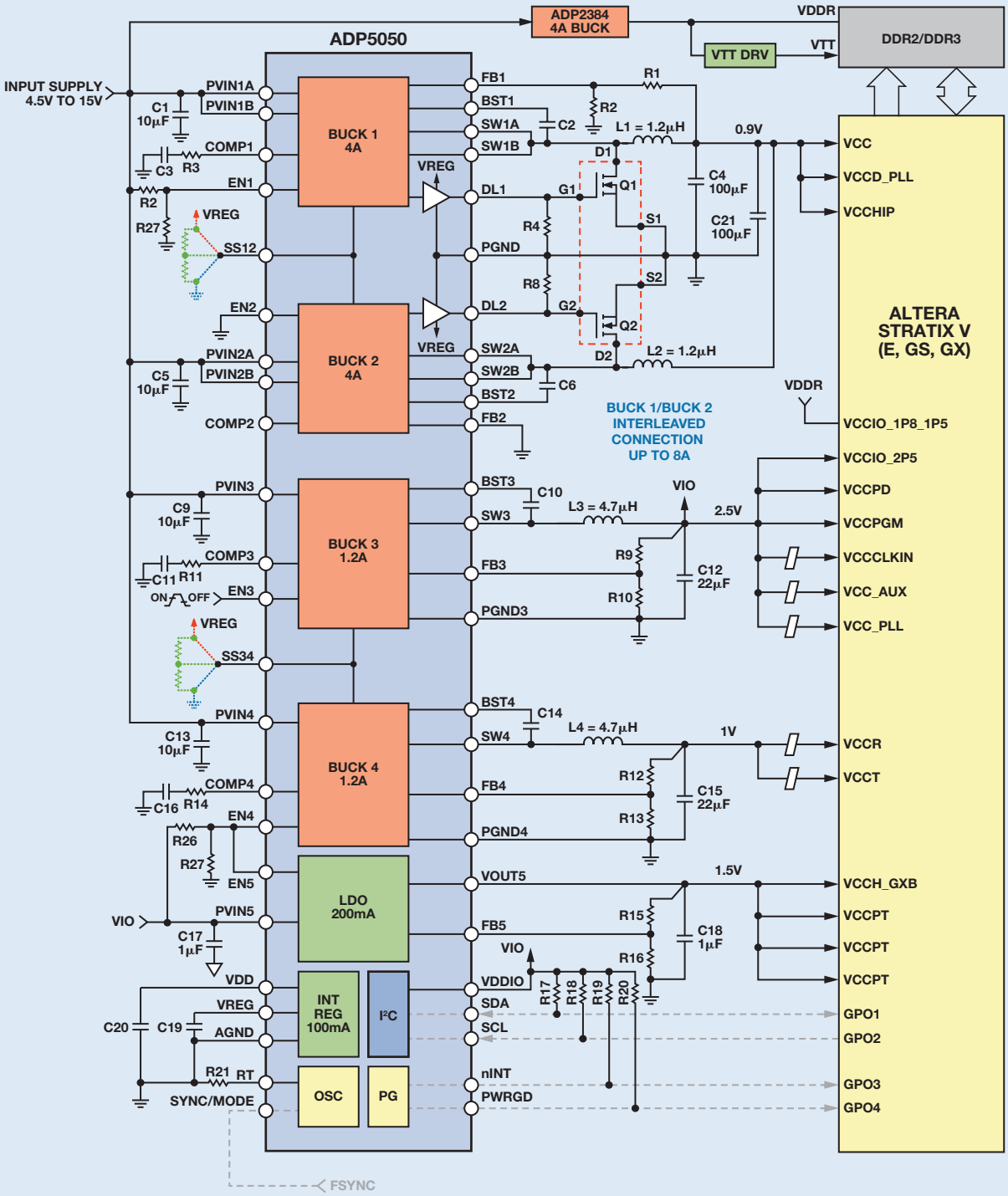
[1] Power requirement derived from Altera PowerPlay 12.1—the spreadsheet assumes at least 50% of resources occupation.
[2] Assumes 1.5 V I/O domain and DDR3 control interface, current consumption for the external DDR is not considered.
[3] 4 A to 8 A core current requirement can be achieved by connecting the ADP505x Buck 1 and Buck 2 used in interleaved configuration (see Stratix V and Arria V application diagrams).

Bill of Materials for the ADP5050 Powering Altera Stratix IV

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	5-channel micro PMU	ADP5050ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
C17, C18, C19, C20	4	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C8, C21	3	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C12, C15	2	22 µF, X5R, 6.3 V	GRM188R60J226MEA0	Murata	0603	
C3, C7, C11, C16	4	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 23 A, 25 mΩ	Si7228DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 10 A, 20 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1	1	2.2 µH, 15.9 A, 12.7 mΩ	XAL6030-222ME	Coilcraft	6.0 × 6.0 × 3.0	
		2.3 µH, 6.4 A, 22 mΩ	NRS6045-2R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L2, L3, L4	3	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R21	1	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8	2	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R5, R6, R9, R10, R12, R13, R15, R16,	14	Resistor, 1%		Various	0402	Value depends on output voltage setting
R3, R7, R11, R14	4	10 kΩ, resistor, 5%		Various	0402	
R17, R18, R19, R20	4	10 kΩ, resistor, 5%		Various	0402	Optional for I²C interface

ADP5050 Supply for Altera Stratix V

- Additional buck (ADP2384) for DDR
- External DDR termination driver
- Buck 1 and Buck 2 interleaved for 8 A



ADP5052—NON I²C VERSION

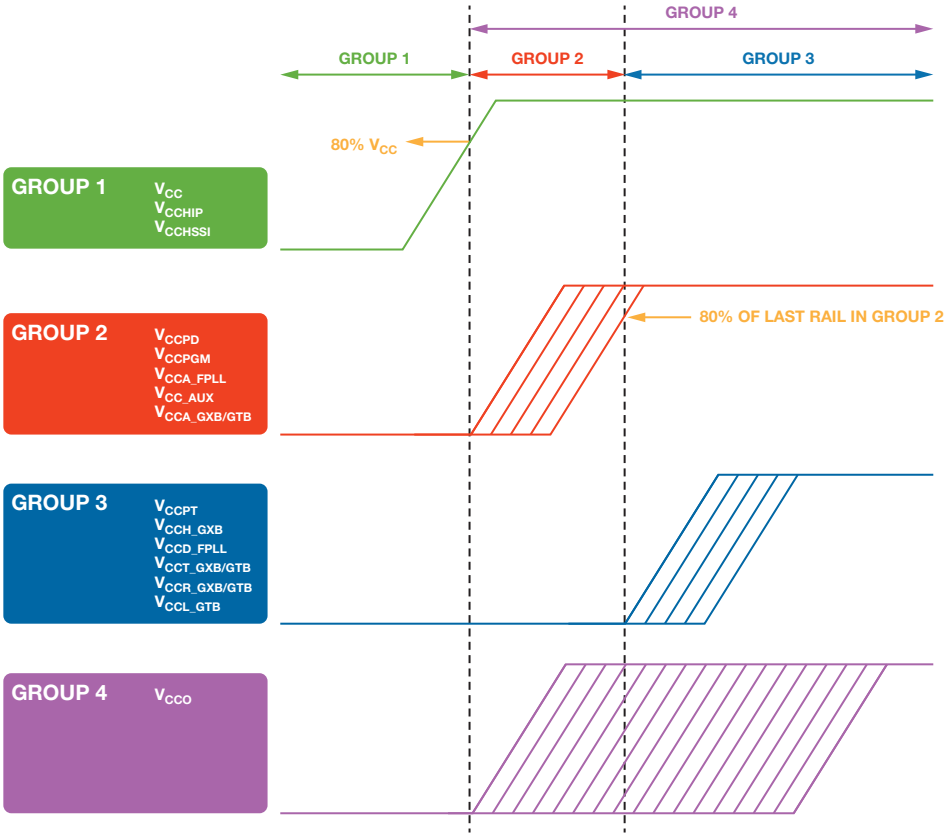
PowerPlay Power Estimation—Use Case for Altera Stratix V

See Page 5.

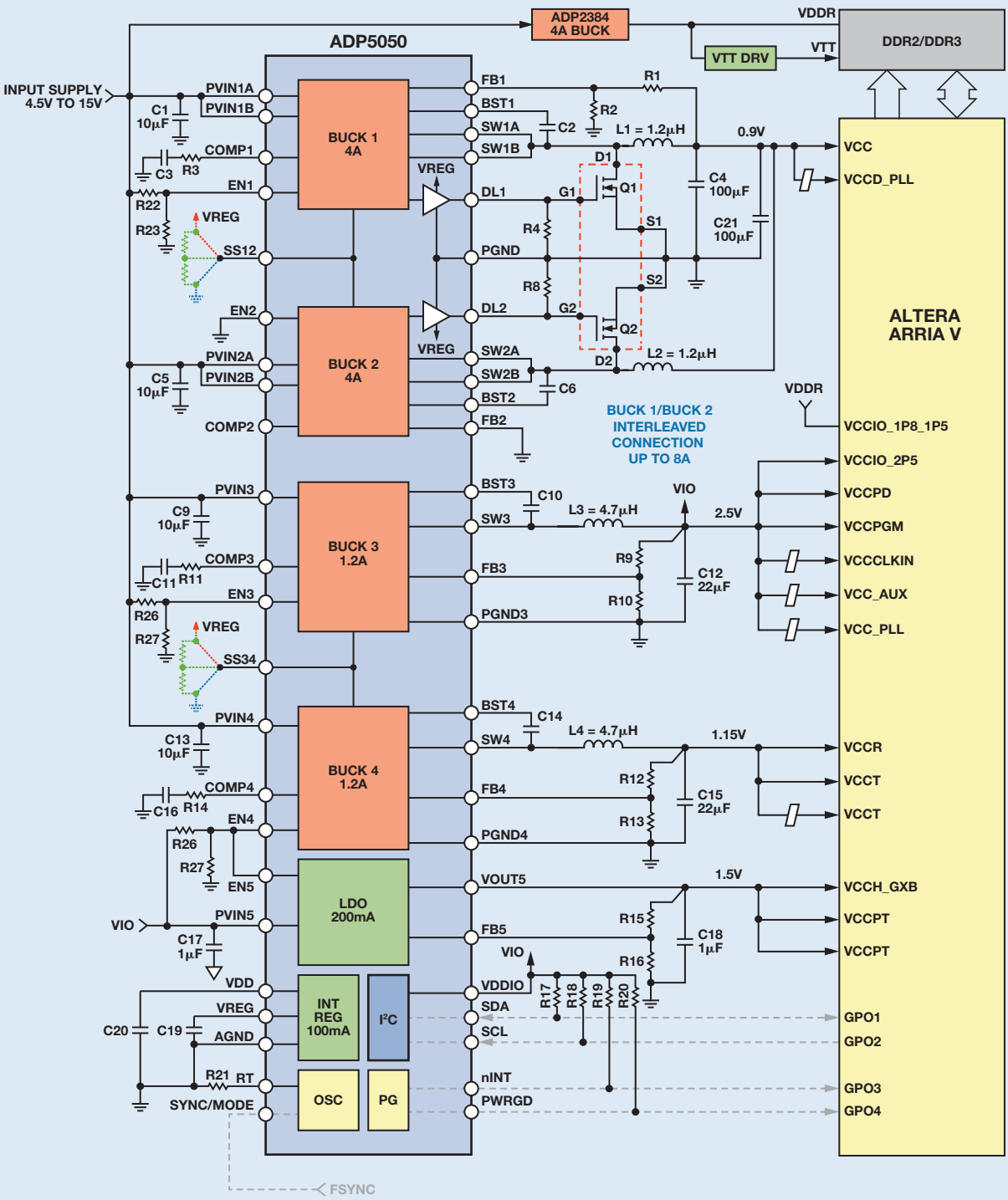
Bill of Materials for the ADP5050 Powering Altera Stratix V

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	5-channel micro PMU	ADP5050ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
U2	1	20 V, 4 A buck regulator	ADP2384ACPZN	ADI	4.0 × 4.0 × 0.75 QFN	Passive not included
C17, C18, C19, C20	4	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C21	2	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C15	2	22 µF, X5R, 6.3 V	GRM188R60J226MEA0	Murata	0603	
C3, C11, C16	4	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 23 A, 25 mΩ	Si7228DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 10 A, 20 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1, L2	2	1.2 µH, 22 A, 6.8 mΩ	XAL6030-122ME	Coilcraft	6.0 × 6.0 × 3.0	
		1.3 µH, 8.2 A, 16 mΩ	NRS6045-1R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L3, L4	2	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R21	1	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8	2	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R9, R10, R12, R13, R15, R16, R22, R23, R24, R25, R26, R27	14	Resistor, 1%		Various	0402	Value depends on output voltage setting and sequence threshold setting
R3, R11, R14	4	10 kΩ, resistor, 5%		Various	0402	
R17, R18, R19, R20	4	10 kΩ, resistor, 5%		Various	0402	Optional for I²C interface

Sequencing Requirements



ADP5050 Supply for Altera Arria V



ADP5052—NON I²C VERSION

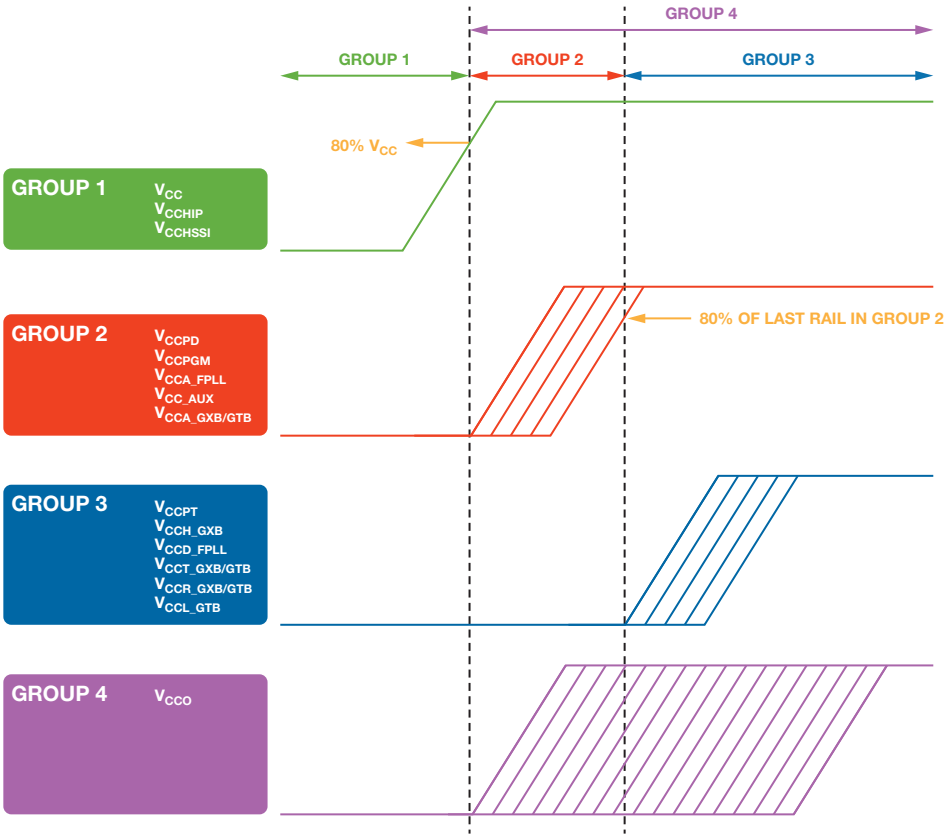
PowerPlay Power Estimation—Use Case for Altera Arria V

See Page 5.

Bill of Materials for the ADP5050 Powering Altera Arria V

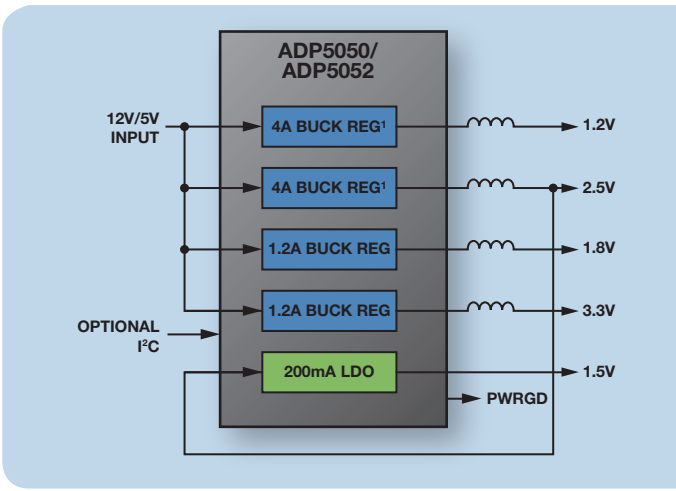
Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	5-channel micro PMU	ADP5050ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
U2	1	20 V, 4 A buck regulator	ADP2384ACPZN	ADI	4.0 × 4.0 × 0.75 QFN	Passive not included
C17, C18, C19, C20	4	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C21	2	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C15	2	22 µF, X5R, 6.3 V	GRM188R60J226MEA0	Murata	0603	
C3, C11, C16	4	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 23 A, 25 mΩ	Si7228DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 10 A, 20 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1, L2	2	1.2 µH, 22 A, 6.8 mΩ	XAL6030-122ME	Coilcraft	6.0 × 6.0 × 3.0	
		1.3 µH, 8.2 A, 16 mΩ	NRS6045-1R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L3, L4	2	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R21	1	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8	2	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R9, R10, R12, R13, R15, R16, R22, R23, R24, R25, R26, R27	14	Resistor, 1%		Various	0402	Value depends on output voltage setting and sequence threshold setting
R3, R11, R14	4	10 kΩ, resistor, 5%		Various	0402	
R17, R18, R19, R20	4	10 kΩ, resistor, 5%		Various	0402	Optional for I²C interface

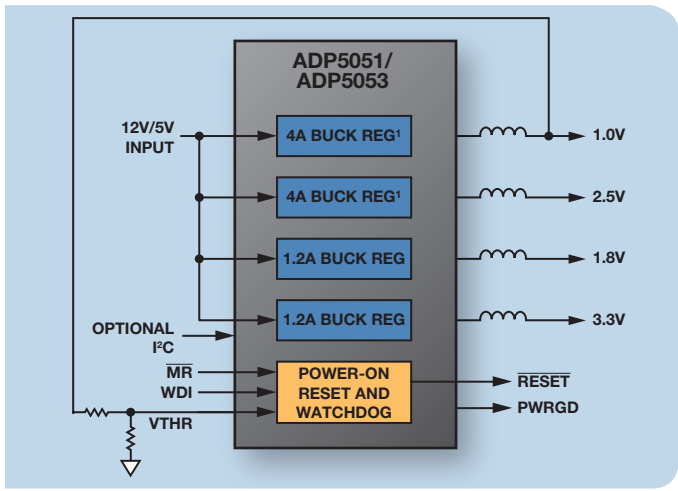
Sequencing Requirements



ADP5050/ADP5051/ADP5052/ADP5053

Quad Buck Switching Regulator with LDO or POR/WDI in LFCSP



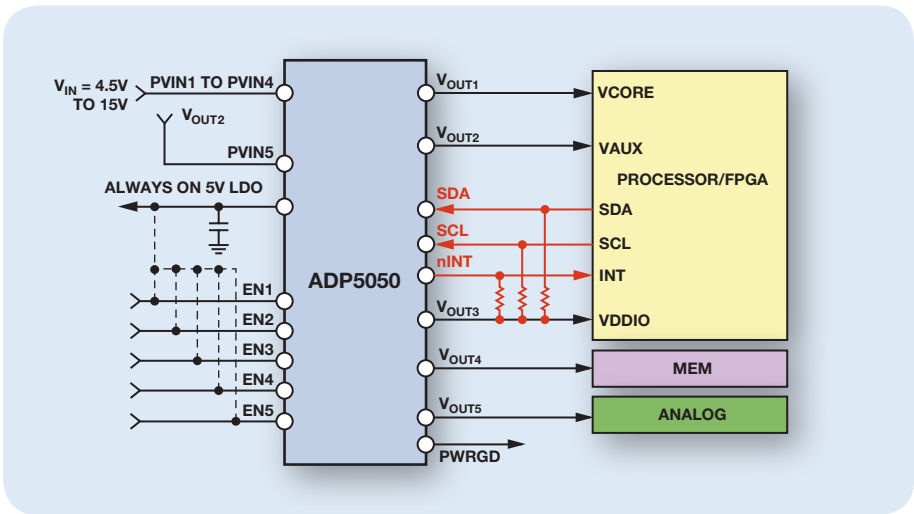


[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

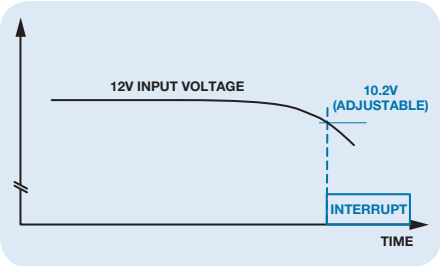
Key Features

- Wide input voltage range: 4.5 V to 15 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options
- Pseudo-DVS: dynamic voltage scaling
- I²C interface with interrupt supportive on fault condition
- CH1/CH2: programmable 1.2 A/2.5 A/4 A sync buck regulator with low-side FET driver
- CH3/CH4: 1.2 A sync buck regulator
- CH5: 200 mA low dropout LDO or watchdog timer and power-on reset
- Precision enable on 0.8 V accurate threshold
- Active output discharge switch
- FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag on selective channels
- Startup with the precharged output
- 48-lead, 7 mm × 7 mm LFCSP package
- −40°C to +125°C junction temperature
- I²C functionality

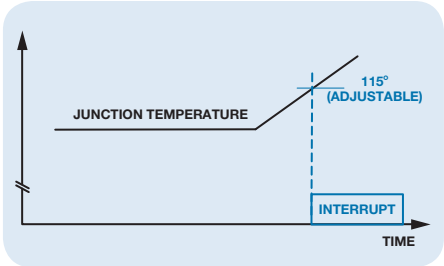
I²C Functionality



ADP5050 application diagram featuring the I²C interface.



Low input voltage detection on PVIN1.



Overheat function on junction temperature.

Option 1: Resistor programmable output voltage from 0.8 V to V_{IN} × 0.85

Option 2: Fixed output voltage with I²C programmability with these ranges for each channel

[CH1: 0.85 V TO 1.60 V, 25 mV STEP]

[CH2: 3.3 V TO 5.0 V, ~300 mV STEP]

[CH3: 1.2 V TO 1.80 V, 100 mV STEP]

[CH4: 2.5 V TO 5.5 V, 100 mV STEP]

ADP505x output voltage options.

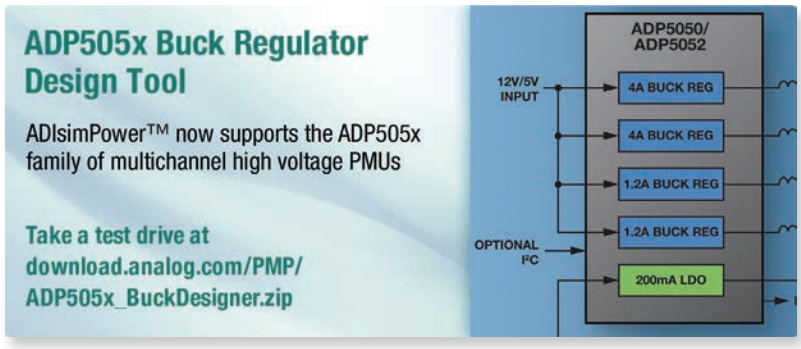
Integrated Power Management Solutions (Micro PMUs)

Part Number	Product Description	V_{IN} (V)	V_{OUT} (V)	Number of Outputs	Output Current (mA)	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Key Features	Package	Price ($U.S.)
ADP5022	Dual, 3 MHz buck regulator with 150 mA LDO	Buck: 2.3 to 5.5	3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8	2 × buck	600	—	—	—	—	Mode pin, individual enable pins	16-ball WLCSP	1.80
		LDO: 1.7 to 5.5	3.3, 3.0, 2.9, 2.8, 2.775, 2.5, 2.0, 1.875, 1.8, 1.75, 1.7, 1.65, 1.6, 1.55, 1.5, 1.2	1 × LDO	150							
ADP5023	Dual, 800 mA buck regulator with 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.59
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	1 × LDO	300							
ADP5024	Dual, 1.2 A buck regulator with300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.79
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	1 × LDO	300							
ADP5033	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	2 × buck	800	—	—	—	—	Mode pin, two enable pins	16-ball WLCSP	1.90
		LDO: 1.7 to 5.5	3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1.0, 0.9, 0.8	2 × LDO	300							
ADP5034	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP 28-lead TSSOP	1.99
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5037	Dual, 3 MHz, 800 mA buck regulator with dual 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.69
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5040	3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	—	—	—	Individual enable pins, mode pin	20-lead LFCSP	1.39
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5041	3 MHz buck regulator with dual LDO, supervisor, and watchdog timer	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	0.5 (adj)	20, 140	102, 1600	Individual enable pins and supervisor, WDI, mode pin, and MR pin	20-lead LFCSP	1.79
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5042	3 MHz buck regulator with dual LDO, supervisor, and dual watchdog timers	Buck: 2.3 to 5.5	3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	1 × buck	800	—	4.63, 3.08, 2.93, 2.63, 2.50, 2.35, 2.068, 1.692	20, 140	102, 1600	Individual enable pins and supervisor, WDI, WDI2, mode pin, and MR pin	20-lead LFCSP	1.99
		LDO: 1.7 to 5.5	3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1, 0.9, 0.8	2 × LDO	300	—						
ADP5043	3 MHz buck regulator with LDO, supervisor, and dual watchdog timers	Buck: 2.3 to 5.5	3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	1 × buck	800	—	4.63, 3.08, 2.93, 2.63, 2.50, 2.35, 2.068, 1.692	20, 140	102, 1600	Individual enable pins and supervisor, WDI, WDI2, mode pin, and MR pin	20-lead LFCSP	1.79
		LDO: 1.7 to 5.5	3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1, 0.9, 0.8	1 × LDO	300							
ADP320	Triple, 200 mA LDO	1.8 to 5.5	LDO1: 3.3; LDO2: 1.8, 3.3; LDO3: 1.5	3 × LDO	200	—	—	—	—	Fixed V_{OUT} options	16-lead LFCSP	0.54
ADP322	Triple, 200 mA LDO	1.8 to 5.5	LDO1: 3.3, 2.8, 2.5; LDO2: 2.8, 2.5, 1.8; LDO3: 1.8. 1.5, 1.2	3 × LDO	200					Fixed V_{OUT} options	16-lead LFCSP	0.54
ADP323	Triple, 200 mA LDO	1.8 to 5.5	Adj (0.5 to 5)	3 × LDO	200	—	—	—	—	Adjustable V_{OUT} options	16-lead LFCSP	0.54
ADP5050 ***New***	Quad buck regulator + LDO with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	—	—	—	I²C interface with individual enable pins and power good	48-lead LFCSP	4.39
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5051 ***New***	Quad buck regulator + POR and WDI with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	I²C interface with individual enable pins and power good	48-lead LFCSP	4.59
				2 × buck	1200							
ADP5052 ***New***	Quad buck regulator + LDO	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	—	—	—	Individual enable pins with power good	48-lead LFCSP	3.59
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5053 ***New***	Quad buck regulator + POR and WDI	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	Individual enable pins with power good	48-lead LFCSP	3.79
				2 × buck	1200							
ADP5134 ***New***	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.5 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Precision enables, power good pin	24-lead LFCSP	2.09
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							

[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

ADP505x Design Tool

ADIsimPower™ now supports the ADP505x family of multichannel high voltage PMUs. This new family of parts supports 4/5 channels from inputs up to 15 V with load current up to 4 A per channel. Users can optimize the design by taking into account the thermal contributions of each channel by cascading channels, and even by placing the high current channels in parallel to create an 8 A rail. With the advanced features, users can specify independently each channel's performance, from ripple and transient, to switching frequency selection from the channels that support half the master frequency. As with all the other tools, evaluation boards are available by request directly from the tool. Download at *download.analog.com/PMP/ADP505x_BuckDesigner.zip*.

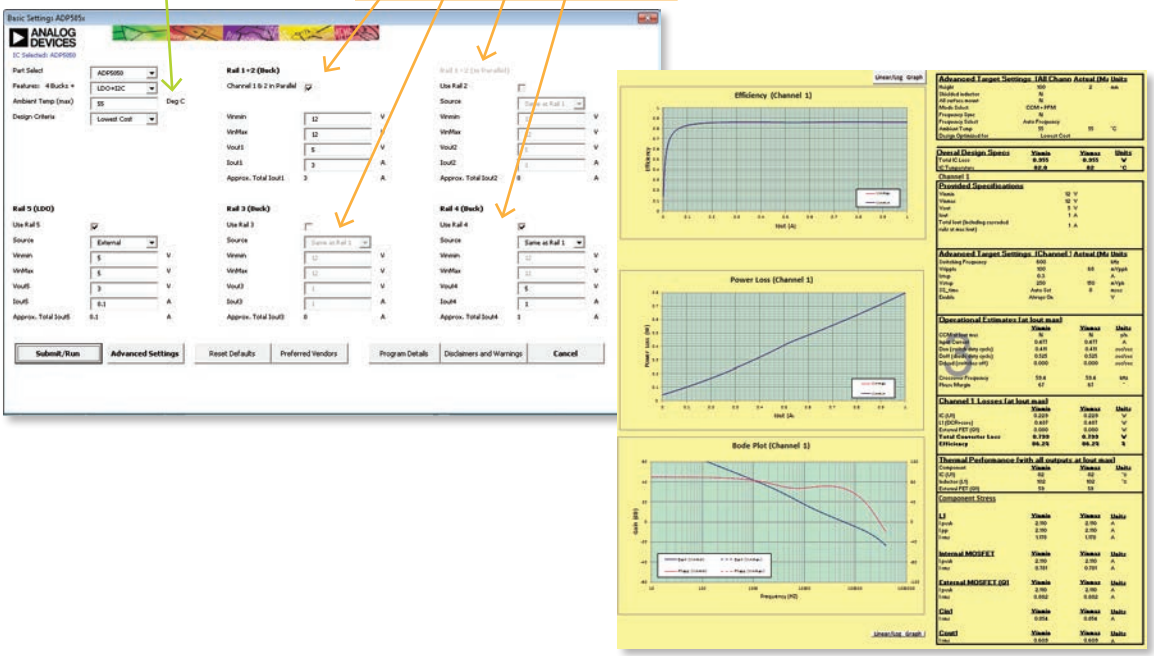


Step 1:

Optimize for size, cost, or efficiency

Step 2:

Specify each channel's operating conditions, including "do not use"



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