

Evaluating the **ADP5056** Triple Buck Regulator Integrated Power Solution

FEATURES

Wide input voltage range: 2.75 V to 18 V

Bias input voltage range: 4.5 V to 18 V

Full-featured evaluation board for the **ADP5056**

**Channel 1 and Channel 2: 7 A synchronous buck regulator,
or 14 A output in parallel operation**

Channel 3: 3 A synchronous buck regulator

Selective PSM or FPWM operation

Programmable switching frequency from 2.5 MHz to 250 kHz

Frequency synchronization input or output

GENERAL DESCRIPTION

This user guide describes the evaluation of the [ADP5056](#) and includes detailed schematics and printed circuit board (PCB) layouts.

The ADP5056-EVALZ features the [ADP5056](#), which combines three high performance buck regulators in a 43-terminal land grid array (LGA) to meet the demanding performance and board space requirements. The ADP5056-EVALZ connects to input voltages up to 18 V directly, without any preregulators.

Full details on the device are provided in the [ADP5056](#) data sheet, available from Analog Devices, Inc. Consult this data sheet in conjunction with this user guide when evaluating the [ADP5056](#).

ADP5056-EVALZ PHOTOGRAPH

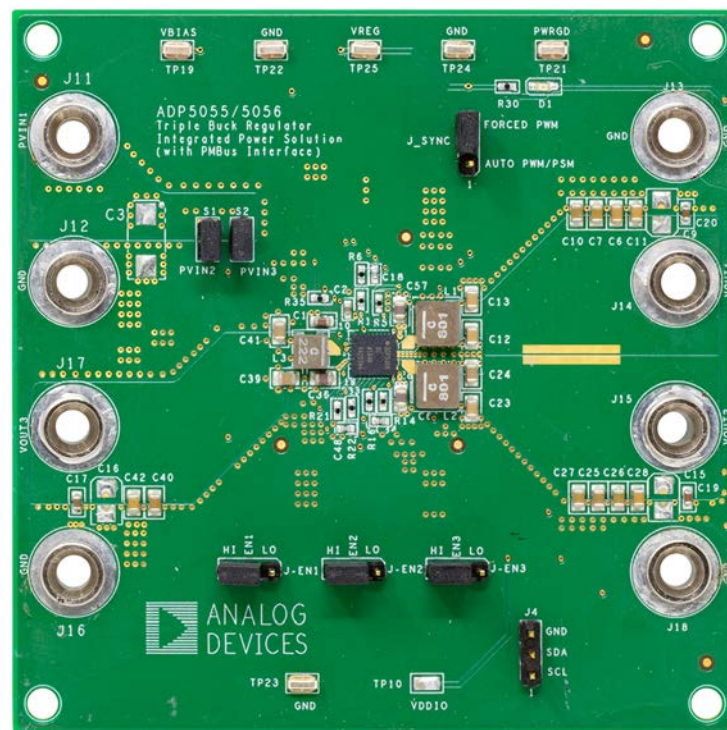


Figure 1.

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REVISION HISTORY

5/2020—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADP5056-EVALZ is fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

ENABLE JUMPERS

Each channel has an enable pin that must be pulled high to enable that channel (see Table 1). Pull the enable pin low or leave it floating to disable the channel.

The enable control for each regulator has a 0.615 V precision enable threshold, which allows the ADP5056 to be sequenced between channels or other input/output supplies.

Table 1. Enable Pin Channels

Channel	Pin Name	Enable Jumpers
Channel 1	EN1	J-EN1
Channel 2	EN2	J-EN2
Channel 3	EN3	J-EN3

POWER INPUT JUMPERS

Each channel has its own power input jumper, which supports separate input voltages or cascaded options for all channels.

The input voltage range for the three buck regulators is 4.5 V to 18 V. If separate power supplies are used for PVIN1 and VBIAS with R35 removed (on the ADP5056-EVALZ, PVIN1 and VBIAS are connected together through the R35, 0 Ω resistor by default), the input voltage range for the three buck regulators is 2.75 V to 18 V. Shunt S1 and S2 to allow easy setup by using the same input voltages for the three buck regulators. See Table 2 for the power input details.

Table 2. Power Input Pin Channels

Channel	Pin Name	Input Jumper	Input Range (V)
Channel 1	PVIN1	J11	4.5 to 18
Channel 2	PVIN2	S1	4.5 to 18
Channel 3	PVIN3	S2	4.5 to 18

J-SYNC JUMPER (SYNC/MODE)

The J-SYNC jumper, as shown in Figure 1, is used to connect the SYNC/MODE pin of the device to either low (GND) or high (VREG).

- Shunt the center contact of J-SYNC (SYNC_MODE) to the top pin header, which pulls the SYNC/MODE pin high to VREG (4.8 V) to allow the three buck regulators into forced pulse width modulation (FPWM) operation.
- Shunt the center contact of J-SYNC to the bottom pin header, which pulls the SYNC/MODE pin low to force the three buck regulators to operate in automatic pulse width modulation/power saving mode (PWM/PSM) operation.

INPUT POWER SOURCE

Use the following steps to connect the evaluation board to the input power source:

- Ensure that the evaluation board is disabled by connecting the enable jumpers (J-EN1 to J-EN3) to the low position before connecting the power source to the ADP5056-EVALZ.
- If the input power source includes a current meter, use the meter to monitor the input current.
- Connect the positive terminal of the power source to the PVIN1 terminal (J11) on the evaluation board, and connect the negative terminal of the power source to the GND terminal (J12) of the evaluation board.
- If the power source does not include a current meter, connect a current meter in series with the input source voltage.
- Connect the positive terminal of the power source to the positive lead of the current meter, the negative terminal of the power source to the GND terminal (J12) on the evaluation board, and the negative lead of the current meter to the PVIN1 terminal (J11) on the board.

OUTPUT LOAD

Use the following steps to connect the evaluation board to the output load:

- Ensure that the evaluation board is turned off before connecting the load.
- Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board, with the positive load connected to one of the channels. For example, connect the positive load terminal to the Channel 1 buck regulator output, J14 (VOUT1), and connect the negative load terminal to J13 (GND).
- If an ammeter is used, connect it in series with the load.
- Connect the positive ammeter terminal to the Channel 1 buck regulator output, J14 (VOUT1), connect the negative ammeter terminal to the positive load terminal, and connect the negative load terminal to J13 (GND).

INPUT AND OUTPUT VOLTMETERS

Use the following steps to measure the input and output voltages with voltmeters:

- Ensure that the voltmeters are connected to the appropriate evaluation board terminals and not to the load or power sources themselves. If the voltmeters are not connected directly to the evaluation board, the measured voltages are inaccurate due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.
- Connect the voltmeter positive terminal measuring the input voltage to J11 (PVIN1), and connect the voltmeter negative terminal measuring the input voltage to J12 (GND).

3. Connect the voltmeter positive terminal measuring the output voltage of the Channel 1 buck regulator to J14 (VOUT1), and connect the voltmeter negative terminal measuring the output voltage to J13 (GND).

QUICK STARTUP

Verify the following before powering up the evaluation board:

- The power source voltage for the three buck regulators (PVIN1, PVIN2, and PVIN3) is 4.5 V to 18 V. Shunt the S1 and S2 jumpers to use the same input voltage for all three buck regulators
- Use the J-EN1, J-EN2, and J-EN3 jumpers to enable or disable the desirable channel

When the power source and load are connected to the evaluation board, the evaluation board can be powered for operation. If the load is not enabled, enable the load. Check that the load is drawing the proper current and that the output voltage maintains voltage regulation.

After power-up, the following output voltages (V_{OUTx}) can be measured:

- $V_{OUT1} = 1.0$ V, supply up to 7 A continuous load current
- $V_{OUT2} = 1.3$ V, supply up to 7 A continuous load current
- $V_{OUT3} = 1.8$ V, supply up to 3 A continuous load current

MEASURING EVALUATION BOARD PERFORMANCE

MEASURING OUTPUT VOLTAGE RIPPLE OF THE BUCK REGULATOR

To observe the output voltage ripple of Channel 1, place an oscilloscope probe across the output capacitor (C_{OUT1}) with the probe ground lead at the negative capacitor terminal and the probe tip at the positive capacitor terminal.

Set the oscilloscope to ac coupling and 1 μ s/division time base, with the bandwidth set to 20 MHz to avoid noise that interferes with the measurements. It is recommended to shorten the ground loop of the oscilloscope probe to minimize coupling.

An accurate output voltage ripple measurement can be performed across C11 or C20 using the proper measurement technique as shown in Figure 2.

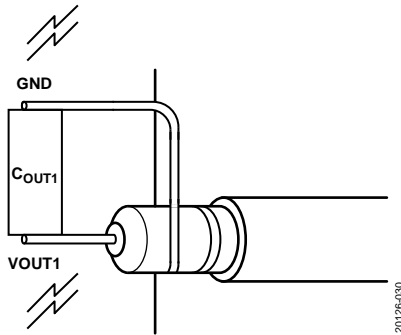


Figure 2. Measure Output Voltage Ripple

MEASURING THE SWITCHING WAVEFORM OF THE BUCK REGULATOR

To observe the switching waveform using an oscilloscope, place the oscilloscope probe tip at the exposed copper trace at the SWx terminal of the inductor with the probe ground at GND. Set the oscilloscope to dc coupling, 5 V/division, and 1 μ s/division time base.

When the SYNC/MODE pin is set to high, the buck regulators operate in FPWM mode. When the SYNC/MODE pin is set to low, the buck regulators operate in PSM, improving the light load efficiency.

EVALUATING THE SYNCHRONIZATION INPUT OR OUTPUT

The SYNC/MODE pin can be configured as the clock output by the CFG1 pin. A clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with the frequency equal to the internal frequency set by the RT pin.

When the SYNC/MODE pin is configured as the input, the ADP5056 can be synchronized to an external clock applied to the SYNC/MODE pin. The internal switching frequency set by the RT pin must be programmed to a value close to the external clock value.

EVALUATING EFFICIENCY

Measure the efficiency, η , by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

where:

V_{OUT} is the output voltage.

I_{OUT} is the output current.

V_{IN} is the input voltage.

I_{IN} is the input current.

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of the trace voltage drops.

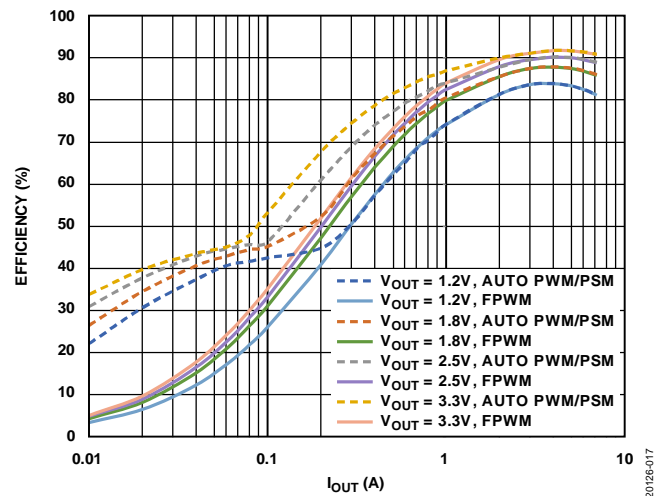


Figure 3. Typical Channel 1/Channel 2 Efficiency, $V_{IN} = 12$ V, Switching Frequency (f_{SW}) = 600 kHz, FPWM and PSM Mode

MODIFYING THE BOARD

Setting the Output Voltages

The output voltage three buck regulators are set through external resistor dividers, as shown in Figure 4, for Channel 1. The equation for setting the output voltage is

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}} \right)$$

where:

V_{REF} is the reference voltage, $V_{REF} = 0.6$ V.

R_{TOP} is the top resistor in the feedback voltage divider.

R_{BOT} is the bottom resistor in the feedback voltage divider.

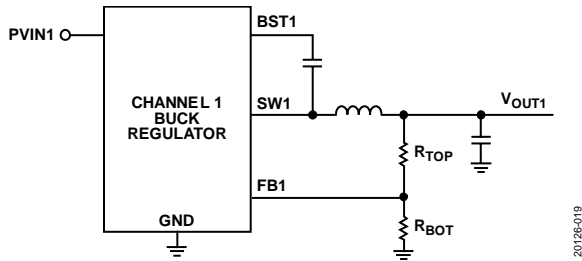


Figure 4. Channel 1 Output Voltage Setting

When the output voltage of the buck regulator is changed, the values of the inductors, the output capacitors, and the compensation networks may require recalculation and changes for stable operation. Refer to the [ADP5056](#) data sheet for details on external components selection.

The ADP5056-EVALZ is supplied with resistor dividers for setting target output voltages. Table 3 shows the external resistor divider components for each channel.

Table 3. External Resistor Dividers in Each Channel

Resistor Divider	Channel 1	Channel 2	Channel 3
R _{TOP}	R2	R13	R23
R _{BOT}	R7	R17	R25

Changing the Switching Frequency

The switching frequency of ADP5056-EVALZ is programmed to be 600 kHz by default. To change the switching frequency (within the range of 2.5 MHz to 250 kHz), replace the R3 resistor connected to the RT pin with a different value. Refer to the [ADP5056](#) data sheet for the relationship between switching frequency and the RT resistor. When the switching frequency is changed, the values of the inductors, output capacitors, and the compensation networks may need to be recalculated and changed for stable operation. Refer to the [ADP5056](#) data sheet for more details on external components selection.

Setting Channel 1 and Channel 2 to Interleaved Parallel Operation

Channel 1 and Channel 2 are configured as individual outputs on the ADP5056-EVALZ by default. To configure Channel 1 and Channel 2 to operate in interleaved parallel single output mode, follow these steps:

- Short J14 and J15
- Ensure that Jumper S1 is shunted
- Change R26 to 23.7 k Ω on the CFG1 pin
- Remove R16 and C34 on the COMP2 pin
- Remove R13, and replace R17 with 0 Ω on the FB2 pin
- Shunt the J-EN2 jumper to low
- Use the Channel 1 feedback resistor dividers, R2 and R7, to set the output voltage
- Use J-EN1 (EN1 pin) to enable or disable the regulator

During parallel operation, the input voltage and current-limit threshold for both channels are the same, and FPWM mode operation on both Channel 1 and Channel 2 is recommended. Refer to the [ADP5056](#) data sheet for more details on inphase parallel operation and interleaved parallel operation.

Phase Shift (0°, 120°, 240°) in the Three Buck Regulators

In the ADP5056-EVALZ, the phase shift is 120° between Channel 1, Channel 2, and Channel 3. This value provides the benefits of out of phase operation by reducing the input ripple current and lowering the ground noise.

EVALUATION BOARD SCHEMATICS AND ARTWORK

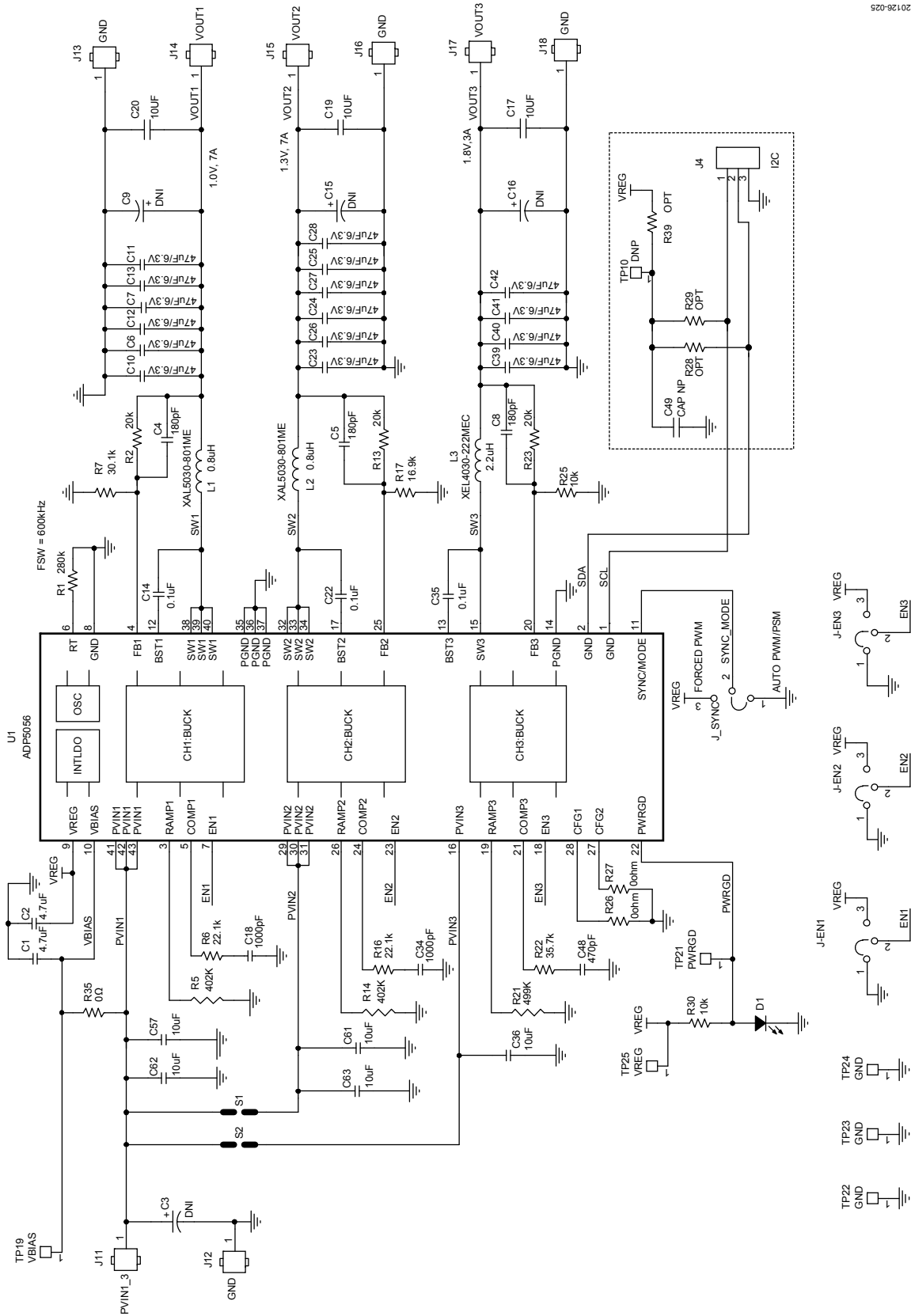


Figure 5. Evaluation Board Schematic of the ADP5056

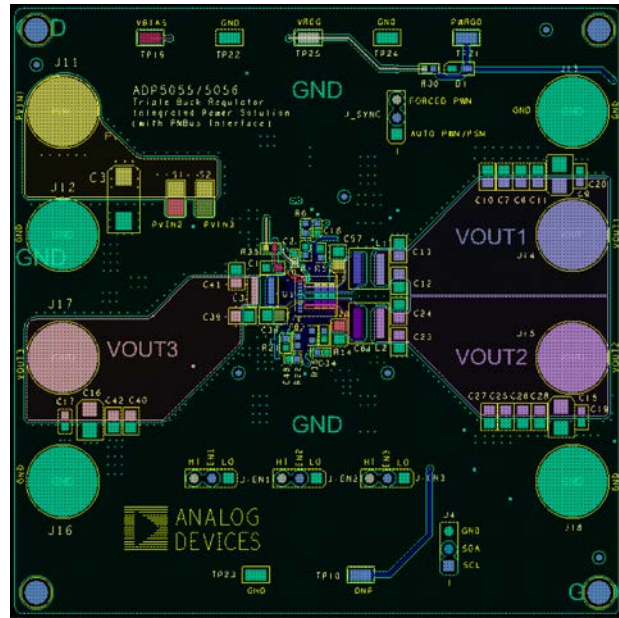


Figure 6. Top Layer, Recommended Layout for ADP5056

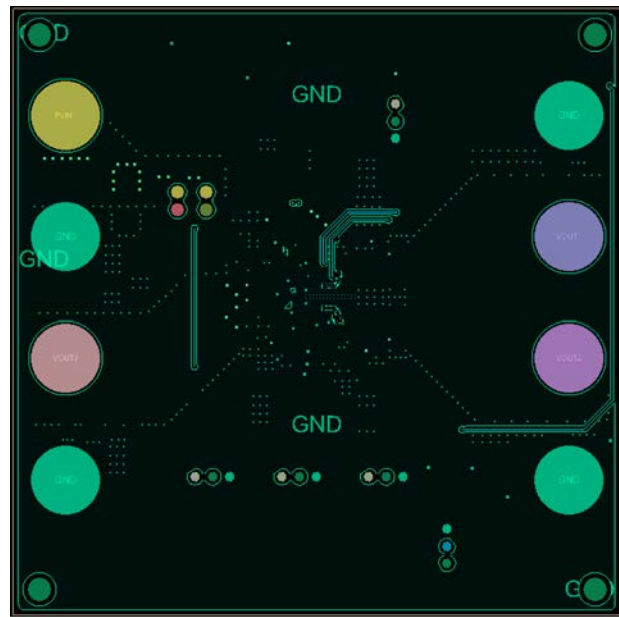


Figure 7. Second Layer, Recommended Layout for ADP5056

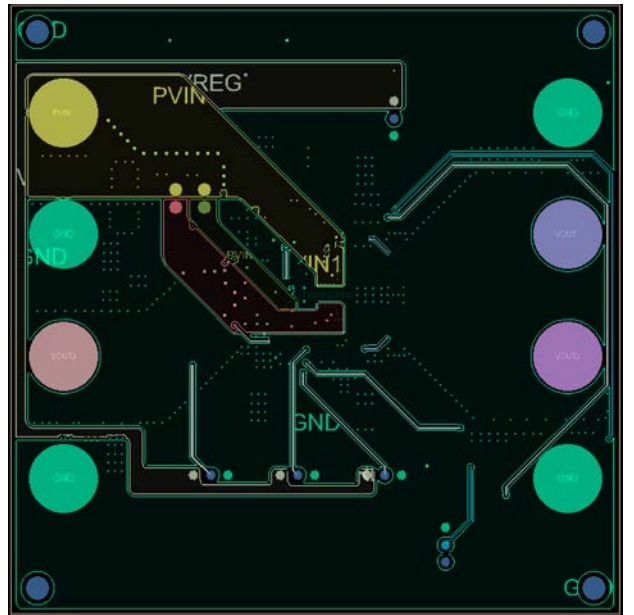


Figure 8. Third Layer, Recommended Layout for ADP5056

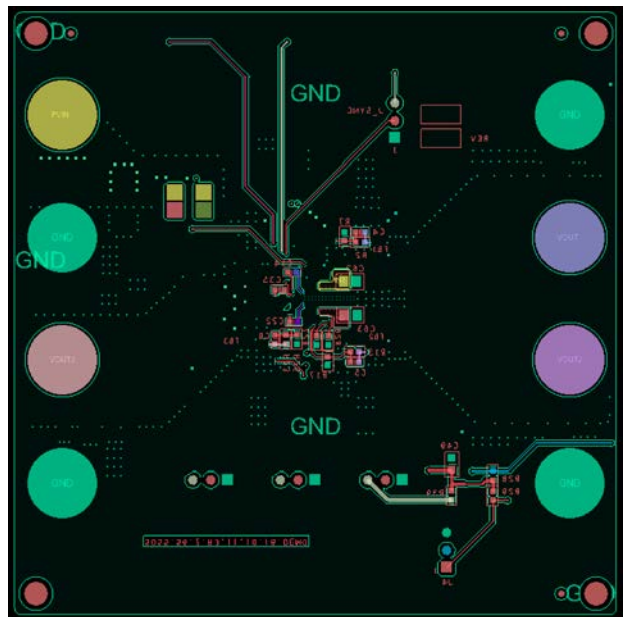


Figure 9. Bottom Layer, Recommended Layout for ADP5056

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	C1	Ceramic capacitor, 4.7 μ F, X6S, 25 V, 10%, 0603	Murata	GRM188C81E475KE11
1	C2	Ceramic capacitor, 4.7 μ F, X6S, 6.3 V, 20%, 0402	Murata	GRM155C80J475MEAA
3	C4, C5, C8	Ceramic capacitors, 180 pF, C0G, 50 V, 1%, 0402	Murata	GCM1555C1H181FA16D
16	C6, C7, C10 to C13, C23 to C28, C39 to C42	Ceramic capacitors, 47 μ F, 6.3 V, 20%, 0805	Murata/Taiyo Yuden	GRM21BR60J476ME11, MK212BJ476MG-T
3	C14, C22, C35	Ceramic capacitors, 0.1 μ F, X7R, 16 V, 10%, 0402	KEMET	C0402C104K4RACTU
2	C18, C34	Ceramic capacitors, 1 nF, 50 V, 5%, 0402	Murata	GRM1555C1H102JA01
5	C36, C57, C61 to C63	Ceramic capacitors, 10 μ F, X7S, 25 V, 10%, 0805	Murata	GRM21BC71E106KE11
3	C17, C19, C20	Ceramic capacitors, 10 μ F, X5R, 10 V, 10%, 0603	Murata	GRM188R61A106KAAL
5	C3, C9, C15, C16, C49	Capacitors		Do not install (DNI)
1	C48	Ceramic capacitor, 470 pF, C0G, 50 V, 5%, 0402	Murata	GRT1555C1H471JA02
1	D1	Clear green LED, 0603, surface-mount device (SMD)	LITE-ON	LTST-C191KGKT
4	J-EN1, J-EN2, J-EN3, J_SYNC	2.54 mm, 3-pin headers	Würth	61300311121
2	S1, S2	2.54 mm, 2-pin headers	Würth	61300311121
8	J11 to J18	Noninsulated jacks, .218 inches	Keystone Electronics	575-4
2	L1, L2	Inductors, 0.8 μ H	Coilcraft	XAL5030-801ME
1	L3	Inductor, 2.2 μ H	Coilcraft	XEL4030-222ME
1	R1	Resistor, SMD, 280 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW0402280KFKED
3	R2, R13, R23	Resistors, SMD, 20 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW040220K0FKED
2	R5, R14	Resistors, SMD, 402 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW0402402KFKED
2	R6, R16	Resistors, SMD, 22.1 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW040222K1FKED
1	R7	Resistor, SMD, 30.1 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW040230K1FKED
1	R17	Resistor, SMD, 16.9 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW040216K9FKED
1	R21	Resistor, SMD, 499 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW0402499KFKED
1	R22	Resistor, SMD, 35.7 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW040235K7FKED
2	R25, R30	Resistors, SMD, 10 k Ω , 1%, 1/16 W, 0402	Vishay Dale	CRCW040210K0FKED
3	R26, R27, R35	Resistors, SMD, 0 Ω , jumper, 1/10 W, 0603	Vishay Dale	CRCW04020000Z0ED
3	R28, R29, R39	Resistors, 0402		DNI
6	TP19, TP21 to TP25	Test points, miniature	Keystone Electronics	5019
1	TP10	Test point		DNI
1	U1	Triple buck regulator	Analog Devices	ADP5056

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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