

Signal Chain Power ADP7142 Low Noise, CMOS LDO Linear Regulator

DESCRIPTION

Demonstration circuit SCP-ADP7142-EVALZ is a 40V, 200mA low dropout (LDO) regulator designed to allow low noise operation in noise sensitive circuits. It is easily configured for a wide output range and can provide extremely quiet operation with its high PSRR.

Like all boards in the Signal Chain Power series, this board is designed to be easily plugged into other SCP boards to form a complete signal chain power system, enabling fast evaluation of low power signal chains. To evaluate this board, some universal SCP hardware is required, namely:

- SCP-INPUT-EVALZ SCP-FILTER-EVALZ
- SCP-OUTPUT-EVALZ SCP-1X2BKOUT-EVALZ
- SCP-1X5BKOUT-EVALZ SCP-5X1-EVALZ
- SCP-THRUBRD-EVALZ

To properly evaluate SCP series demo boards, you will need the SCP Configurator companion software. SCP Configurator can help you choose the right board and topology for your design.

Note that this Demo Manual does not cover details important to the operation and configuration regarding the [ADP7142](#). Please refer to the [ADP7142 datasheet](#) for a complete description of the part.

Design files for this circuit board are available.

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Table 1. Performance Summary

SYMBOL	PARAMETER	NOTES	MIN	TYP	MAX	UNITS
$V_{IN(MAX)}$	Max Input Voltage				40	V
$V_{OUT(MAX)}$	Max Output Voltage				39.58	V
$I_{OUT(MAX)}$	Max Output Current				200	mA

BOARD IMAGE

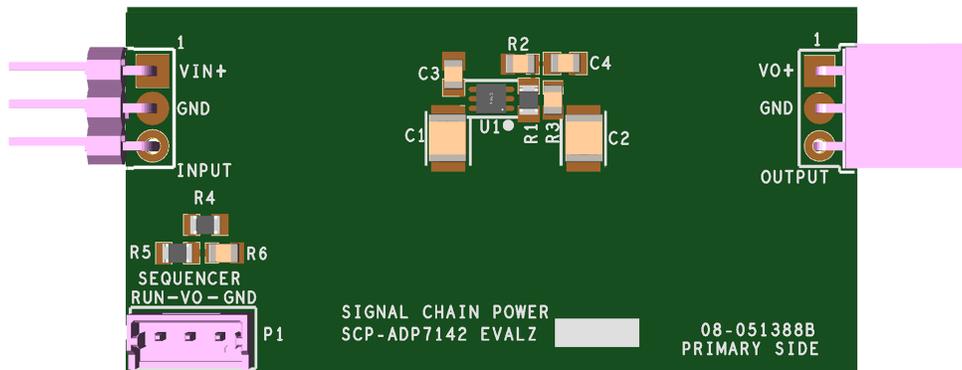


Figure 1. SCP-ADP7142-EVALZ Board

DEMO MANUAL SCP-ADP7142-EVALZ

QUICK START PROCEDURE

Demonstration circuit SCP-ADP7142-EVALZ is easy to set up to evaluate the performance of any SCP hardware configuration.

1. The SCP-ADP7142-EVALZ ships with a default output voltage of 3.3V. To change the output voltage, see “Configuration Settings” section, and modify the board accordingly. Be sure to check for open connections or solder shorts after making any modifications.
2. Connect the SCP-INPUT-EVALZ and SCP-OUTPUT-EVALZ boards to the SCP-ADP7142-EVALZ (refer to Figure 2) and connect the input board to a voltage source, V_{SOURCE} . Connect the output board to a voltmeter or dynamic load. Slowly raise the input voltage until the SCP-ADP7142-EVALZ powers up into regulation and sweep V_{SOURCE} through the desired range of operation.

NOTE: Make sure that the input voltage is always within spec. If using a dynamic load to measure output voltage, make sure the load is initially set to zero.

3. Check for proper output voltage. The output should be regulated at the programmed value ($\pm 5\%$).
4. Once the proper output voltage is established, power off V_{SOURCE} and similarly test other boards in the SCP system until all elements have been individually verified prior to assembling into the final circuit configuration.

NOTE: When measuring the input or output voltage ripple, use the optional SMA connector locations available on the input, output, 1 × 5, 1 × 2, and 5 × 1 breakout boards. Avoid using the test point connections with long scope leads.

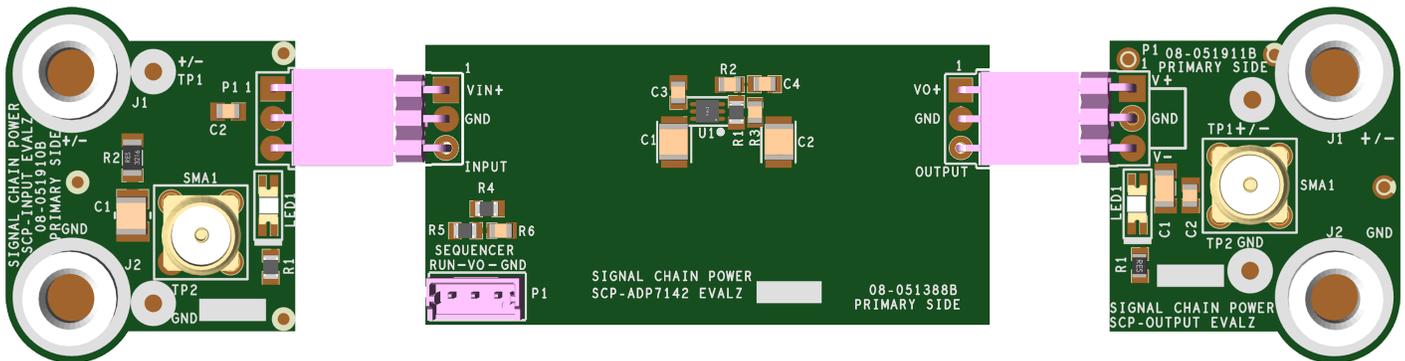


Figure 2. Proper Measurement Equipment Setup (Use SMA connectors for Measuring Input or Output Ripple)

CONFIGURATION SETTINGS

Demonstration circuit SCP-ADP7142-EVALZ is a 40V, 200mA Low Dropout (LDO) regulator designed to allow low noise operation in noise sensitive circuits. It is easily configured for a wide output range and can provide extremely quiet operation with its high PSRR.

The output of the SCP-ADP7142-EVALZ is resistor-programmable from 1.2V to 39.5V.

OUTPUT VOLTAGE PROGRAMMING

$$V_{OUT} = 1.2V \left(1 + \frac{R1}{R2} \right)$$

Table 2. Resistor Selection Guide for Common Output Voltages

V _{OUT} (V)	R1 (Ω)	R2 (Ω)
1.2	0	Open
1.25	1.07k	25.5k
1.5	2.55k	10.2k
1.8	5.90k	11.8k
2.0	10.0k	15.0k
2.5	16.2k	15.0k
2.7	18.7k	15.0k
3.0	15.0k	10.0k
3.3	18.7k	10.7k
3.5	41.2k	21.5k
4.0	24.9k	10.7k
4.5	31.6k	11.5k
5.0	47.5k	15.0k
5.5	41.2k	11.5k
6.0	102k	25.5k
6.5	280k	63.4k
7.0	107k	22.1k
7.5	105k	20.0k
8.0	113k	20.0k
8.5	69.8k	11.5k
9.0	71.5k	11.0k
9.5	102k	14.7k
10	110k	15.0k
11	133k	16.2k
12	102k	11.3k
13	113k	11.5k
14	200k	18.7k
15	115k	10.0k
20	215k	13.7k
25	102k	5.11k
30	255k	10.7k
35	324k	11.5k
39.5	340k	10.7k

ENABLE PIN CONFIGURATION

The EN pin is tied to the optional SCP Run/Sequence header P1. To create a harness for this function, use Molex part 0510650300 with crimp pin 50212-8000.

To use an active run signal, use a 1.00MΩ resistor for either pull-up or pull-down resistors R4 and R6, short R5 with 0Ω, and use the drive signal from connector P1.

If precision undervoltage lockout (UVLO) operation is desired, program enable divider R4 and R6 such that:

R6 in the 10k–100k (nominal) range.

$$R4 = R6 \left(\frac{V_{IN} - 1.2V}{1.2V} \right)$$

The hysteresis threshold is 100mV typical, and scales by the factor:

$$V_{HYST} = 100mV \frac{R4 + R6}{R6}$$

SOFT-START CONFIGURATION

The SS pin can be used to limit inrush current to the load by retarding the output voltage slew. With the pin left open, the startup time defaults to approximately 380μs. This can be modified with additional capacitance C_{SS} to increase the soft-start time t_{SS}:

$$t_{SS}(s) = 380 + \left(\frac{0.6}{1.15} \right) C_{SS}$$

Table 3. Soft Start Capacitance Configuration

C _{SS}	t _{SS} (approx.)
180pF	500ns
1.5nF	1ms
10nF	5ms
22nF	10ms
47nF	25ms
100nF	50ms
180nF	100ms
470nF	250ms
1μF	500ms

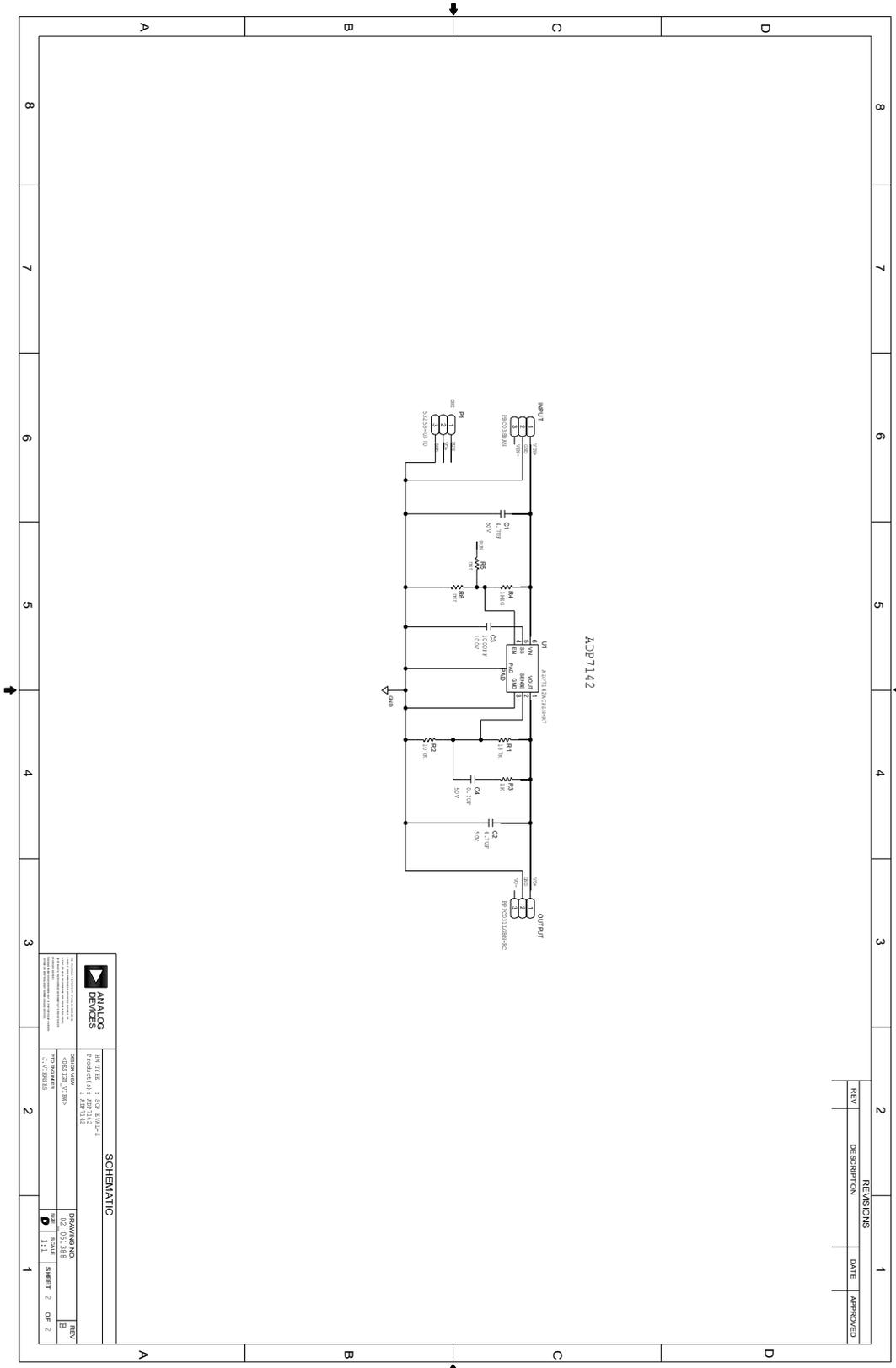
DEMO MANUAL SCP-ADP7142-EVALZ

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	PCB	PCB	ANALOG DEVICES 08_051388b
2	2	C1, C2	CAP 4.7UF 50V CER X7R 1206	SAMSUNG CL31B475KBHNNNE
3	1	C3	CAP 1nF 100V CER X7R 0805	AVX CORPORATION 08051C102KAT2A
4	1	C4	CAP 0.1uF 50V CER X7R 0805	AVX CORPORATION 08055C104JAT2A
5	1	INPUT	CONN-PCB MALE 3POS 2.54MM PITCH R/A	SULLINS PBC03SBAN
6	1	OUTPUT	CONN FEMALE 3POS 2.54MM PITCH R/A	SULLINS PPPC031LGBN-RC
7	1	P1	CONN-PCB 3POS HEADER WIRE TO BRD WAFER ASSY STRAIGHT 2MM PITCH (Note 1)	MOLEX 53253-0370
8	1	R1	RES 187k 1% THICK FILM 0805	PANASONIC ERJ-6ENF1873V
9	1	R2	RES 107k 1% THICK FILM 0805	YAGEO RC0805FR-07107KL
10	1	R3	RES 1.00k 1% THICK FILM 0805	VISHAY CRCW08051K00FKEAHP
11	1	R4	RES 1.00M 1% THICK FILM 0805	YAGEO RC0805JR-071ML
12	2	R5, R6	RES THICK FILM 0805 (Note 1)	N/A
13	1	U1	IC-ADI LOW NOISE, CMOS LDO LINEAR REGULATOR	ANALOG DEVICES ADP7142ACPZN-R7

Note 1. These items are not stuffed (DNI).

SCHEMATIC DIAGRAM



REV	DESCRIPTION	DATE	APPROVED

ANALOG DEVICES		SCHEMATIC	
REV	1	DRAWING NO.	15
DATE	11/11	SHEET 2	OF 2
DESIGNED BY	J. VITENBERG	PROPOSED BY	J. VITENBERG
DESIGNED BY	J. VITENBERG	PROPOSED BY	J. VITENBERG
DESIGNED BY	J. VITENBERG	PROPOSED BY	J. VITENBERG

DEMO MANUAL SCP-ADP7142-EVALZ



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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