40 GHz to 80 GHz, GaAs, pHEMT, MMIC, Wideband Power Amplifier

Data Sheet **ADPA7004CHIPS**

FEATURES

- **Gain: 18.5 dB typical at 45 GHz to 75 GHz**
- **Input return loss: 20.0 dB typical at 45 GHz to 75 GHz**
- **Output return loss: 22.0 dB typical at 45 GHz to 75 GHz**
- **Output P1dB: 22.0 dBm typical at 45 GHz to 75 GHz**
- **P_{SAT}: 24.0 dBm typical at 45 GHz to 75 GHz**
- **Output IP3: 31.0 dBm typical at 45 GHz to 75 GHz**
- **Supply voltage: 3.5 V at 550 mA**
- **50 Ω matched input and output**
- **Die size: 2.940 mm × 3.320 mm × 0.05 mm**

APPLICATIONS

- **Test instrumentation**
- **Military and space**
- **Telecommunications infrastructure**

FUNCTIONAL BLOCK DIAGRAM

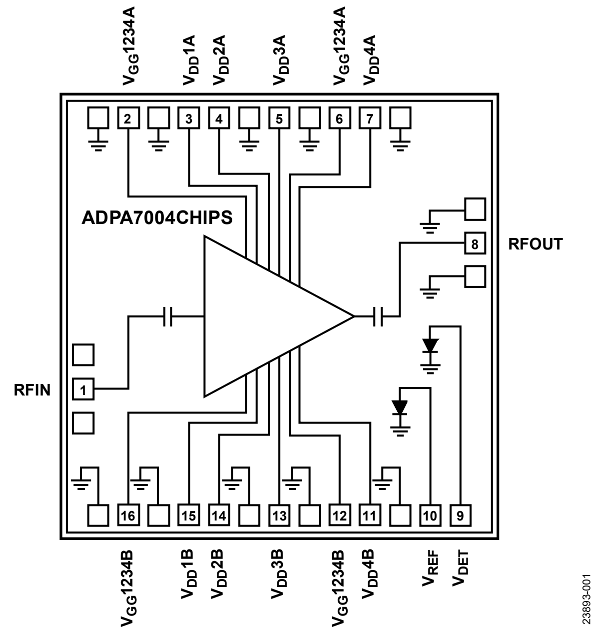

Figure 1.

GENERAL DESCRIPTION

The ADPA7004CHIPS is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), balanced medium power amplifier, with an integrated temperature compensated on-chip power detector that operates from 40 GHz to 80 GHz. In the lower band of 40 GHz to 45 GHz, the ADPA7004CHIPS provides a gain of 17 dB typical, an output third-order intercept (IP3) of 30.5 dBm, and output power for 1 dB gain compression (P1dB) of 21.5 dBm. In the upper band of 75 GHz to 80 GHz, the ADPA7004CHIPS provides a gain of 16 dB (typical), an output IP3 of 31.5 dBm, and an output P1dB of 20.5 dBm. The ADPA7004CHIPS requires 550 mA from a 3.5 V supply. The ADPA7004CHIPS amplifier input and output are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the RFIN and RFOUT pads connected via one 0.076 mm (3 mil) ribbon bond of 0.076 mm (3 mil) minimal length.

Rev. 0 Document Feedback

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REVISION HISTORY

1/2021—Revision 0: Initial Version

SPECIFICATIONS

40 GHz TO 45 GHz FREQUENCY RANGE

Die bottom temperature ($T_{DIE\ BOTTOM}$) = 25°C, drain bias voltage (V_{DD}) = V_{DD}1A and V_{DD}1B = V_{DD}2A and V_{DD}2B = V_{DD}3A and V_{DD}3B = V_{DD}4A and V_{DD}4B = 3.5 V, and I_{DQ}1x + I_{DQ}2x+ I_{DQ}3x + I_{DQ}4x = 550 mA, unless otherwise noted. Note that I_{DQ}1x, I_{DQ}2x, I_{DQ}3x, and I_{DQ}4x are the I_{DQ} for V_{DD}1x, V_{DD}2x, V_{DD}3x, V_{DD}4x, respectively, where x stands for A and B. Adjust V_{GG}1234A from −1.5 V to 0 V to achieve the desired supply current (I_{DQ}). The typical gate bias voltage (V_{GG}) = −0.4 V for I_{DQ} = 550 mA.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		40		45	GHz	
GAIN			17		dB	
Gain Variation over Temperature			0.023		dB/°C	
RETURN LOSS						
Input	S11		18		dB	
Output	S22		23		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		21.5		dBm	
Saturated Output Power	P_{SAT}		23.5		dBm	
Output Third-Order Intercept	IP3		30.5		dBm	Output power (P_{OUT}) per tone = 12 dBm with 1 MHz tone spacing
SUPPLY						
Current	I_{DQ}		550		mA	Adjust V_{GG} to achieve I_{DQ} = 550 mA typical
Voltage	V_{DD}	3	3.5	4	V	

45 GHz TO 75 GHz FREQUENCY RANGE

$T_{DIE\ BOTTOM}$ = 25°C, V_{DD} = V_{DD}1A and V_{DD}1B = V_{DD}2A and V_{DD}2B = V_{DD}3A and V_{DD}3B = V_{DD}4A and V_{DD}4B = 3.5 V and I_{DQ}1x + I_{DQ}2x+ I_{DQ}3x + I_{DQ}4x = 550 mA, unless otherwise noted. Adjust V_{GG}1234A from −1.5 V to 0 V to achieve the desired I_{DQ}. The typical V_{GG} = −0.4 V for I_{DQ} = 550 mA.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		45		75	GHz	
GAIN		15	18.5		dB	
Gain Variation over Temperature			0.023		dB/°C	
RETURN LOSS						
Input	S11		20.0		dB	
Output	S22		22.0		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	20	22.0		dBm	
Saturated Output Power	P_{SAT}		24.0		dBm	
Output Third-Order Intercept	IP3		31.0		dBm	P_{OUT} per tone = 12 dBm with 1 MHz tone spacing
Current	I_{DQ}		550		mA	Adjust V_{GG} to achieve I_{DQ} = 550 mA typical
Voltage	V_{DD}	3	3.5	4	V	

75 GHz TO 80 GHz FREQUENCY RANGE

$T_{DIE\ BOTTOM}$ = 25°C, V_{DD} = V_{DD}1A and V_{DD}1B = V_{DD}2A and V_{DD}2B = V_{DD}3A and V_{DD}3B = V_{DD}4A and V_{DD}4B = 3.5 V, and I_{DQ}1x + I_{DQ}2x+ I_{DQ}3x + I_{DQ}4x = 550 mA, unless otherwise noted. Adjust V_{GG}1234A from −1.5 V to 0 V to achieve the desired I_{DQ}. The typical V_{GG} = −0.4 V for I_{DQ} = 550 mA.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		75		80	GHz	
GAIN		13	16		dB	
Gain Variation over Temperature			0.023		dB/°C	
RETURN LOSS						
Input	S11		25.0		dB	
Output	S22		21.0		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	18	20.5		dBm	
Saturated Output Power	P_{SAT}		22.0		dBm	
Output Third-Order Intercept	IP3		31.5		dBm	P_{OUT} per tone = 12 dBm with 1 MHz tone spacing
SUPPLY						
Current	I_{DQ}		550		mA	Adjust V_{GG} to achieve I_{DQ} = 550 mA typical
Voltage	V_{DD}	3	3.5	4	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	4.5 V
V_{GG}	−2 V dc to 0 V dc
RF Input Power (RFIN)	18 dBm
Continuous Power Dissipation (P_{DISS}), at $T_{DIE\ BOTTOM}$ = 85°C (Derate 33.3 mW/°C Above 85°C)	3.04 W
Temperature	
Storage Range (Ambient)	−65°C to +150°C
Operating Range (Die Bottom)	−55°C to +85°C
Junction Temperature to Maintain 1,000,000 Hours Mean Time to Failure (MTTF)	175
Nominal Junction Temperature (T_J = 85°C, V_{DD} = 3.5 V, I_{DQ} = 550 mA)	142

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to printed circuit board (PCB) thermal design is required.

θ_{JC} is the channel to case thermal resistance, channel to bottom of die attach epoxy.

Table 5.

Package Type	θ_{JC}	Unit
C-16-4	29.6	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

ESD Ratings ADPA7004CHIPS

Table 6. ADPA7004CHIPS, 16-Pad CHIP

ESD Model	Withstand Threshold (V)	Class
HBM	±125	0

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

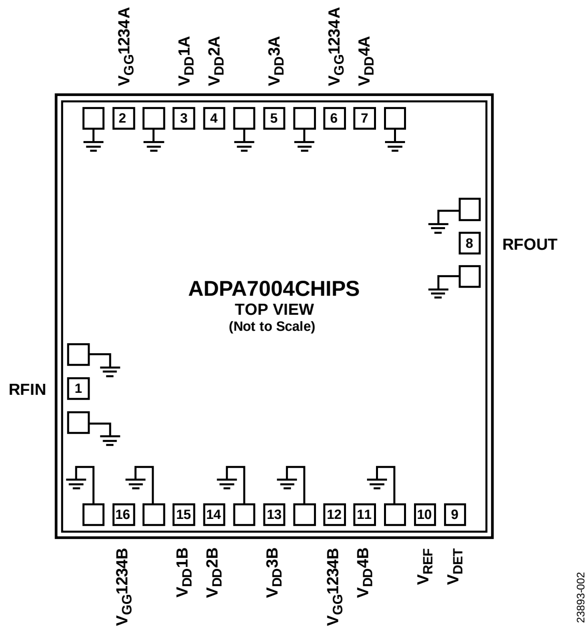

Figure 2. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	RF Input. This pad is ac-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
2, 6	V_{GG}1234A	Gate Bias Voltage Pads for the First, Second, Third, and Fourth Stage Amplifiers. See Figure 4 for the interface schematic.
3, 4, 5, 7	V_{DD}1A, V_{DD}2A, V_{DD}3A, V_{DD}4A	Top Edge Drain Bias Voltage Pads for the Amplifiers. External bypass capacitors are required on the V_{DD}1A, V_{DD}2A, V_{DD}3A, and V_{DD}4A pads. Connect the V_{DD}1A, V_{DD}2A, V_{DD}3A, and V_{DD}4A pads to a 3.5 V supply. See Figure 5 for the interface schematic.
8	RFOUT	RF Output. This pad is ac-coupled and matched to 50 Ω. See Figure 9 for the interface schematic.
9	V_{DET}	DC Voltage Representing the RF Output Power. The voltage is rectified by the diode that is biased through external resistor. See Figure 9 for the interface schematic.
10	V_{REF}	Reference DC Voltage for the Temperature Compensation of the V_{DET} diode. See Figure 10 for the interface schematic.
11, 13, 14, 15	V_{DD}4B, V_{DD}3B, V_{DD}2B, V_{DD}1B	Bottom Edge Drain Bias Voltage Pads for Amplifiers. External bypass capacitors are required on the V_{DD}4B, V_{DD}3B, V_{DD}2B, and V_{DD}1B pads. Connect the V_{DD}4B, V_{DD}3B, V_{DD}2B, and V_{DD}1B pads to a 3.5 V supply. See Figure 7 for the interface schematic.
12, 16	V_{GG}1234B	Gate Bias Voltage Pads for the First, Second, Third, and Fourth Stage Amplifiers, Alternative Bias Configuration. See Figure 8 for the interface schematic.
Die Bottom	GND	Ground. Die bottom must be connected to RF and dc ground. See Figure 6 for the interface schematic.

INTERFACE SCHEMATICS

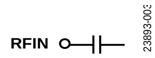

Figure 3. RFIN Interface Schematic

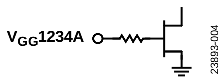

Figure 4. V_{GG}1234A Interface Schematic

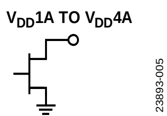

Figure 5. V_{DD}1A to V_{DD}4A Interface Schematic

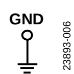

Figure 6. GND Interface Schematic

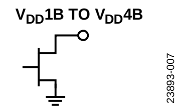

Figure 7. V_{DD}1B to V_{DD}4B Interface Schematic

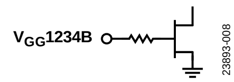

Figure 8. V_{GG}1234B Interface Schematic

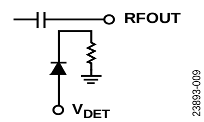

Figure 9. RFOUT and V_{DET} Interface Schematic

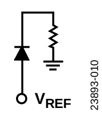

Figure 10. V_{REF} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

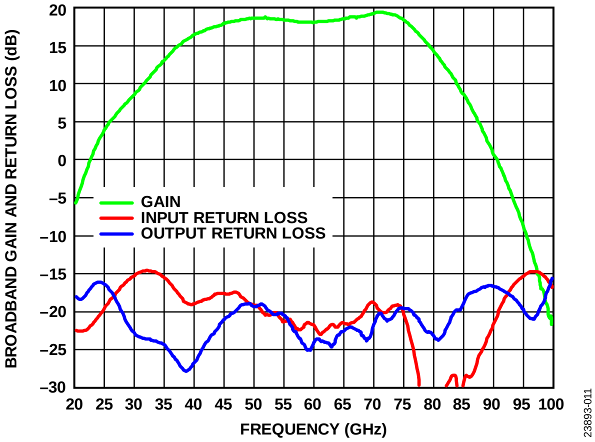

Figure 11. Broadband Gain and Return Loss vs. Frequency

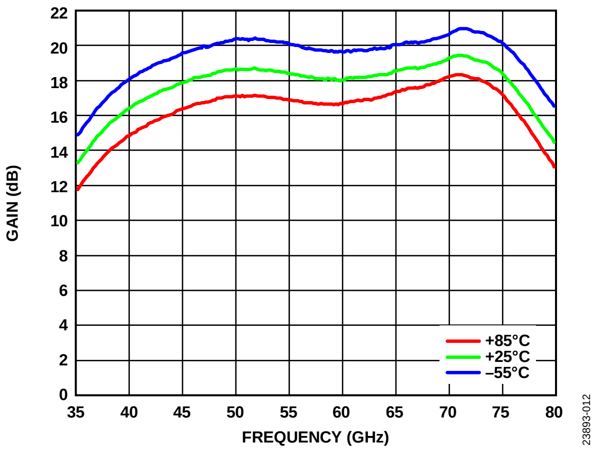

Figure 12. Gain vs. Frequency at Various Temperatures

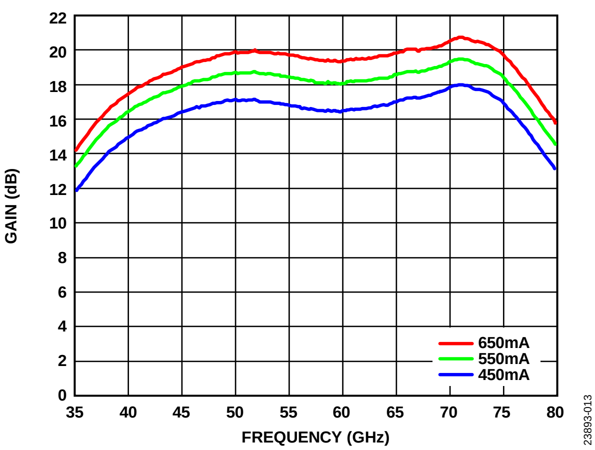

Figure 13. Gain vs. Frequency at Various Supply Currents

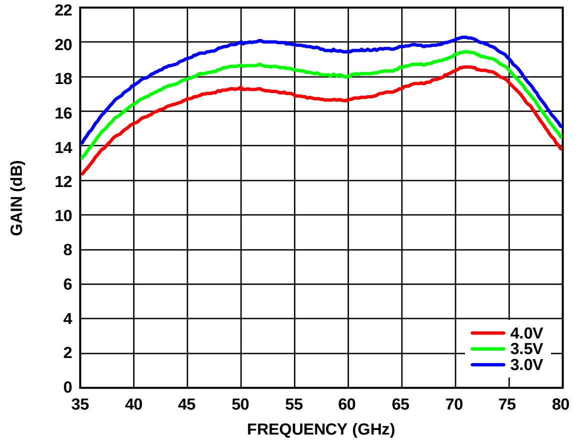

Figure 14. Gain vs. Frequency at Various Drain Bias Voltages

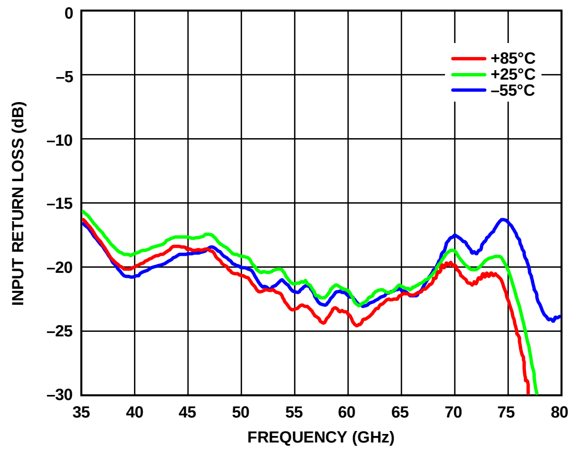

Figure 15. Input Return Loss vs. Frequency at Various Temperatures

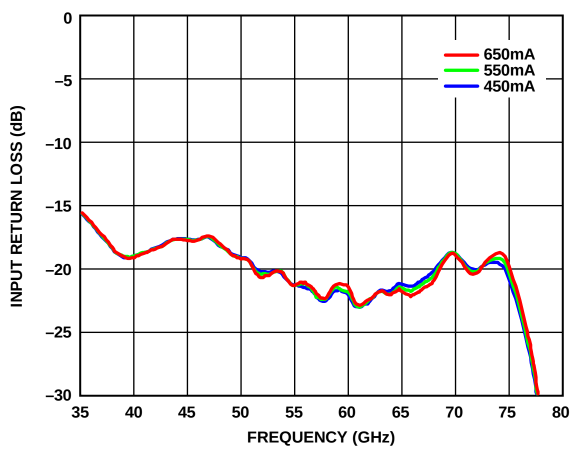

Figure 16. Input Return Loss vs. Frequency at Various Supply Currents

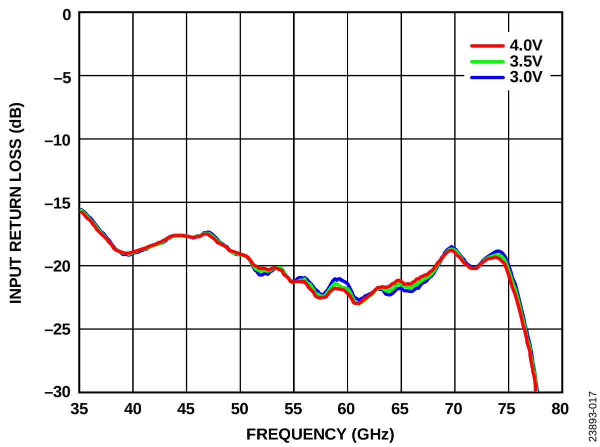

Figure 17. Input Return Loss vs. Frequency at Various Drain Bias Voltages

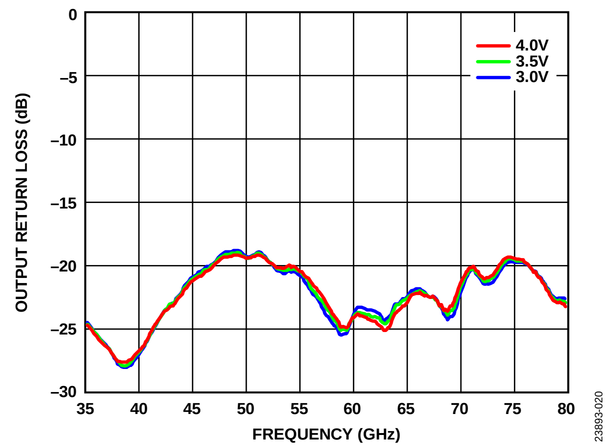

Figure 20. Output Return Loss vs. Frequency at Various Drain Bias Voltages

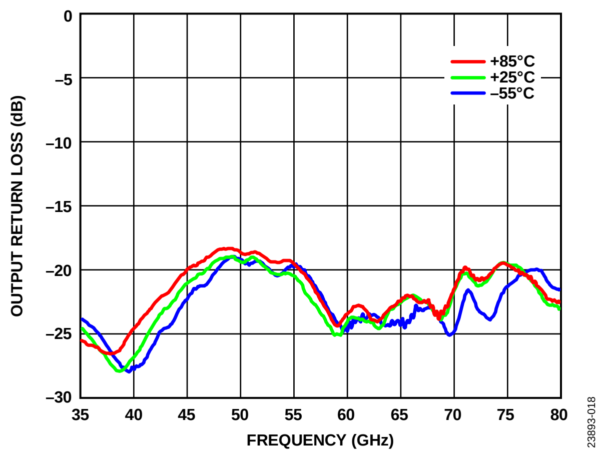

Figure 18. Output Return Loss vs. Frequency at Various Temperatures

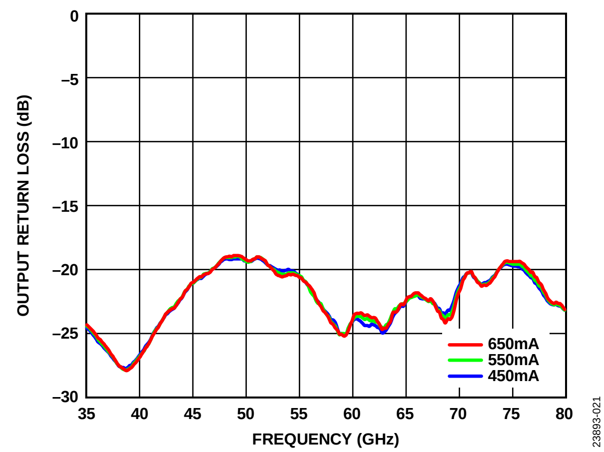

Figure 21. Output Return Loss vs. Frequency at Various Supply Currents

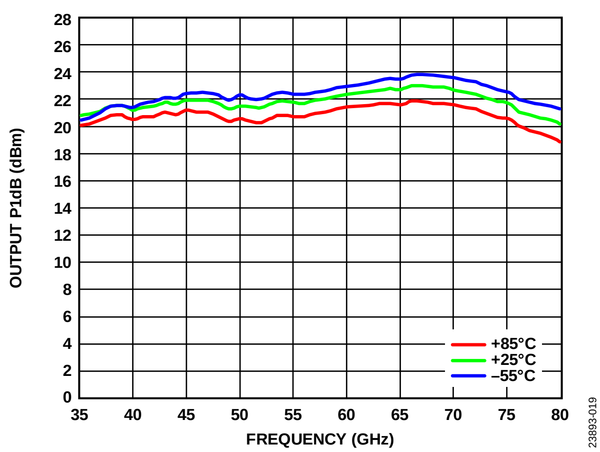

Figure 19. Output P1dB vs. Frequency at Various Temperatures

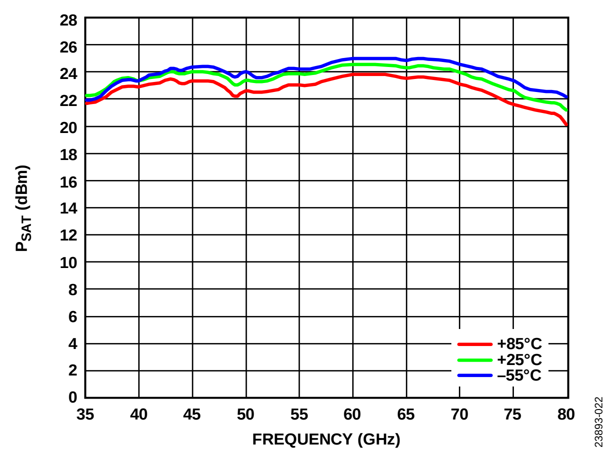

Figure 22. P_{SAT} vs. Frequency at Various Temperatures

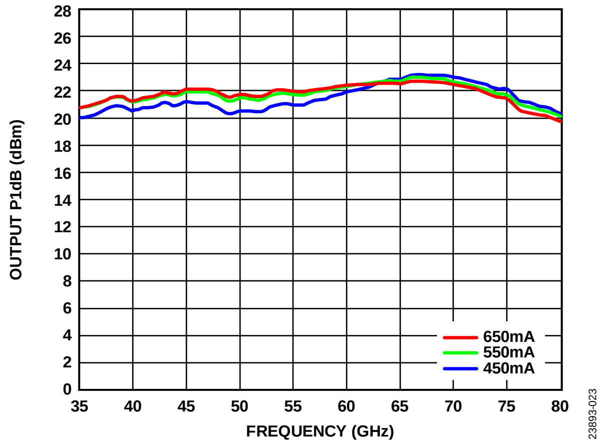

Figure 23. Output P1dB vs. Frequency at Various Supply Currents

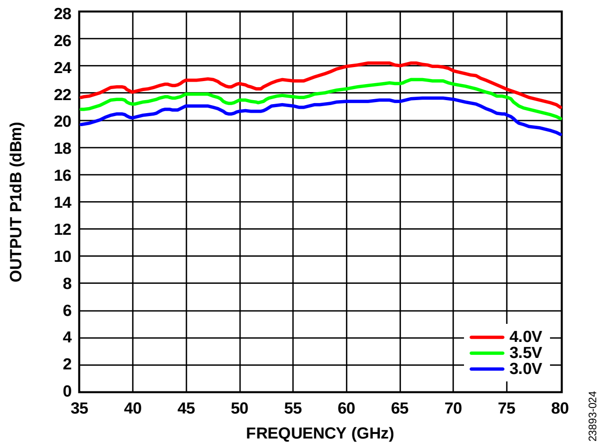

Figure 24. Output P1dB vs. Frequency at Various Drain Bias Voltages

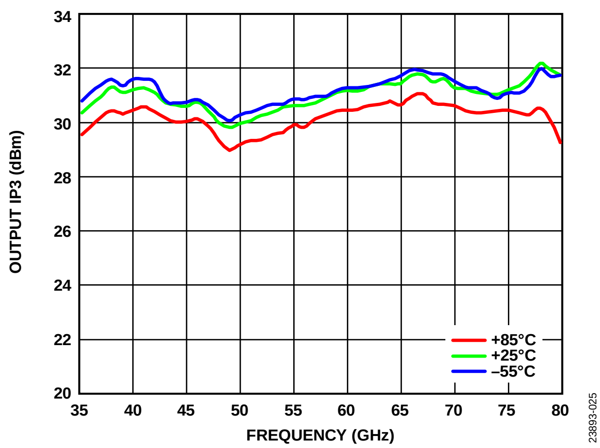

Figure 25. Output IP3 vs. Frequency at Various Temperatures

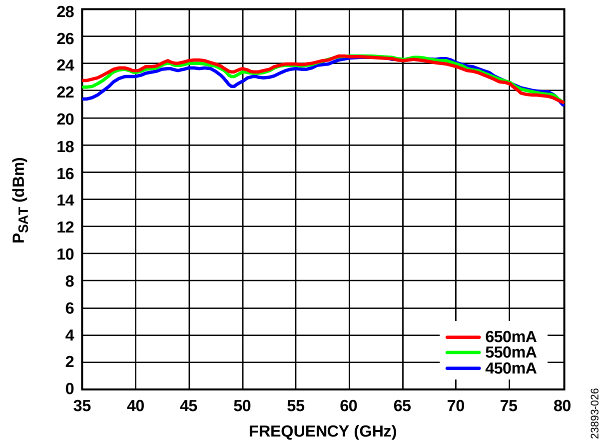

Figure 26. P_{SAT} vs. Frequency at Various Supply Currents

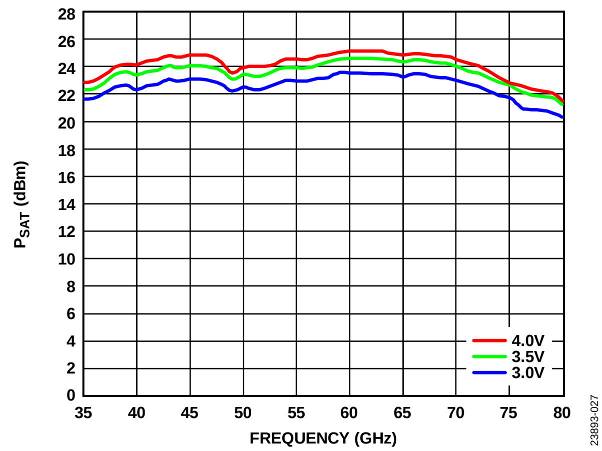

Figure 27. P_{SAT} vs. Frequency at Various Drain Bias Voltages

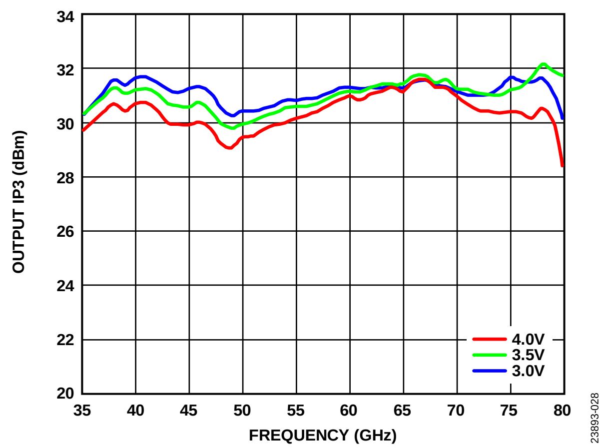

Figure 28. Output IP3 vs. Frequency at Various Drain Bias Voltages

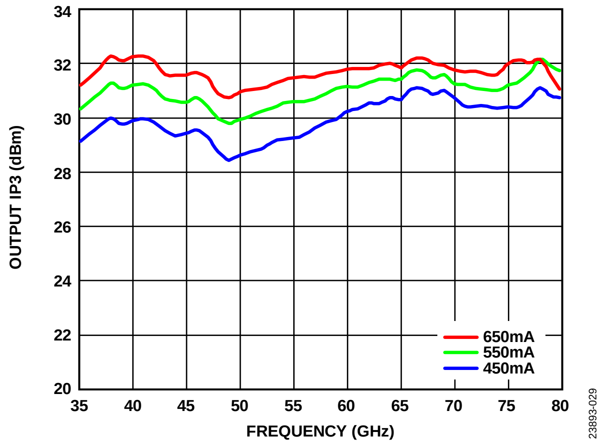

Figure 29. Output IP3 vs. Frequency at Various Supply Currents

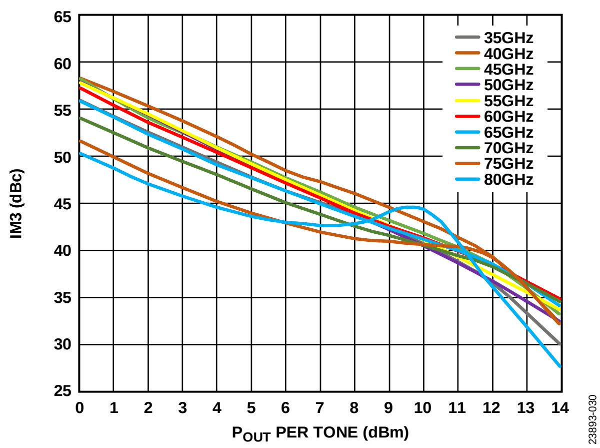

Figure 30. Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone at Various Frequencies at V_{DD} = 3 V, I_{DQ} = 550 mA

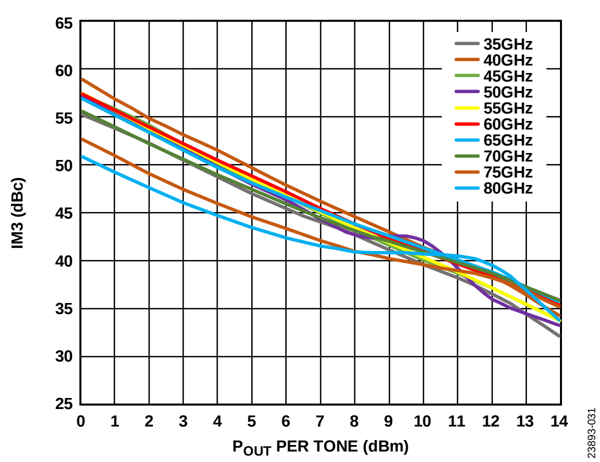

Figure 31. IM3 vs. P_{OUT} per Tone at Various Frequencies at V_{DD} = 3.5 V, I_{DQ} = 550 mA

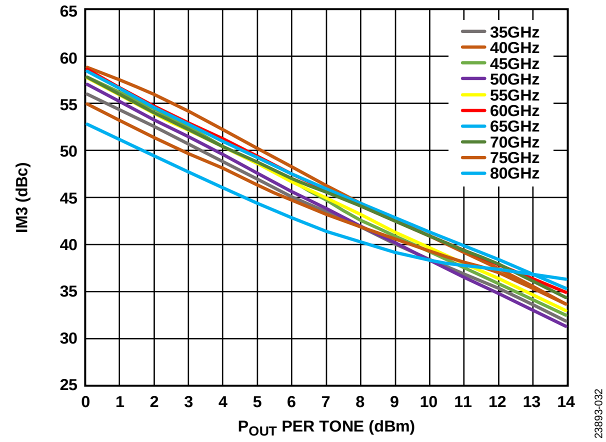

Figure 32. IM3 vs. P_{OUT} per Tone at Various Frequencies at V_{DD} = 4 V, I_{DQ} = 550 mA

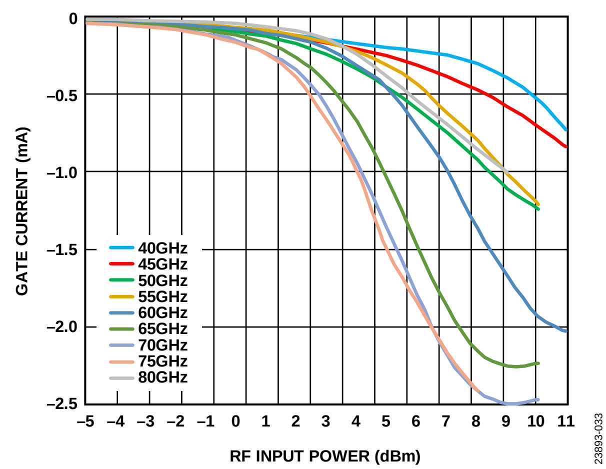

Figure 33. Gate Current vs. RF Input Power at Various Frequencies

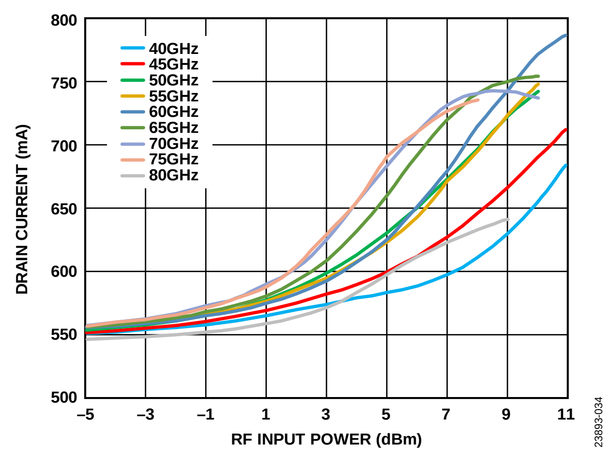

Figure 34. Drain Current vs. RF Input Power at Various Frequencies

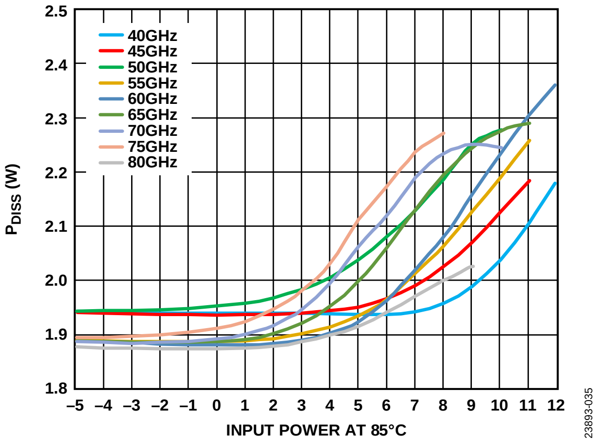

Figure 35. P_{DISS} vs. Input Power at 85°C at Various Frequencies, V_{DD} = 3.5 V, I_{DQ} = 550 mA

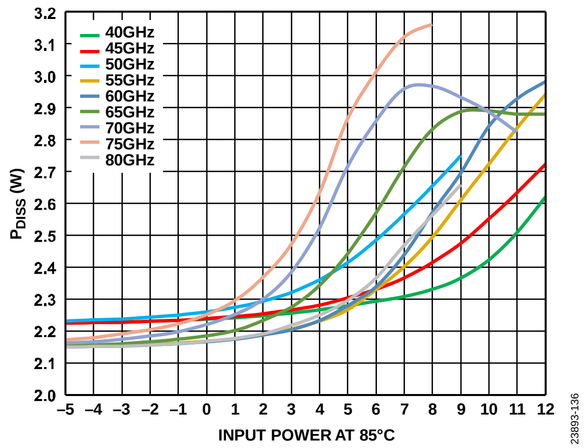

Figure 36. P_{DISS} vs. Input Power at 85°C at Various Frequencies, V_{DD} = 4 V, I_{DQ} = 550 mA

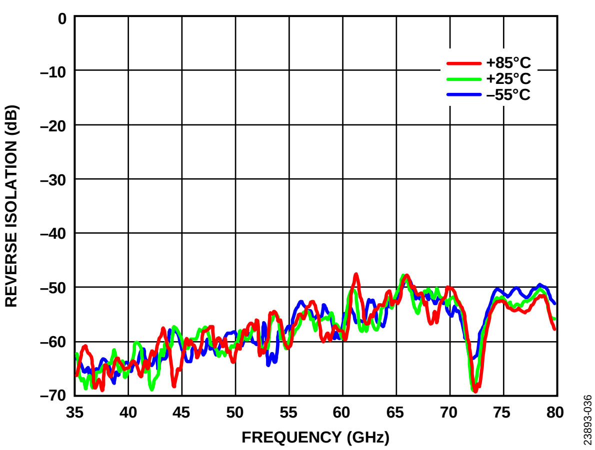

Figure 37. Reverse Isolation vs. Frequency at Various Temperatures

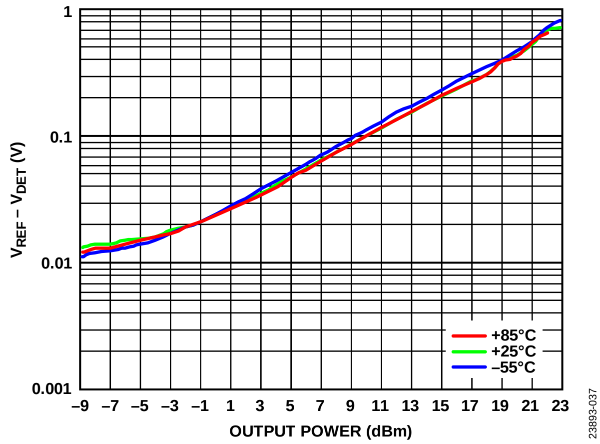

Figure 38. Detector Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures at 40 GHz

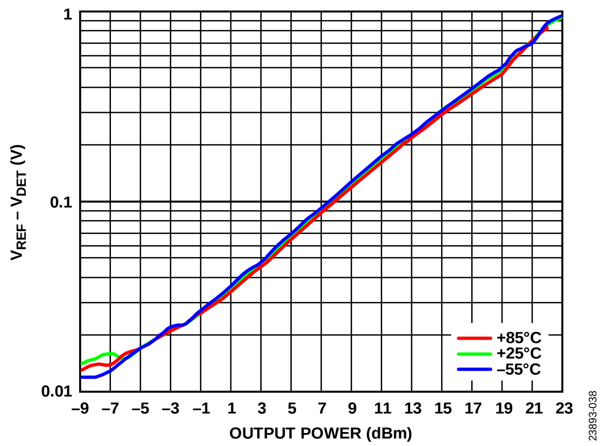

Figure 39. V_{REF} – V_{DET} vs. Output Power at Various Temperatures at 50 GHz

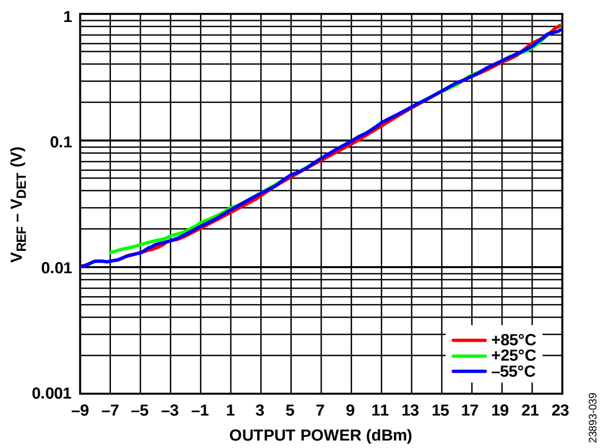

Figure 40. V_{REF} – V_{DET} vs. Output Power at Various Temperatures at 60 GHz

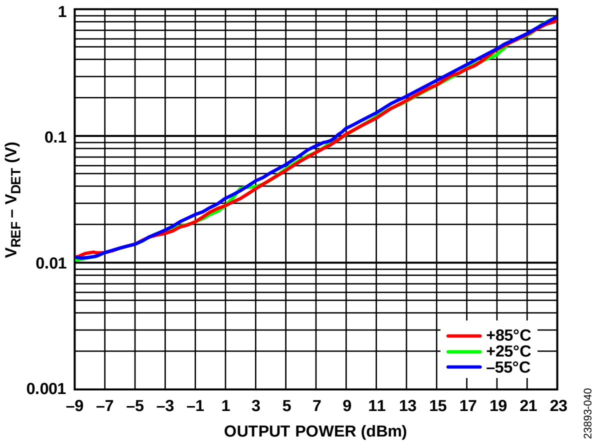

Figure 41. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures at 70 GHz

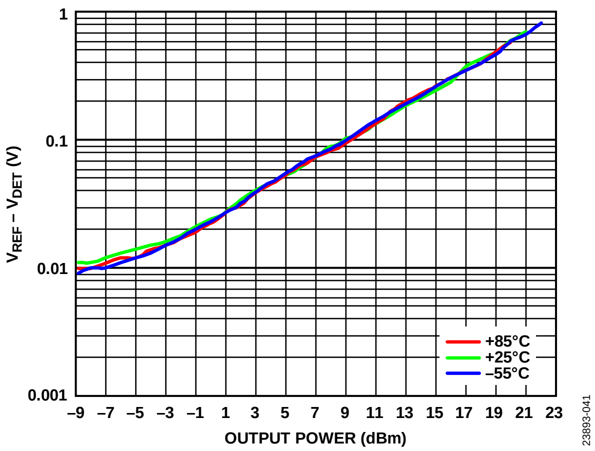

Figure 42. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures at 80 GHz

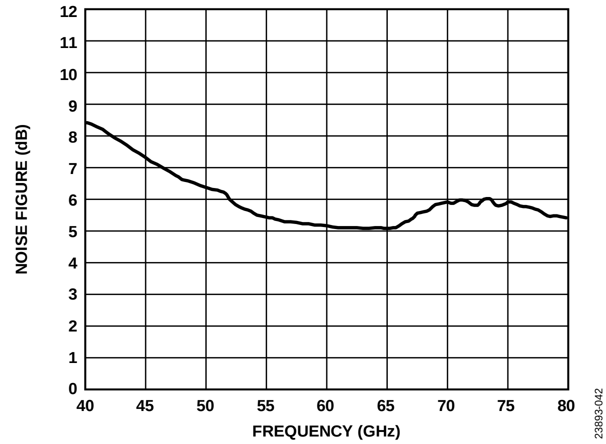

Figure 43. Noise Figure vs. Frequency at 25°C

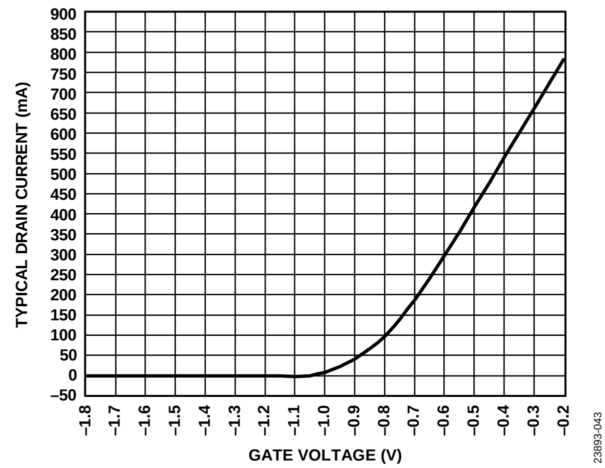

Figure 44. Typical Drain Current vs. Gate Voltage at 25°C

THEORY OF OPERATION

Figure 45 shows a simplified block diagram of ADPA7004CHIPS. The ADPA7004CHIPS consists of two cascaded, four-stage amplifiers, operating in quadrature between two 90° hybrids. This balanced approach forms an amplifier with a combined gain of 17 dB and a P_{SAT} of 23.5 dBm. The 90° hybrids ensure that the input and output return losses are excellent.

All gate bias voltages pads (V_{GG}1234x) are internally connected together. The drain bias pads (V_{DD}xA through V_{DD}xB) are internally connected together in four pairs of two with each pair providing bias current for one amplifier stage. In the case of the gate bias, the gate bias voltage can be applied to a single pad. However, in the case of the eight V_{DD}xA and V_{DD}xB drain bias pad connections, all eight pads must be used to minimize voltage drops. See Figure 46 and Figure 47 for further details on biasing the various blocks.

A portion of the RF output signal (RFOUT) is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes this power available for measurement as a dc voltage at V_{DET}. To allow temperature compensation of V_{DET}, the reference dc voltage detected through an identical diode that is not coupled to the RF power is available on the V_{REF} pad. The difference of V_{REF} − V_{DET} provides a temperature compensated detector voltage that is proportional to the RF output power (see Figure 38 to Figure 42).

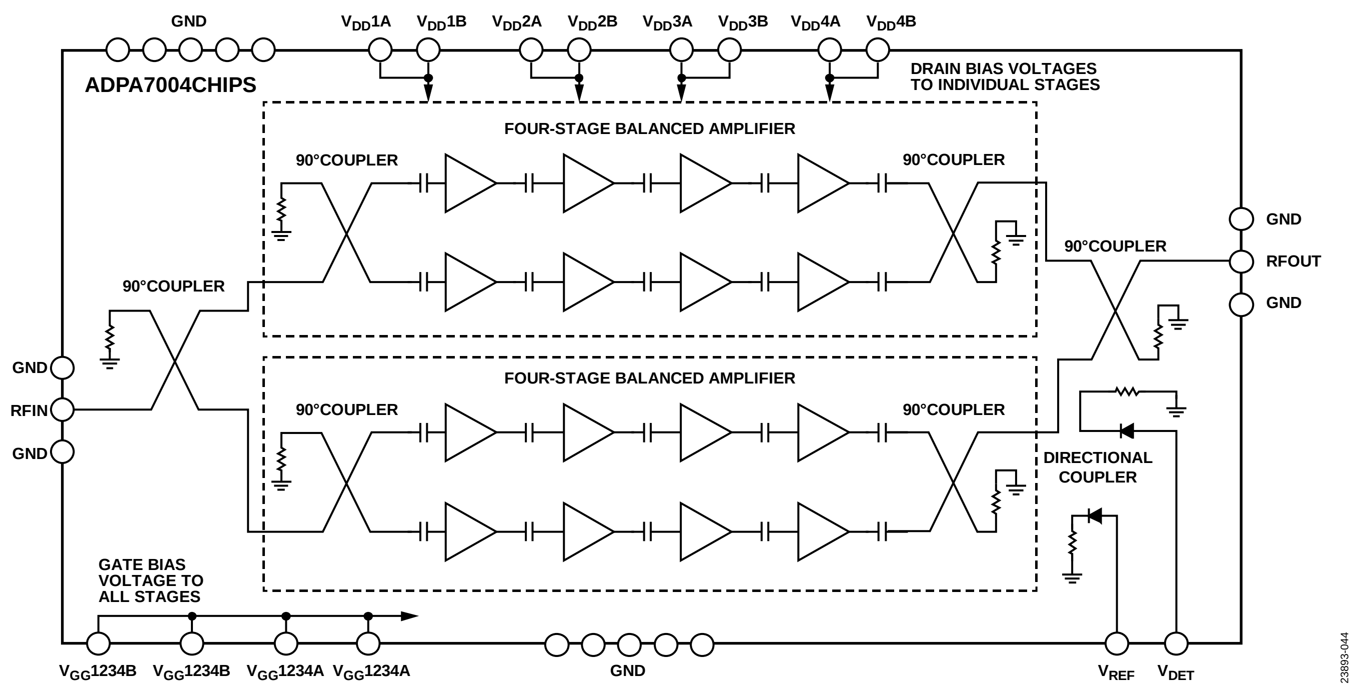

Figure 45. Simplified Block Diagram

APPLICATIONS INFORMATION

Basic connections for operating the ADPA7004CHIPS are shown in Figure 46 and Figure 47. There are eight V_{DD}xA and V_{DD}xB drain bias pads. To minimize voltage drops in bond wires and on die traces, all eight pads (V_{DD}xA through V_{DD}xB) must be used. Each V_{DD}xA and V_{DD}xB line has a 100 pF decoupling capacitor with adjacent pads sharing larger decoupling capacitors. The power supply decoupling capacitors shown in Figure 46 represent the configuration that was used to characterize and qualify the device. It may be possible to reduce the number of capacitors, but the scope varies from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the device.

All four gate bias voltages pads (V_{GG}1234x) are internally connected. In contrast to the V_{DD}xA through V_{DD}xB drain bias lines, the gate bias voltage can be applied through a single pad on either the north or the south side of the die. Figure 46 shows the gate bias voltage applied through the V_{GG}1234B pins on the south side of the die, and Figure 47 shows the gate bias voltage applied to the V_{GG}1234A pins on the north side of the die. In both cases, a single 100 pF capacitor must be connected to one of the gate bias pads on the unused side.

POWER-UP AND POWER-DOWN SEQUENCING

To prevent damage to the ADPA7004CHIPS, follow the power-up and power-down sequences.

Power-Up Sequence

Take the following steps to power up the device:

1. Connect all grounds.
2. Set the gate bias voltages (V_{GG}1234x) to −1.5 V.
3. Set the drain bias voltages (V_{DD}xA through V_{DD}xB) to 3.5 V.
4. Increase the gate bias voltages (V_{DD}xA through V_{DD}xB) to achieve I_{DQ} = 550 mA.
5. Apply the RF signal.

Power-Down Sequence

Take the following steps to power down the device:

1. Turn off the RF signal.
2. Decrease the gate bias voltages (V_{GG}1234x) to −1.5 V to reduce I_{DQ} to approximately 0 mA.
3. Reduce the drain bias voltages (V_{DD}xA through V_{DD}xB) to 0 V.
4. Increase the gate bias voltages (V_{GG}1234x) to 0 V.

The V_{DD} = 3.5 V and I_{DQ} = 550 mA bias conditions are recommended to optimize overall performance. Table 8 summarizes the performance at 60 GHz at other drain current settings along with the dc quiescent power consumption (dc power consumption increases with RF applied). In this case, higher drain current slightly increases output IP3 but has minimal impact on output P1dB.

RF DETECTOR OPERATION

To achieve a temperature stable RF detector output voltage (V_{OUT}), subtract the voltage on the V_{DET} pad from the voltage on the V_{REF} pad, which can be done by using the differential op-amp circuit shown in Figure 46 and Figure 47.

Table 8. DC Power Consumption Selection Table[1, 2]

I_{DQ} (mA)	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W)	V_{GG} (V)
450	16.4	22	30.1	1.6	−0.5
550	18	22.2	31.0	1.9	−0.4
650	19.5	22.2	31.9	2.3	−0.3

[1] Data taken at the following nominal bias conditions: V_{DD} = 3.5 V, T_A = 25°C, and frequency = 60 GHz.
[2] Adjust V_{GG}1234x between −1.5 V and 0 V to achieve the desired I_{DQ}.

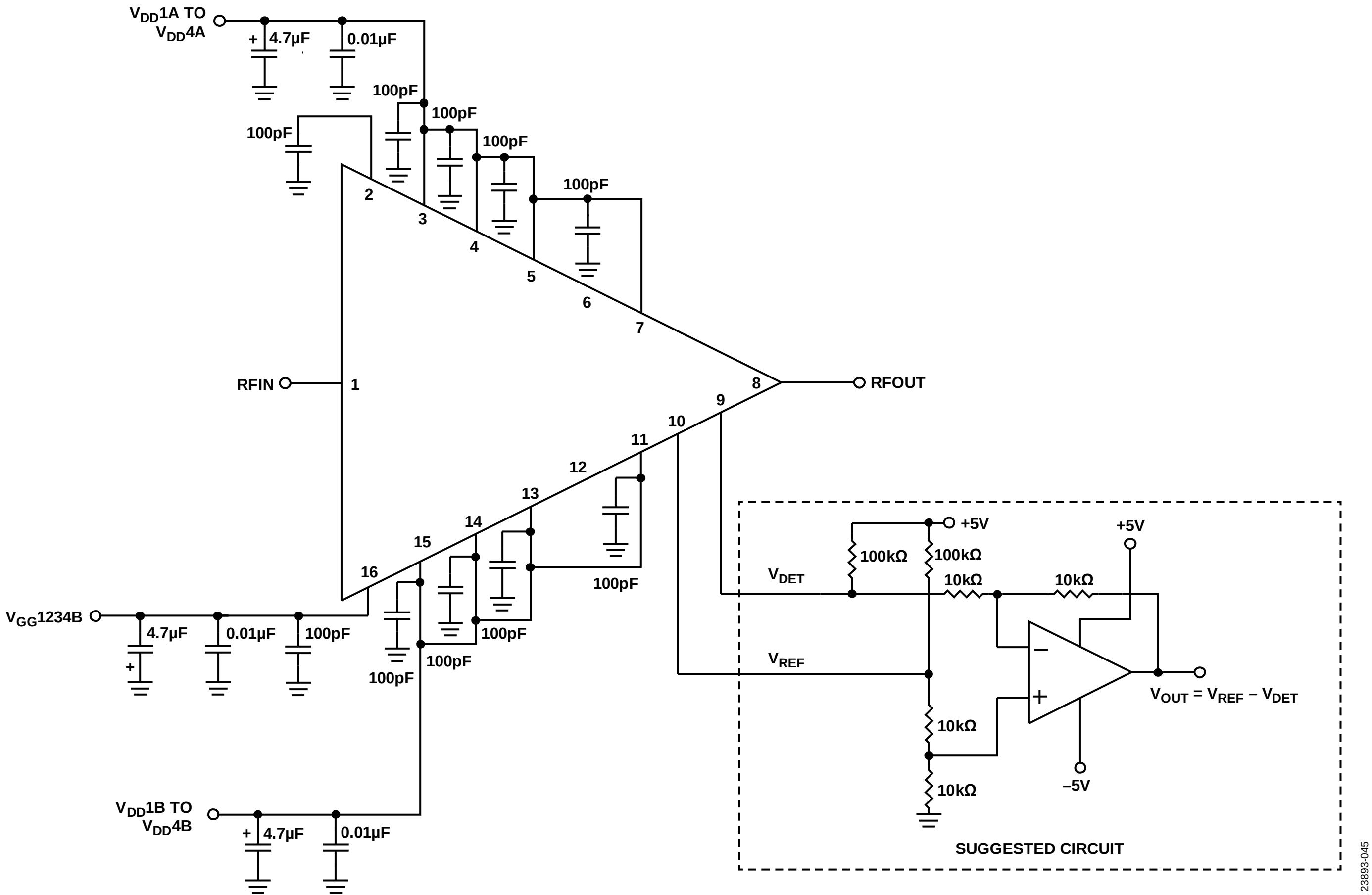

Figure 46. Basic Connections for Operation with Gate Bias Control on South Side of Die

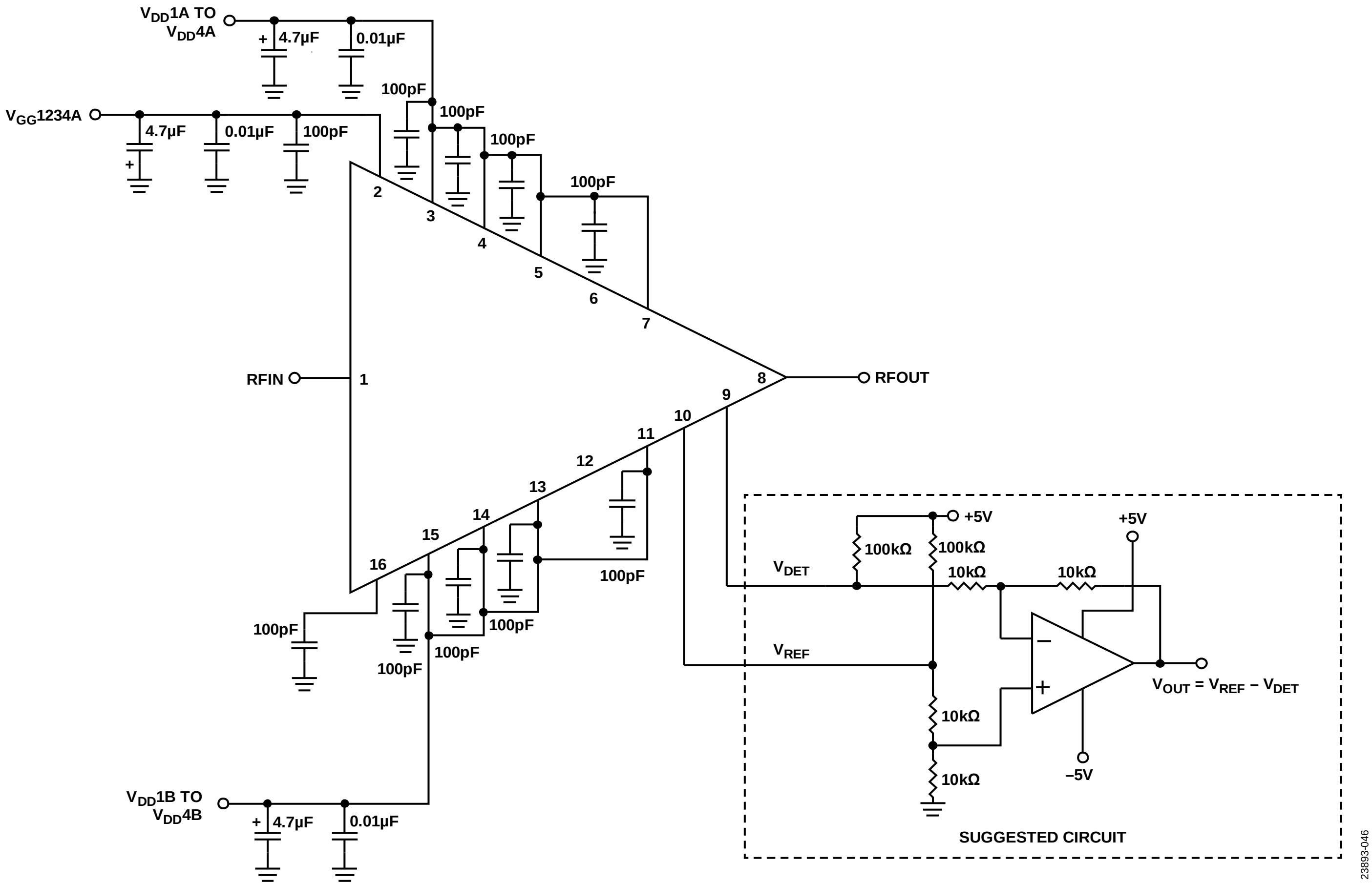

Figure 47. Basic Connections for Operation with Gate Bias Control on North Side of Die

ASSEMBLY DIAGRAM

Figure 48 shows the recommended assembly diagram for ADPA7004CHIPS.

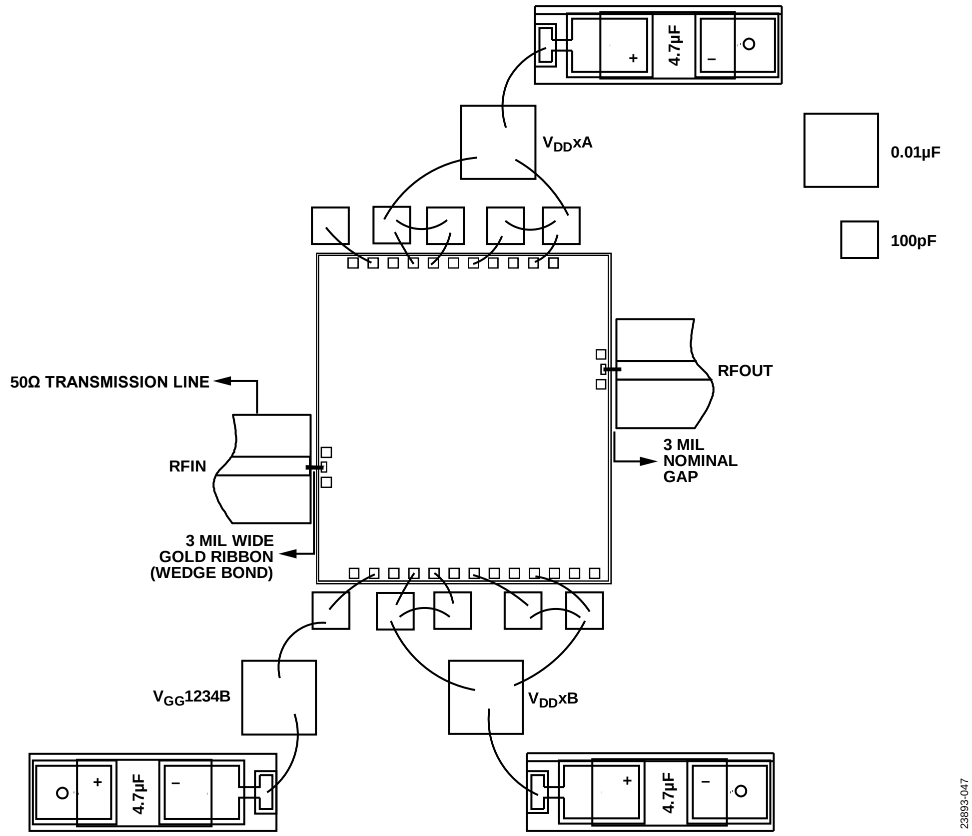

Figure 48. Assembly Diagram with Gate Bias Control on South Side of Die

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane with high thermal conductivity epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω transmission lines on 0.127 mm (5 mil) thick alumina, thin film substrates are recommended for bringing the RF to and from the chip. Raise the die 0.076 mm (3 mil) to ensure that the surface of the die is coplanar with the surface of the substrate.

Place microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm (3 mil). To ensure wideband matching, a 15 fF capacitive stub is recommended on the transmission line before the ribbon bond.

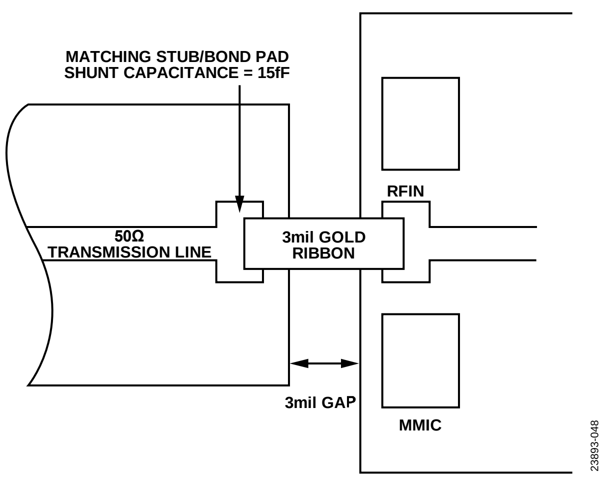

Figure 49. High Frequency Input Matching

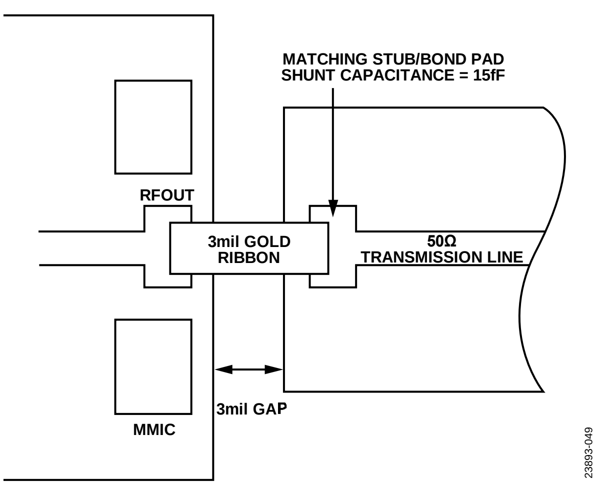

Figure 50. High Frequency Output Matching

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle-based or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chip in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

Before epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with 0.003 in. × 0.0005 in. gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 0.001 in. (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

Alternatively, short (≤3 mil) RF bonds made with two 1 mil wires can be used.

OUTLINE DIMENSIONS

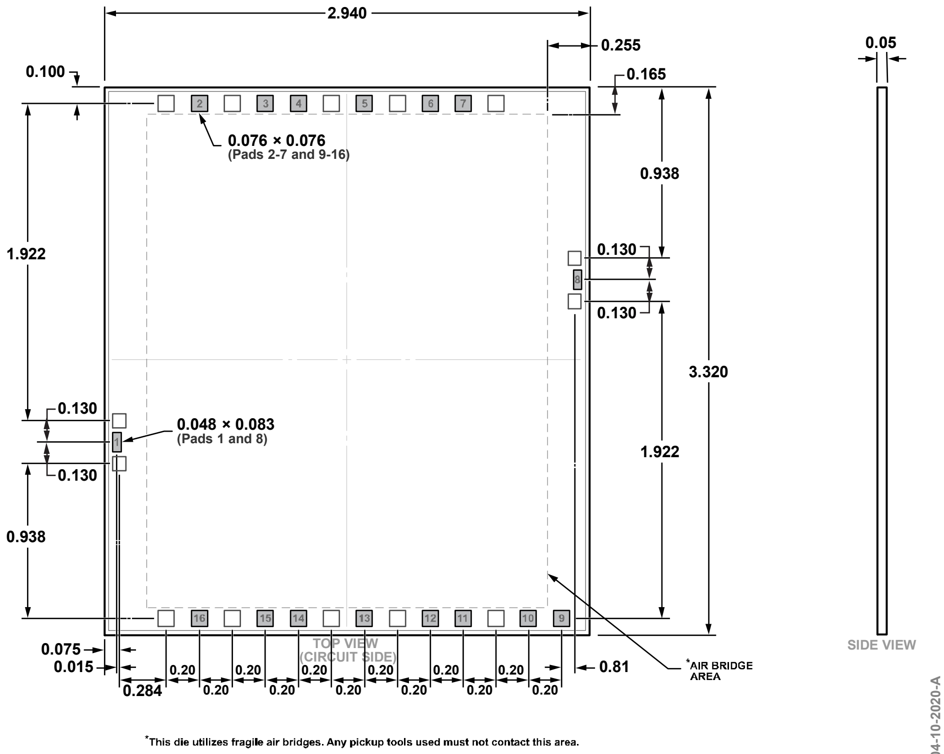

Figure 51. 16-Pad Bare Die [CHIP]
(C-16-4)
Dimensions shown in millimeter

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADPA7004CHIPS	−55°C to +85°C	16-Pad Bare Die [CHIP]	C-16-4
ADPA7004CHIP-SX	−55°C to +85°C	16-Pad Bare Die [CHIP]	C-16-4

[1] ADPA7004CHIPS and ADPA7004CHIP-SX are RoHS compliant parts.

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