

# ADRF5019-EVALZ User Guide

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### **Evaluating the ADRF5019 Silicon SPDT Switch, Nonreflective, 100 MHz to 13 GHz**

#### **FEATURES**

Contains ADRF5019 device and external components RF SMA connectors
Through line for calibration

#### **EQUIPMENT NEEDED**

DC power supplies Network analyzer

#### **GENERAL DESCRIPTION**

The ADRF5019-EVALZ (see Figure 1) is designed to evaluate the features and performance of the ADRF5019 100 MHz to 13 GHz, single-pole double throw (SPDT) switch manufactured in a silicon process.

For full details on the ADRF5019, see the ADRF5019 data sheet, which must be consulted in conjunction with this user guide when using the ADRF5019-EVALZ.

#### **EVALUATION BOARD PHOTOGRAPH**

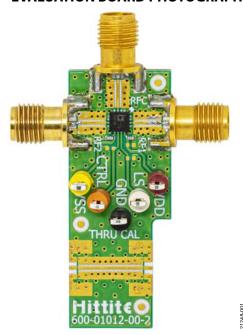


Figure 1.

# UG-1616

# ADRF5019-EVALZ User Guide

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#### **REVISION HISTORY**

8/2019—Revision 0: Initial Version

# **EVALUATION BOARD HARDWARE** OVERVIEW

The ADRF5019-EVALZ is a connectorized evaluation board assembled with the ADRF5019 device and the ADRF5019 application circuitry. All components are located on the primary side of the ADRF5019-EVALZ (see Figure 2).

#### **BOARD LAYOUT**

Figure 2 shows the topside ADRF5019-EVALZ layout and component placement locations.

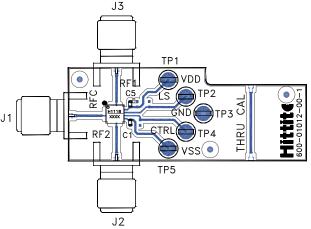


Figure 2. ADRF5019-EVALZ Layout

#### **RF INPUTS AND OUTPUTS**

The RF input and output ports (RFC, RF1, and RF2) are connected through 50  $\Omega$  transmission lines to the Subminiature Version A (SMA) launchers (J1, J3, and J2, respectively).

The through calibration line, THRU CAL, calibrates out the board loss effects from the ADRF5019-EVALZ measurements to determine the device performance at the pins of the IC. Figure 3 shows the typical board loss for the ADRF5019-EVALZ at room temperature, as well as the embedded and de-embedded insertion loss for the ADRF5019.

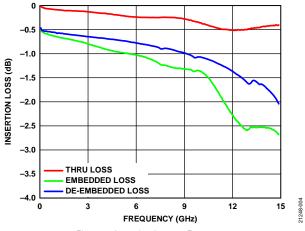


Figure 3. Insertion Loss vs. Frequency

#### **POWER SUPPLY AND CONTROL INPUTS**

Two power supply ports are connected to the VDD and VSS test points on the ADRF5019-EVALZ, and the ground reference is connected to the GND test point. On the VDD and VSS supply traces, a 100 pF bypass capacitor filters high frequency noise. Unpopulated component positions are available for applying extra bypass capacitors.

Two control ports are connected to the CTRL and LS test points. There are provisions for the RC filter to eliminate dc-coupled noise, if needed by the application.

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### **USING THE ADRF5019-EVALZ**

The ADRF5019-EVALZ is shipped assembled and tested. Figure 4 provides a basic test setup diagram to measure the scattering parameter response of the ADRF5019. To complete the test setup and verify the operation of the ADRF519-EVALZ, take the following steps:

- 1. Connect the GND test point to the ground terminal of the power supply.
- 2. Connect the VDD, VSS, LS, and CTRL test points to the voltage output terminal of the power supplies. See Table 2 for the power supply connections.
- 3. Connect the RFC, RF1, and RF2 ports to a calibrated network analyzer.
- 4. Turn on the VDD and VSS power supplies connected to the ADRF5019-EVALZ. See Table 2 for nominal bias conditions.
- Turn on the LS and CTRL power supplies. Use LS and CTRL to control the state of the switch. See Table 1 for the control voltage truth table.
- 6. Measure the scattering parameters.

**Table 1. Control Voltage Truth Table** 

Digital Control Inputs		RF Paths		
LS	CTRL	RF1 to RFC	RF2 to RFC	
High	Low	Insertion loss (on)	Isolation (off)	
High	High	Isolation (off)	Insertion loss (on)	
Low	Low	Isolation (off)	Insertion loss (on)	
Low	High	Insertion loss (on)	Isolation (off)	

**Table 2. Power Supply and Control Inputs** 

Test Points Description		Nominal Voltage	Nominal Current	
TP1	VDD	3.3 V	20 μΑ	
TP2	LS	0 V or 3.3 V	<1 µA	
TP3	GND	Ground	Not applicable	
TP4	CTRL	0 V or 3.3 V	< 1 μΑ	
TP5	VSS	−2.5 V	0.5 μΑ	

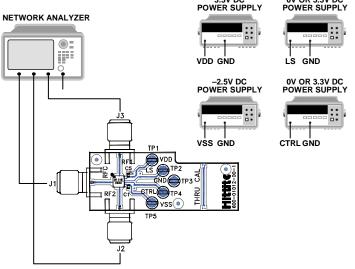


Figure 4. Scattering Parameter Test Setup Diagram

## **EVALUATION BOARD SCHEMATIC**

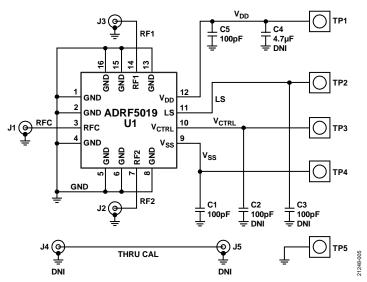


Figure 5. ADRF5019-EVALZ Schematic

### ORDERING INFORMATION

#### **BILL OF MATERIALS**

Table 3. Bill of Materials for ADRF5019-EVALZ

Qty	Reference Designator	Description	Manufacturer	Part Number
3	J1 to J3	PC mount, SMA, RF connectors	SRI Connector Gage Co.	21-146-1000-01
2	J4, J5	PC mount, SMA, RF connectors (do not insert)	SRI Connector Gage Co.	21-146-1000-01
5	TP1 to TP5	Through hole, hold mount test points	Keystone Electronics	5006
2	C1, C5	Capacitors, 100 pF, 50 V, 0402 package	Kemet	C0402C101J5GACTU
3	C2 to C4	Capacitors, 100 pF, 50 V, 0402 package (do not insert)	Kemet	C0402C101J5GACTU
1	U1	SPDT switch	Analog Devices	ADRF5019
1	PCB	600-01012-00-1 evaluation printed circuit board (PCB)	Analog Devices	600-01012-00-1



#### FSD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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