ANALOG DEVICES

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APPLICATION NOTE

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# Single Positive Supply Operation for the HMC1118

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## INTRODUCTION

The HMC1118 is a silicon single-pole, double throw (SPDT) switch specified from 9 kHz to 13 GHz in a 4 mm × 4 mm, 16-lead lead frame chip scale package (LFCSP). This broadband switch is well suited for test and measurement equipment and high performance wireless applications. Key features include the following:

- Low insertion loss: 0.68 dB at 8 GHz
- High isolation: 48 dB at 8 GHz
- High input P1 dB: 37 dBm
- High input IP3: 62 dBm
- Fast settling time (0.05 dB within final RF out): 7.5 µs

The HMC1118 functional diagram is shown in Figure 1. The HMC1118 nominally requires dual supply voltages, $V_{DD}$ = +3.3 V and $V_{SS}$ = −2.5 V, at which the device is fully characterized. Consult the HMC1118 data sheet in conjunction with this application note for complete specifications when using the device in dual-supply operation.

The HMC1118 can be used at single positive supply of $V_{DD}$ = 3.3 V when the $V_{SS}$ pin is connected to ground. Although the large signal specifications are particularly compromised in single-supply operation, the device can still provide decent performance for many applications, which do not have negative supply voltages readily available. This application note primarily examines the operation of the HMC1118, and provides a performance comparison for the device in single-supply and dual-supply operation.

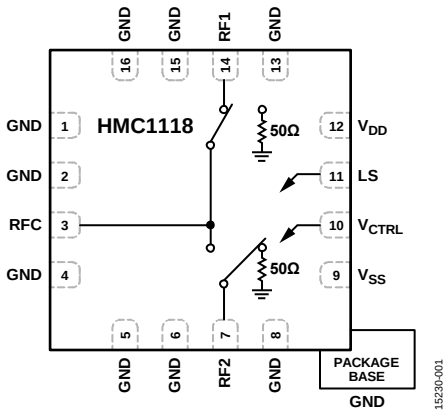


*Figure 1. HMC1118 Functional Diagram*

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## REVISION HISTORY

**11/2018—Rev. 0 to Rev. A**

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**12/2016—Revision 0: Initial Version**

# HMC1118 SWITCH OPERATION

The HMC1118 uses a familiar absorptive SPDT switch topology, utilizing a series field effect transistor (FET) and a shunt FET on two identical RF paths, and incorporates a driver for internal logic functions, shown in Figure 2.

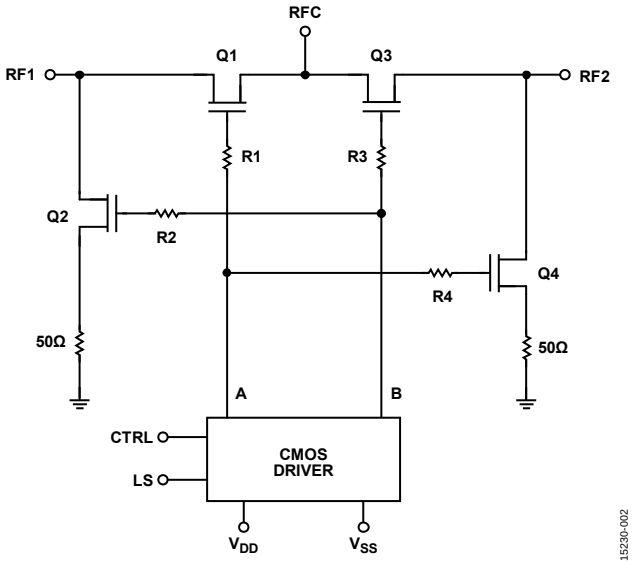


*Figure 2. HMC1118 Simplified Circuit Diagram*

The HMC1118 is designed to support two operation modes for its RF core as shown in Table 1. In Mode 1, the RF1 to RFC path is in insertion loss state and the RF2 to RFC path is in isolation state, and vice versa in Mode 2. The insertion loss path (for example, RF1 to RFC) conducts the RF signal equally well in both directions between its throw port (RF1) and common port (RFC). The isolation path provides high loss between the insertion loss ports (for example, RF1 and RFC) and its throw port terminated to an internal 50 Ω resistor to absorb applied signals.

In the insertion loss path, the series FET is turned on and the shunt FET is turned off. In the isolation path, the converse is true: the series FET is turned off and the shunt FET is turned on. Therefore, complementary control voltages are required for the series and shunt FETs on each RF path. The HMC1118 has a driver integrated on die to generate the A and B complementary control voltages, shown in Figure 2; therefore, the switch can be controlled from a single CMOS logic voltage applied to the $V_{CTRL}$ pin, and the LS pin can be tied ground or $V_{DD}$ (see Table 2).

**Table 1. Switch Modes**

| Mode | RF1 to RFC | RF2 to RFC | Q1, Q4 | Q2, Q3 |
|---|---|---|---|---|
| 1 | Insertion loss | Isolation | On | On |
| 2 | Isolation | Insertion loss | Off | Off |

**Table 2. Control Voltage**

| Mode | $V_{CTRL}$ | LS | A | B |
|---|---|---|---|---|
| 1 | High | Low | $V_{DD}$ | $V_{SS}$ |
| | Low | High | $V_{DD}$ | $V_{SS}$ |
| 2 | High | High | $V_{SS}$ | $V_{DD}$ |
| | Low | Low | $V_{SS}$ | $V_{DD}$ |

A switching FET operates as a voltage controlled device with three ports where a conduction channel for the RF signal is closed (on state) or closed (off state) between the drain and source ports, based on the control voltage applied to the gate port. The HMC1118 employs N-channel enhancement mode FETs with a typical pinch off voltage of 0.3 V, which is the potential difference needed between the gate and drain-source channel to turn on the FETs. The drain and source ports of each FET are held at dc ground to eliminate the need for dc blocking capacitors on RF ports, which limit the low frequency operation. Therefore, an absolute gate voltage greater than and less than 0.3 V turns the FET on and off, respectively.

The FETs are normally biased at extreme voltages, +3.3 V and −2.5 V, to establish certain voltages that turn on and turn off the FETs respectively, and to provide optimum RF performance. Because the HMC1118 does not incorporate a voltage regulator and a negative voltage generator, two regulated supply voltages applied externally to $V_{DD}$ and $V_{SS}$ pins are required to produce the necessary bias voltages for the FET devices. Although typical $V_{DD}$ and $V_{SS}$ are +3.3 V and −2.5 V respectively, the user has the flexibility to use the device with a single positive supply at $V_{DD}$ = 3.3 V only, when the $V_{SS}$ pin is connected to 0 V. However, this causes degradation of electrical specifications for some parameters mentioned in the Performance Comparison for Single-Supply vs. Dual-Supply Operation section.

# PERFORMANCE COMPARISON FOR SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

This section provides a performance comparison for the HMC1118 with dual supplies at $V_{DD}$ = +3.3 V and $V_{SS}$ = −2.5 V, and single supply only at $V_{DD}$ = 3.3 V when the $V_{SS}$ pin is connected to 0 V. Figure 6 shows a schematic of the evaluation board used in evaluating the performance of the HMC1118 in single-supply operation vs. dual-supply operation.

## SMALL SIGNAL PERFORMANCE

The HMC1118 is designed to provide optimum small signal performance for 50 Ω systems. When $V_{SS}$ is changed from −2.5 V to 0 V, which is sufficient to hold the FETs in the off state for small RF input signals, there is no degradation of small signal RF performance of the HMC1118. The return loss, insertion loss, and isolation are maintained over the entire operating frequency range as shown in Figure 3, Figure 4, and Figure 5.

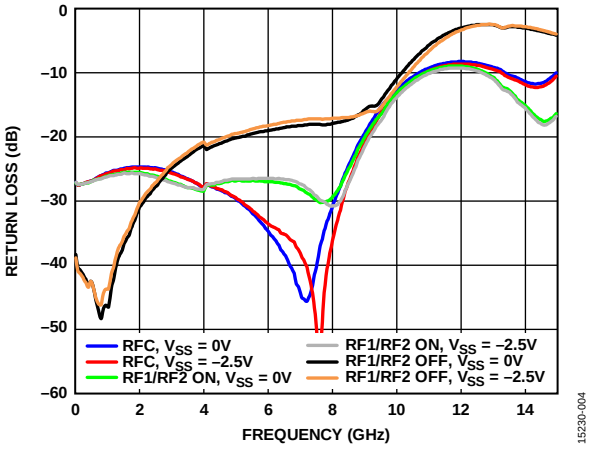


Figure 3. Return Loss vs. Frequency over $V_{SS}$

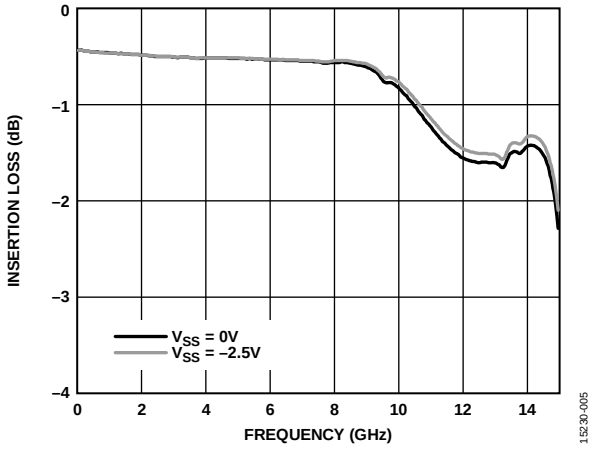


Figure 4. Insertion Loss vs. Frequency over $V_{SS}$

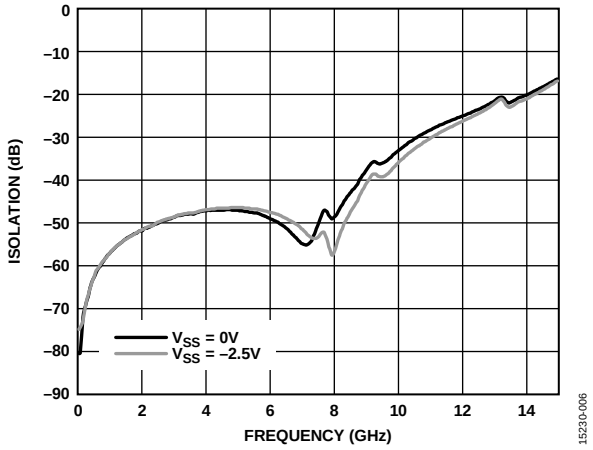


Figure 5. Isolation vs. Frequency over $V_{SS}$

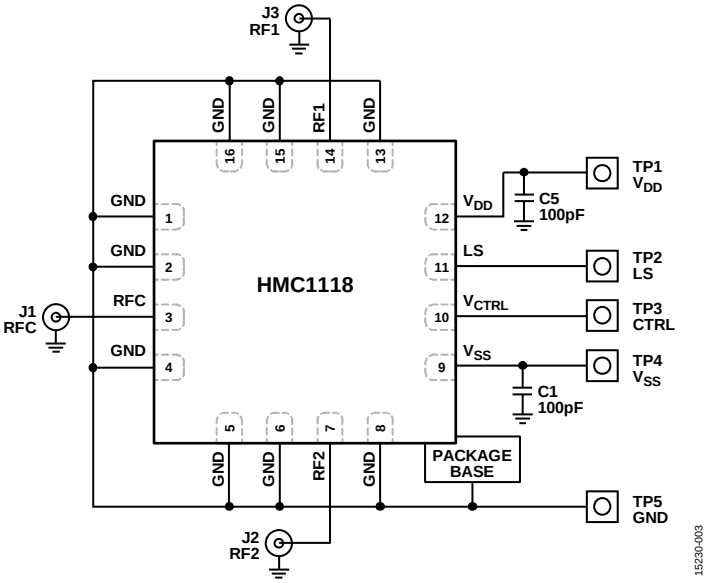


Figure 6. HMC1118 Evaluation Board Schematic

## LARGE SIGNAL PERFORMANCE

The HMC1118 stacks a number of FETs, in series on both series and shunt arms, to withstand power levels higher than the breakdown voltage of a single FET. The switch arms are optimized to achieve excellent linearity by evenly distributing the voltage across the FETs.

High RF power can modulate the gate voltage and drain source channel resistance. This causes intermodulation distortion and the compression or clipping of the input signal. Biasing the FET near pinch off level increases this effect.

Therefore, the power compression and linearity of the HMC1118 are degraded, as shown in Figure 7 and Figure 8, when $V_{SS}$ is changed from −2.5 V to 0 V.

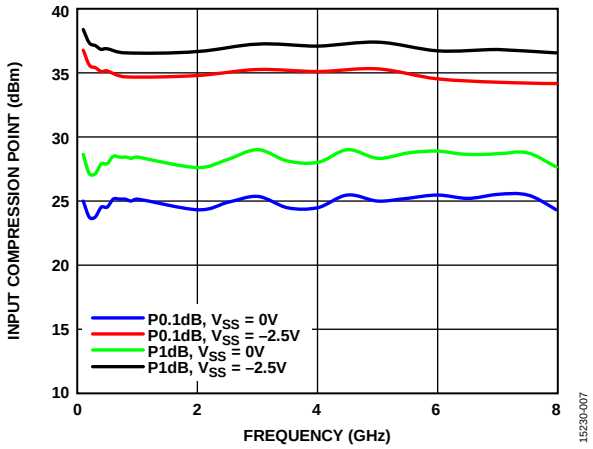


*Figure 7. Input Compression Point vs. Frequency over $V_{SS}$*

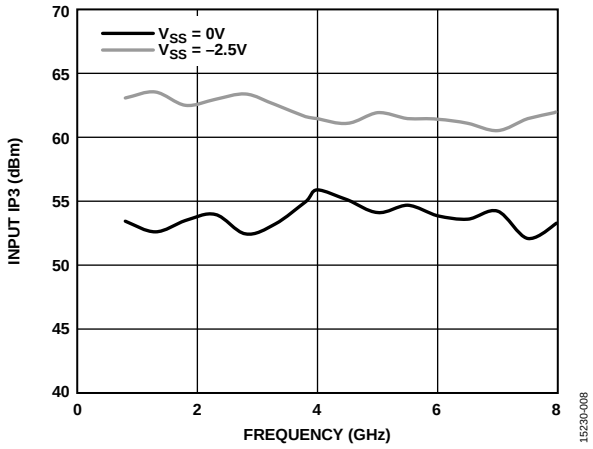


*Figure 8. Input IP3 vs. Frequency over $V_{SS}$*

## SWITCHING TIME

There is a trade-off between high power handling and fast switching time: the wider the gate resistor, the higher the power handling at a low frequency range; however, the switching time becomes slower. The HMC1118 optimizes the gate resistor value for high power handling at low frequency range and adequate switching time.

The switching time of the HMC1118 is degraded, shown in Figure 9, when $V_{SS}$ is changed from −2.5 V to 0 V.

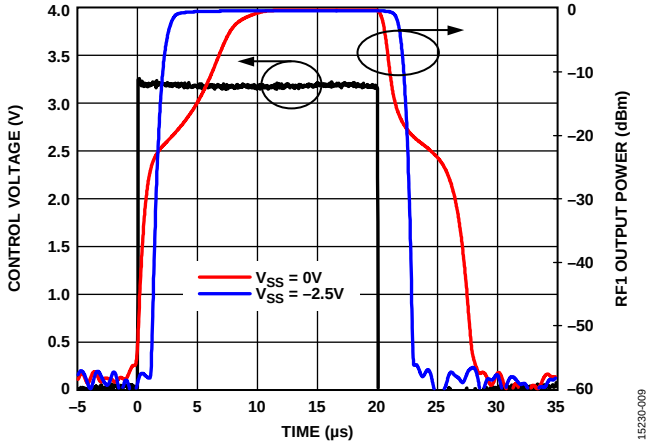


*Figure 9. Switching Time over $V_{SS}$*

## POWER HANDLING

The HMC1118 maintains the same thermal characteristics but enters into power compression at lower input power levels when $V_{SS}$ is changed from −2.5 V to 0 V. Considering the excessive rise in channel temperature, the absolute and recommended maximum input power ratings for the RF ports of the HMC1118 are degraded.

**Table 3. Maximum RF Input Power ($P_{IN, MAX}$) Ratings[1]**

| RF Input Power | Absolute Maximum (dBm) | Recommended Maximum (dBm) |
|---|---|---|
| Through Path | | |
| $V_{SS}$ = −2.5 V | 37 | 35 |
| $V_{SS}$ = 0 V | 29 | 27 |
| Termination Path | | |
| $V_{SS}$ = −2.5 V | 28 | 27 |
| $V_{SS}$ = 0 V | 24 | 22 |
| Hot Switch | | |
| $V_{SS}$ = −2.5 V | 30 | 27 |
| $V_{SS}$ = 0 V | 24 | 22 |

[1] At $V_{CTRL}$ = 0 V or 3.3 V, $T_{CASE}$ = 85°C, f = 2 GHz.

## SUMMARY

Operating the HMC1118 with a single positive supply of $V_{DD}$ = 3.3 V degrades the power handling performance ($P_{IN, MAX}$, $P_{1dB}$, and IP3) and switching speed (on and off times and rise and fall times) but does not change the small signal characteristics (insertion loss, isolation, and return losses). The HMC1118 can be used when the $V_{SS}$ pin is connected to ground if the reduced power handling and switching speed specifications are decent for the application.


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