Silicon SPDT Switch, Reflective, 35 GHz to 44 GHz

Preliminary Technical Data

ADRF5301

FEATURES

- Reflective design
- Low insertion loss: 1.8 dB at 44 GHz
- High isolation: 28 dB at 44 GHz
- High input linearity
  - 0.1 dB power compression (P0.1dB): 37 dBm
  - Third-order intercept (IP3): 52 dBm
- High RF power handling:
  - 28 dBm average
  - 36 dBm peak
- Single supply operation: 3.3V
  - Internal negative voltage generator (NVG)
- RF settling time (0.1 dB final RF output): 45 ns
- 20-terminal, 3 mm × 3 mm, land grid array package
- Pin compatible with the ADRF5300: 24 GHz - 32 GHz

APPLICATIONS

- Industrial scanner
- Test instrumentation
- Cellular infrastructure mmWave 5G
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

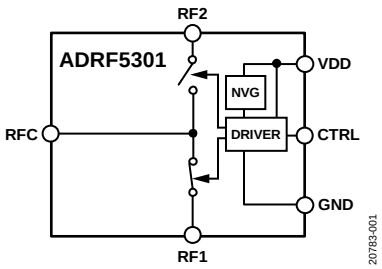

Figure 1.

GENERAL DESCRIPTION

The ADRF5301 is a reflective, single-pole, double-throw (SPDT) switch manufactured in the silicon process.

The ADRF5301 was developed for 5G applications from 35 GHz to 44 GHz. This device has low insertion loss of 1.8 dB, high isolation of 28 dB, and radio frequency (RF) input power handling capability of 28 dBm average and 36 dBm peak.

The ADRF5301 incorporates a negative voltage generator (NVG) to operate with a single positive supply of 3.3 V applied to the VDD pin. The devices employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible control.

The ADRF5301 is pin-compatible with the ADRF5300, which operates from 24 GHz to 32 GHz.

The ADRF5301 comes in a 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

Rev. PrB

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SPECIFICATIONS

V_{DD} = 3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			35		44	GHz
INSERTION LOSS						
Between RFC and RF1/RF2		f = 35 GHz to 44 GHz		1.8		dB
ISOLATION						
Between RFC and RF1/RF2		f = 35 GHz to 44 GHz		28		dB
RETURN LOSS						
RFC and RF1/RF2 (On)		f = 35 GHz to 44 GHz		10		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		15		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		35		ns
RF Settling Time						
0.1 dB		50% V_{CTL} to 0.1 dB of final RF output		45		ns
0.05 dB		50% V_{CTL} to 0.05 dB of final RF output		50		ns
INPUT LINEARITY		f = 35 GHz to 44 GHz				
0.1 dB Power Compression	P0.1dB			37		dBm
Third-Order Intercept	IP3			52		dBm
SUPPLY CURRENT	I_{DD}			450		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage	V_{DD}		3.15		3.45	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power	P_{IN}	f = 35 GHz to 44 GHz, T_{CASE} = 85 °C				
Average					28	dBm
Peak					36	dBm
Case Temperature	T_{CASE}		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
RF Input Power (T_{CASE} = 85 °C)	
Average	28.5 dBm
Peak	36.5 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	TBD

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-20-9, Through Path	232	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

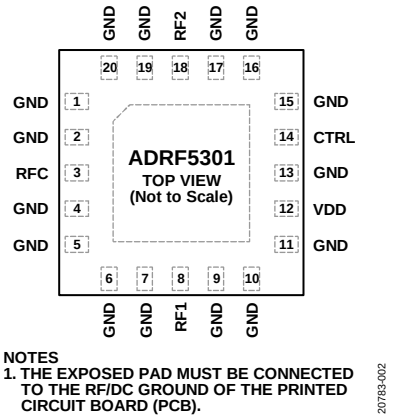

Figure 2. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9 to 11, 13, 15 to 17, 19, 20	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RFC	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
8	RF1	RF Throw Port 1. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
12	VDD	Positive Supply Voltage Input.
14	CTRL	Control Voltage Input.
18	RF2	RF Throw Port 2. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

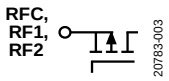

Figure 3. RFC, RF1, and RF2 Pins Interface Schematic

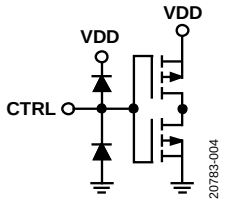

Figure 4. CTRL Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. Measured on the probe matrix board using ground-signal-ground (GSG) probes close to the RF pins.

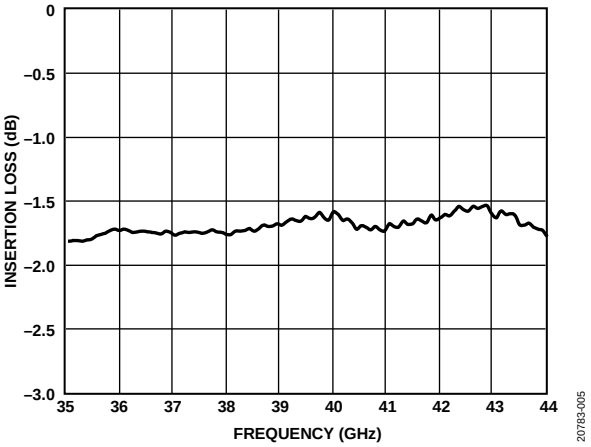

Figure 5. Insertion Loss vs. Frequency, RF1 Selected

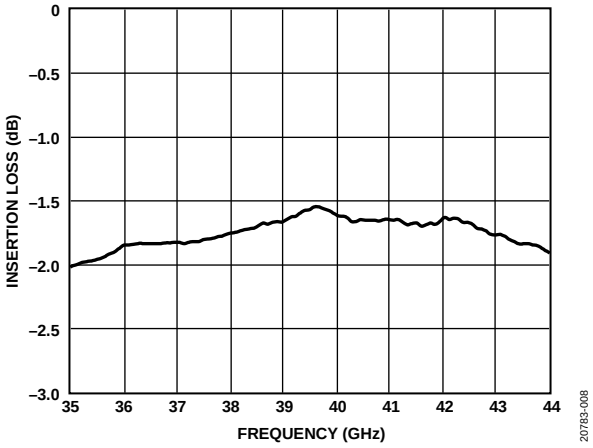

Figure 8. Insertion Loss vs. Frequency, RF2 Selected

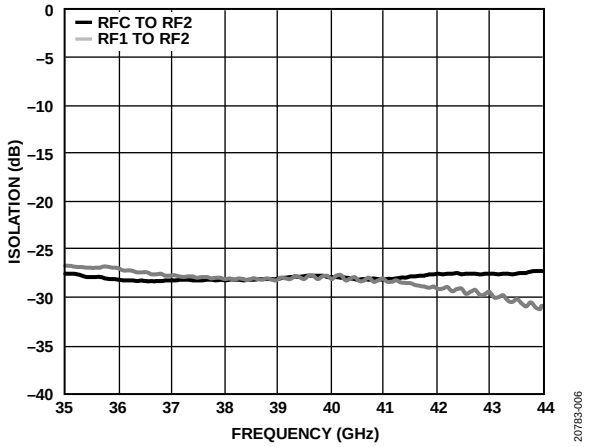

Figure 6. Isolation vs. Frequency, RF1 Selected

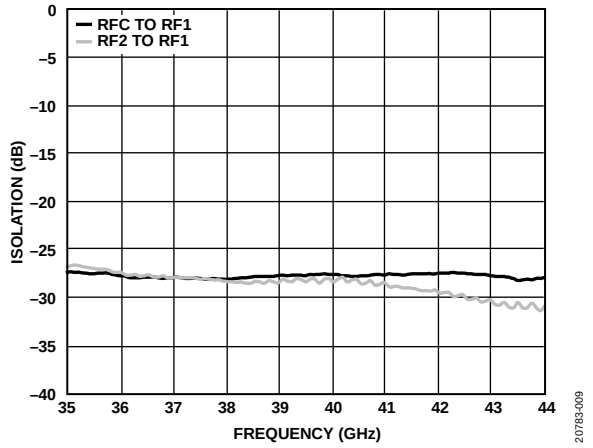

Figure 9. Isolation vs. Frequency, RF2 Selected

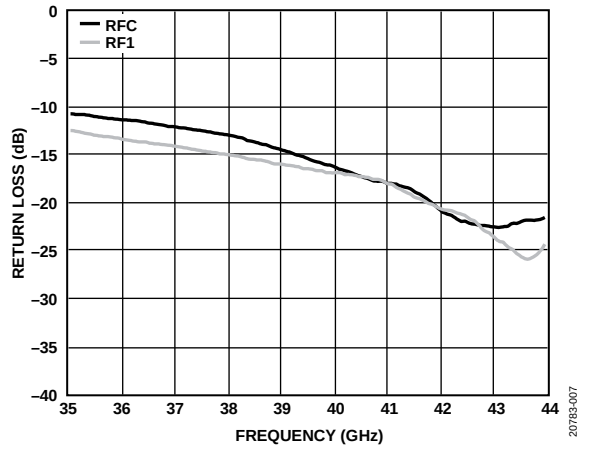

Figure 7. Return Loss vs. Frequency, RF1 Selected

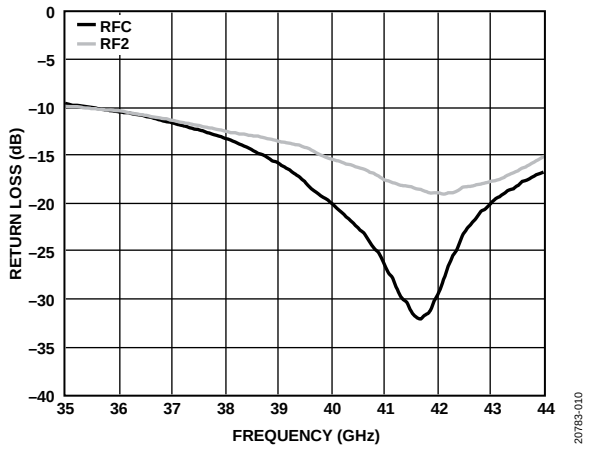

Figure 10. Return Loss vs. Frequency, RF2 Selected

THEORY OF OPERATION

The ADRF5301 integrates a negative voltage generator (NVG) and requires a single positive supply voltage applied to the VDD pin. Bypassing capacitors are recommended on the supply line to minimize RF coupling.

All of the RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5301 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features a single digital control input pin, CTRL, which controls the state of the RF paths. The logic level applied to the CTRL pin determines which RF port is in the insertion loss state while the other path is in the isolation state (see Table 5).

Table 5. Control Voltage Truth Table

Digital Control Input	RF Paths	
CTRL	**RF1 to RFC**	**CTRL**
High	Insertion loss (on)	Isolation (off)
Low	Isolation (off)	Insertion loss (on)

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw port that is reflective.

The ideal power-up sequence is as follows:

1. Connect GND reference.
2. Power up supply input VDD.
3. Apply digital control input CTRL. Applying the CTRL control before applying the VDD supply inadvertently forward biases and damages the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state
4. Apply RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

APPLICATIONS INFORMATION

Figure 11 shows the basic connections for operating the ADRF5301. Apply a 3.3 V supply to the VDD pin that is decoupled with a 100 pF capacitor placed as close to the device as possible. The CTRL pin is driven with a CMOS/LVTTL control. The RF pins must be connected to 50 Ω impedance. The ground pins and exposed pad must be directly connected to the ground plane.

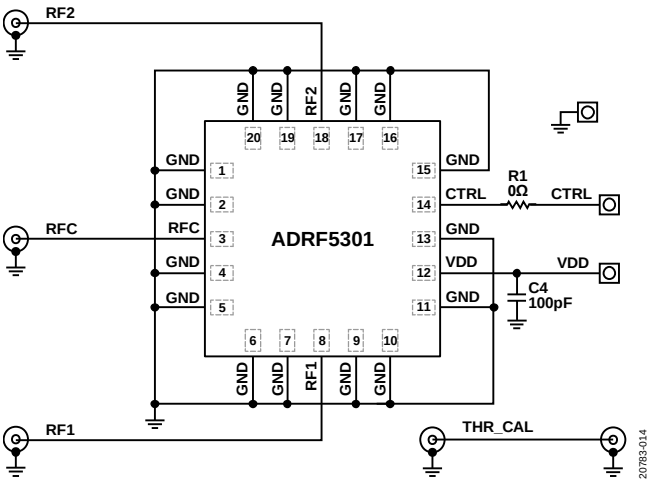

Figure 11. Basic Connections

OUTLINE DIMENSIONS

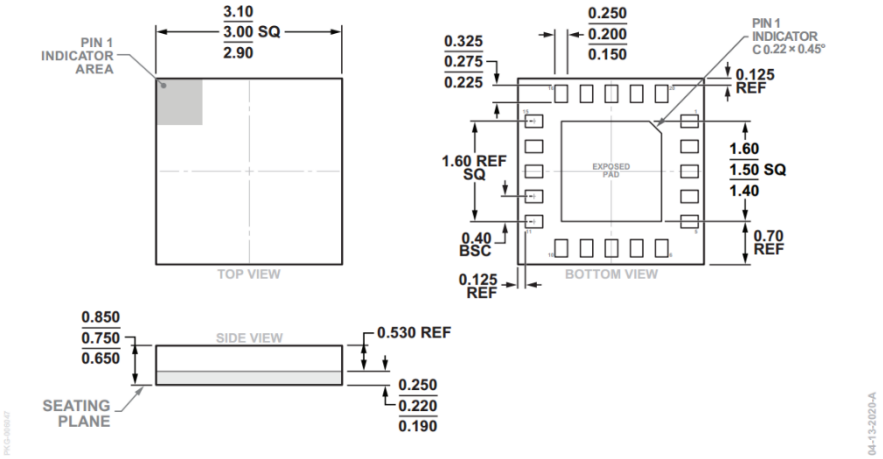

Figure 12. 20-Terminal Land Grid Array [LGA]
3 mm × 3 mm Body and 0.75 mm Package Height
(CC-20-9)
Dimensions shown in millimeters

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