Data Sheet

ADRF5345

High Linearity, Silicon SP4T Switch, 1.8 GHz to 3.8 GHz

FEATURES

- Reflective design
- Low Insertion Loss
  - 0.35 dB to 2.8 GHz typical
  - 0.40 dB to 3.8 GHz typical
- High power handling at T_{CASE} = 105°C
  - Long-term (>10 years) average
    - Continuous wave power: 39 dBm
    - LTE signal
      - Average power: 39 dBm
      - Peak power: 49 dBm
- High input linearity, IP3: 84 dBm typical
- ESD ratings
  - HBM: 2000 V, Class 2
  - CDM: 1000 V, Class C3
- Single-supply operation, integrated NVG
- Positive control, LVCMOS-/LVTTL- compatible
- 4 mm x 4 mm, 22-terminal LGA package

APPLICATIONS

- 5G antenna tilting
- Wireless infrastructure
- Military and high reliability applications
- Test equipment
- Pin diode replacement

FUNCTIONAL BLOCK DIAGRAM

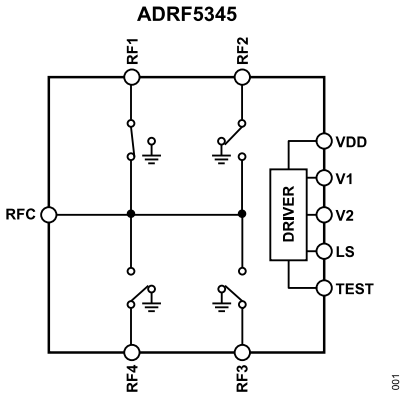

Figure 1.

GENERAL DESCRIPTION

The ADRF5345 is a high linearity, reflective, single-pole, four-throw (SP4T) switch manufactured in the silicon process.

The ADRF5345 operates from 1.8 GHz to 3.8 GHz with a typical insertion loss lower than 0.40 dB and a typical input IP3 of 84 dBm. The device has an RF input power handling capability of 39 dBm for continuous wave signals and 39 dBm average and 49 dBm peak for long-term evolution (LTE) signals.

The ADRF5345 incorporates an integrated negative voltage generator (NVG) to operate with a single positive supply of 5 V (V_{DD}) applied to the VDD pin drawing a 2 mA supply current. The device employs low voltage complementary metal-oxide semiconductor (LVCMOS)-/low voltage transistor to transistor logic (LVTTL)- compatible controls.

The ADRF5345 comes in a 4 mm × 4 mm, 22-terminal, RoHS-compliant, land grid array (LGA) package and operates between −40°C to +105°C.

TABLE OF CONTENTS

REVISION HISTORY

12/2021—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_{DD}) = 5 V, control voltage (V_{CTL}) = 0 V or 3.3 V, T_A = 25°C, and it is a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		1.8		3.8	GHz
INSERTION LOSS					
Between RFC and RF1 to RF4 (On)	2.3 GHz to 2.8 GHz		0.35		dB
	3.3 GHz to 3.8 GHz		0.40		dB
ISOLATION					
Between RFC and RF1 to RF4 (Off)	2.3 GHz to 2.8 GHz		32		dB
	3.3 GHz to 3.8 GHz		29		dB
RETURN LOSS					
RFC and RF1 to RF4 (On)	2.3 GHz to 2.8 GHz		24		dB
	3.3 GHz to 3.8 GHz		24		dB
SWITCHING					
Rise and Fall Time (t_{RISE}, t_{FALL})	90% to 10% of RF output (RF_{OUT})		120		µs
On and Off Time (t_{ON}, t_{OFF})	50% V_{CTL} to 10% to 90% of RF_{OUT}		140		µs
0.1 dB Settling Time	50% V_{CTL} to 0.1 dB of final RF_{OUT}		340		µs
INPUT LINEARITY					
0.1 dB Power Compression (P0.1dB)	LTE (10 dB peak average ratio (PAR))		50		dBm
Third-Order Intercept (IP3)	Two-tone input power = 30 dBm continuous wave per tone		84		dBm
SUPPLY CURRENT			2		mA
DIGITAL CONTROL INPUTS					
Voltage		0		0.8	V
Low Voltage (V_{IL})					
High Voltage (V_{IH})		1.2		3.45	V
Current					
Low (I_{INL})	LS		35		µA
	V1 and V2		<1		µA
High (I_{INH})	LS		<1		µA
	V1 and V2		1.5		µA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage (V_{DD})		4.75		5.25	V
Control Voltage (V_{CTL})		0		3.45	V
RF Input Power	T_{CASE} = 105°C, life time				
Continuous Wave				39	dBm
LTE Signal	10 dB PAR				
Average				39	dBm
Peak				49	dBm
Continuous Wave	T_{CASE} = 105°C, single event (<10 sec)			42	dBm
LTE Signal	10 dB PAR				
Average				42	dBm
Peak				52	dBm
Case Temperature (T_{CASE})		–40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD}	–0.3 V to +5.5 V
V_{CTL}	–0.3 V to +3.6 V
RF Input Power[1] (T_{CASE} = 105°C)	
Average	42.5 dBm
Peak	52.5 dBm
Temperature	
Junction	135°C
Storage	–65°C to +150°C
Reflow	260°C

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-22-2	37	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 105°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5345

Table 4. ADRF5345, 22-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	2000	2
CDM	1000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

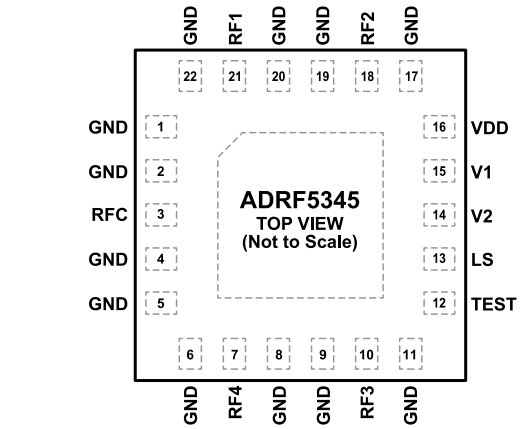

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 6, 8, 9, 17, 19, 20, 22	GND	Ground.
3	RFC	RF Common Port. The RFC pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
7	RF4	RF Throw Port 4. The RF4 pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
10	RF3	RF Throw Port 3. The RF3 pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
12	TEST	Factory Test Pin. The TEST pin must be tied to ground.
13	LS	Logic Select. See Table 6.
14	V2	Control Input 2. See Table 6.
15	V1	Control Input 1. See Table 6.
16	VDD	Positive Supply Voltage.
18	RF2	RF Throw Port 2. The RF2 pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
21	RF1	RF Throw Port 1. The RF1 pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB.

INTERFACE SCHEMATICS

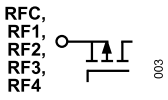

Figure 3. RF Interface Schematic

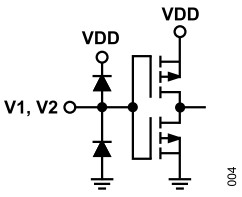

Figure 4. V1 and V2 Control Interface Schematic

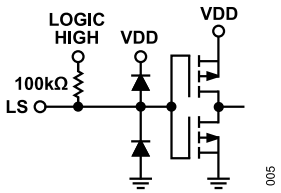

Figure 5. LS Control Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 5 V, V_{CTRL} = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted. Insertion loss and return loss are measured on the ADRF5345-EVALZ evaluation board.

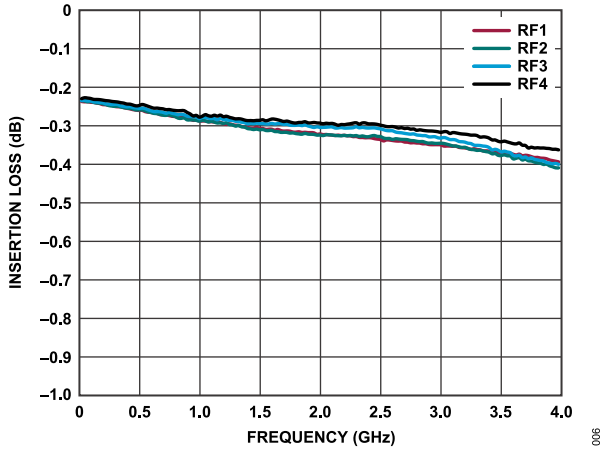

Figure 6. Insertion Loss for RFC to RFx Selected vs. Frequency

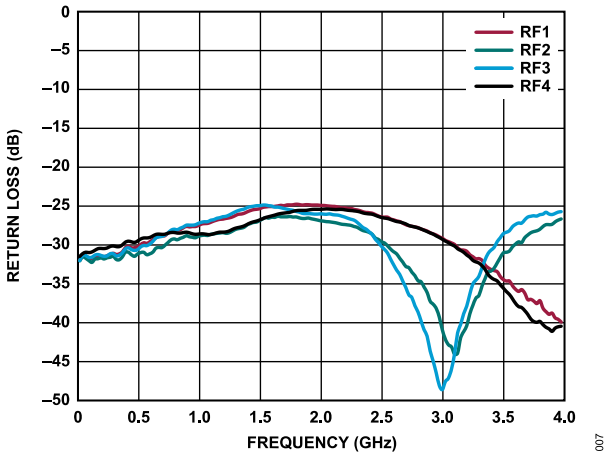

Figure 7. Return Loss for RFC when RFx Selected vs. Frequency

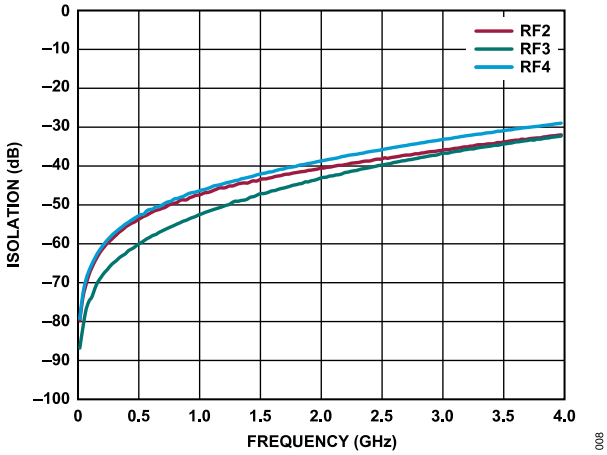

Figure 8. RFC to RF2, RF3, and RF4 Isolation vs. Frequency, RF1 Selected

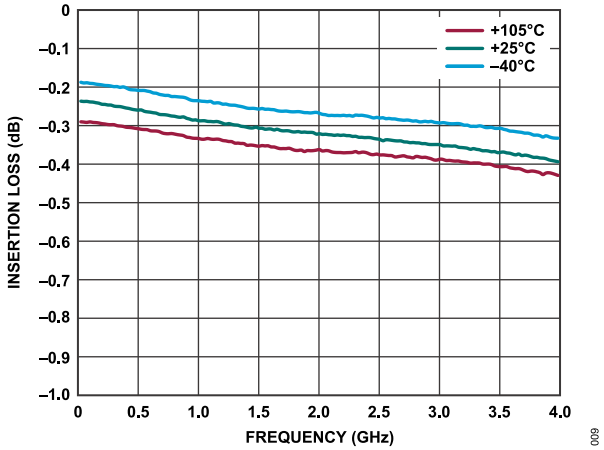

Figure 9. Insertion Loss for RFC to RF1 Selected vs. Frequency over Various Temperatures

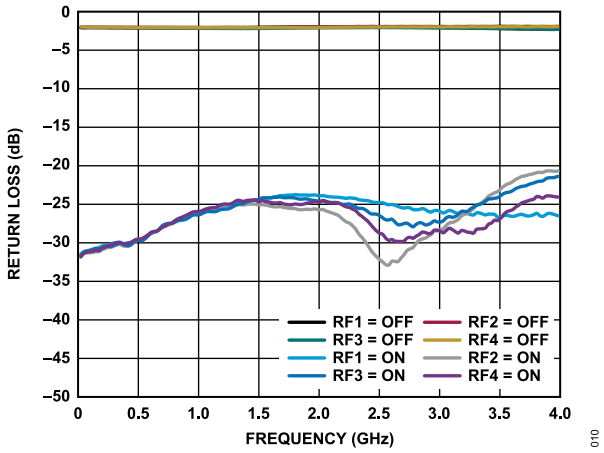

Figure 10. Return Loss for RFx Unselected and Selected

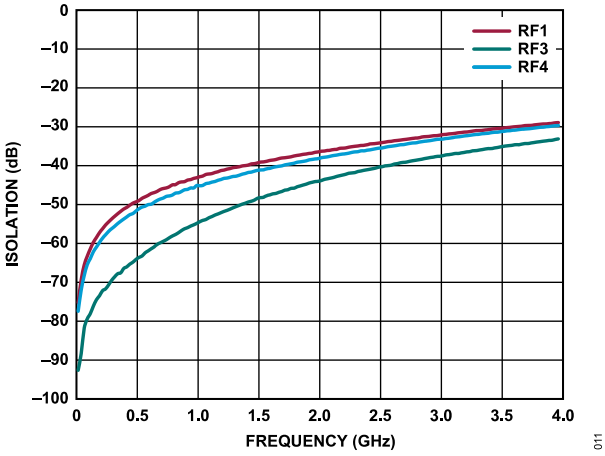

Figure 11. RFC to RF1, RF3, and RF4 Isolation vs. Frequency, RF2 Selected

TYPICAL PERFORMANCE CHARACTERISTICS

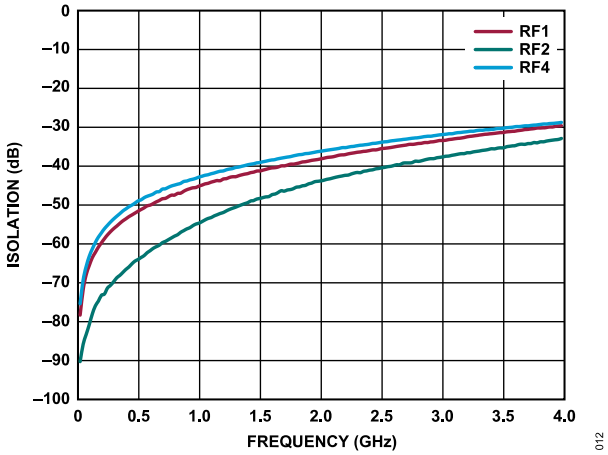

Figure 12. RFC to RF1, RF2, and RF4 Isolation vs. Frequency, RF3 Selected

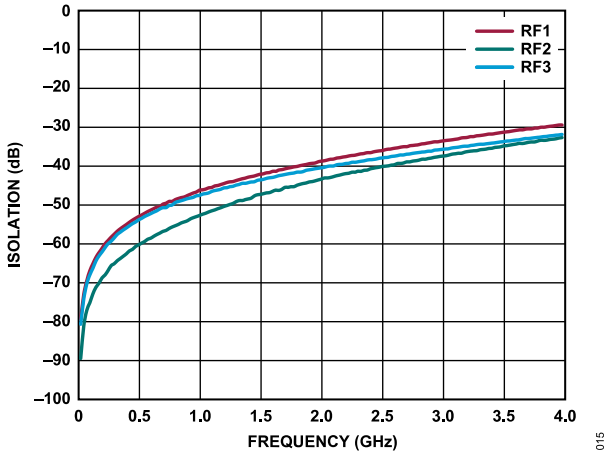

Figure 15. RFC to RF1, RF2, RF3 Isolation vs. Frequency, RF4 Selected

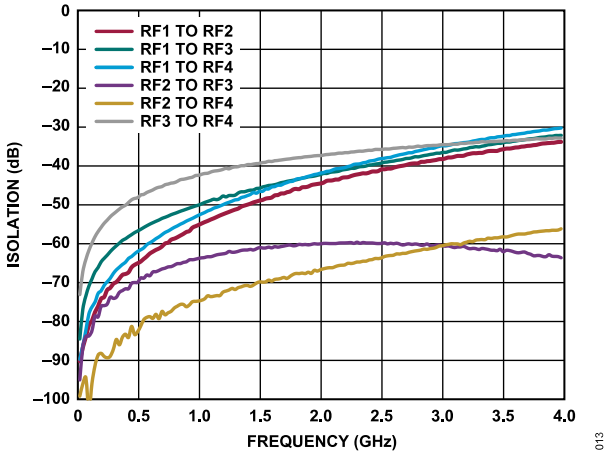

Figure 13. Channel to Channel Isolation vs. Frequency, RFC to RF1 Path Selected

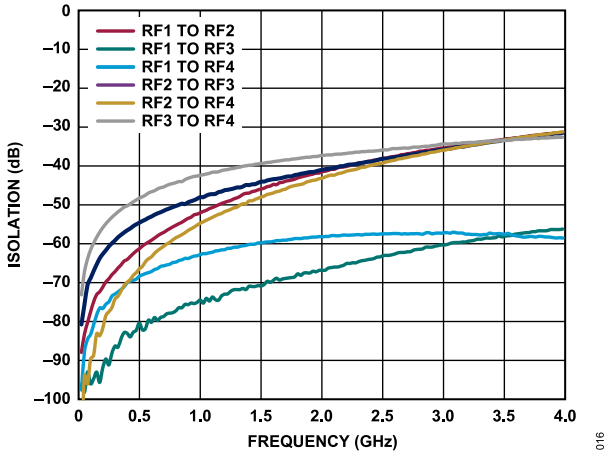

Figure 16. Channel to Channel Isolation vs. Frequency, RFC to RF2 Path Selected

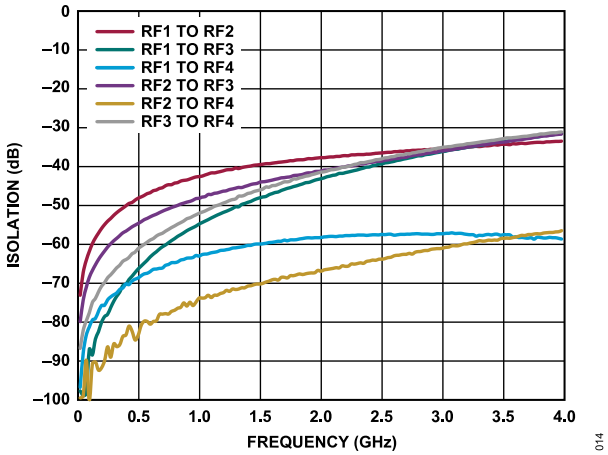

Figure 14. Channel to Channel Isolation vs. Frequency, RFC to RF3 Path Selected

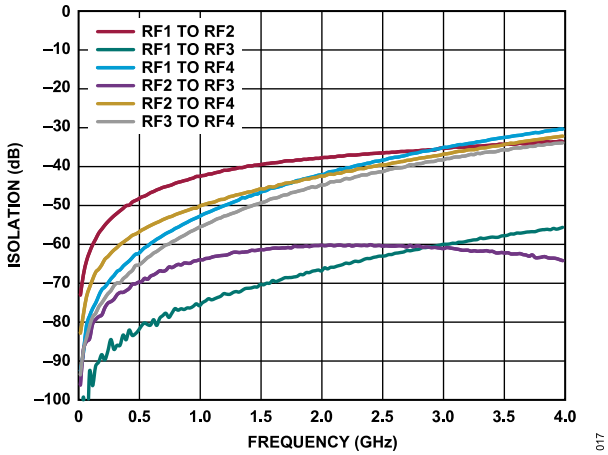

Figure 17. Channel to Channel Isolation vs. Frequency, RFC to RF4 Path Selected

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT THIRD-ORDER INTERCEPT

V_{DD} = 5 V, V_{CTRL} = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted. All of the large signal performance parameters were measured on the ADRF5345-EVALZ evaluation board.

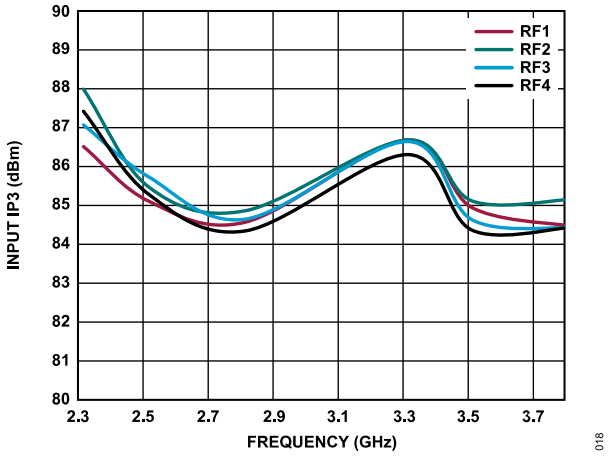

Figure 18. Input IP3 for RFC to RFx Selected vs. Frequency

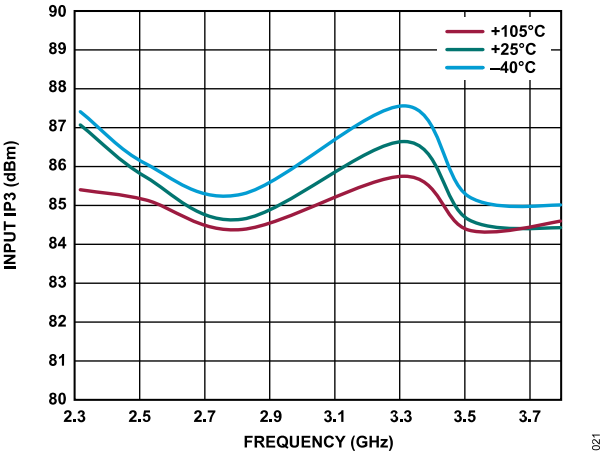

Figure 21. Input IP3 for RF3 vs. Frequency over Various Temperatures

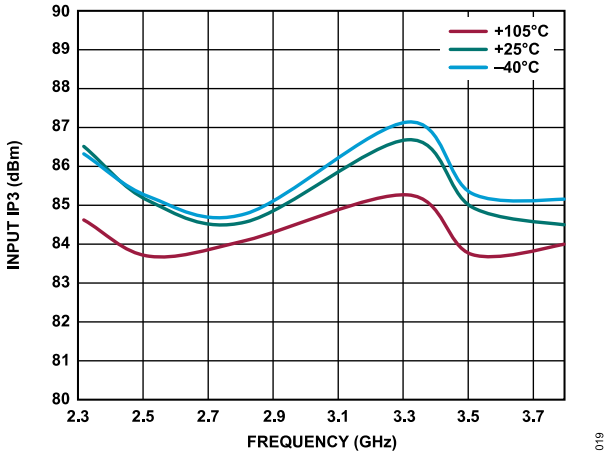

Figure 19. Input IP3 for RF1 vs. Frequency over Various Temperatures

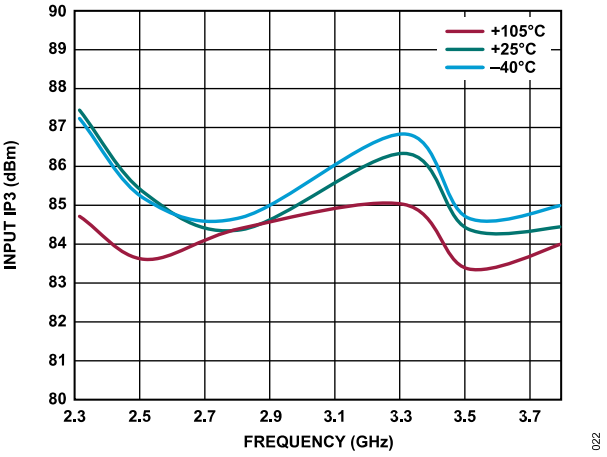

Figure 22. Input IP3 for RF4 vs. Frequency over Various Temperatures

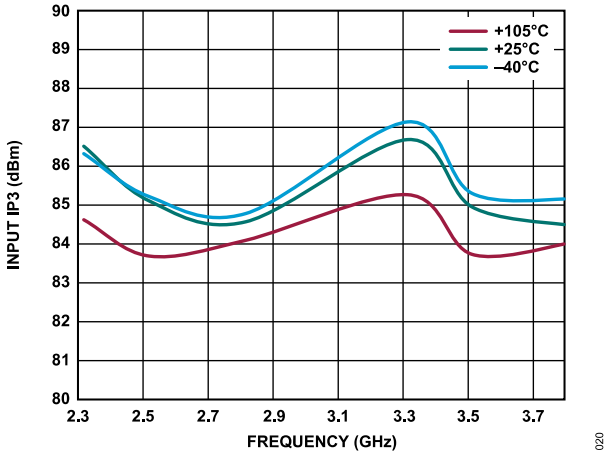

Figure 20. Input IP3 for RF2 vs. Frequency over Various Temperatures

THEORY OF OPERATION

The ADRF5345 integrates a NVG and requires a single, positive supply voltage applied to the VDD pin. Bypass capacitors are recommended on the supply and control lines to minimize RF coupling.

All of the RF ports (RFC and RF1 to RF4) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5345 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified LVCMOS-/LVTTL-compatible control interface. The driver features three digital control input pins (LS, V1, and V2) that control the state of the RFx paths. See Table 6.

The logic select (LS) input allows the user to define the control input logic sequence for the RF path selections. The logic levels applied to the V1 and V2 pins determine which RFx port is in the insertion loss state while the other three paths are in the isolation state.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD.
3. Apply the digital control inputs: LS, V1, and V2. Applying digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. A series 1 kΩ resistor can be used to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, controller output is in high impedance state) after VDD is powered up, it is recommended to use pull-up and power-down resistors.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltage Truth Table

Digital Control Inputs			RFx Paths			
LS	**V1**	**V2**	**RF1 to RFC**	**RF2 to RFC**	**RF3 to RFC**	**RF4 to RFC**
Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)

APPLICATION INFORMATION

Connect the RF ports of the ADRF5345 to transmission lines with a characteristic impedance of 50 Ω. The package ground leads and the backside ground slug must connect directly to the ground plane.

The ADRF5345 has one power supply pin (VDD) and three control pins (V1, V2, and LS). The supply pin must be decoupled with 100 pF and 4.7 µF capacitors, while the control pins must be decoupled with 100 pF capacitors.

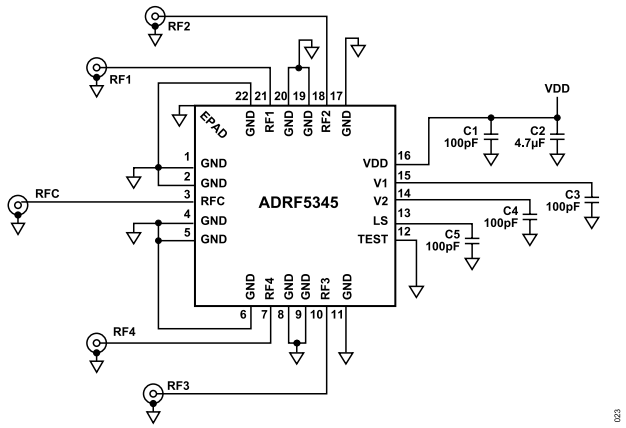

Figure 23. Recommended Schematic

A typical application of ADRF5345 is a 4 step phase shifter that is achieved by connecting the SP4T switches back to back. Each RF arm must have a different delay line (see Figure 24).

The switch control inputs, V1 and V2, can be connected together to configure the back to back phase shifter, which is achieved by applying inverted logic to LS pin of SW1 and SW2. The LS pins do not require additional routing due to the internal pull-up. Therefore, the LS pin of ADRF5345 can be directly grounded or only decoupled with a capacitor.

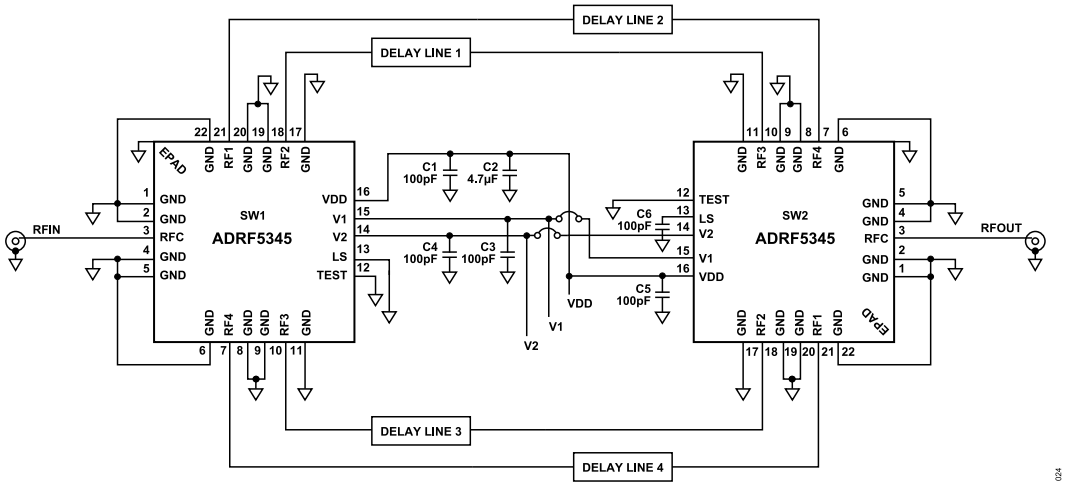

Figure 24. Back to Back Configuration Schematic

OUTLINE DIMENSIONS

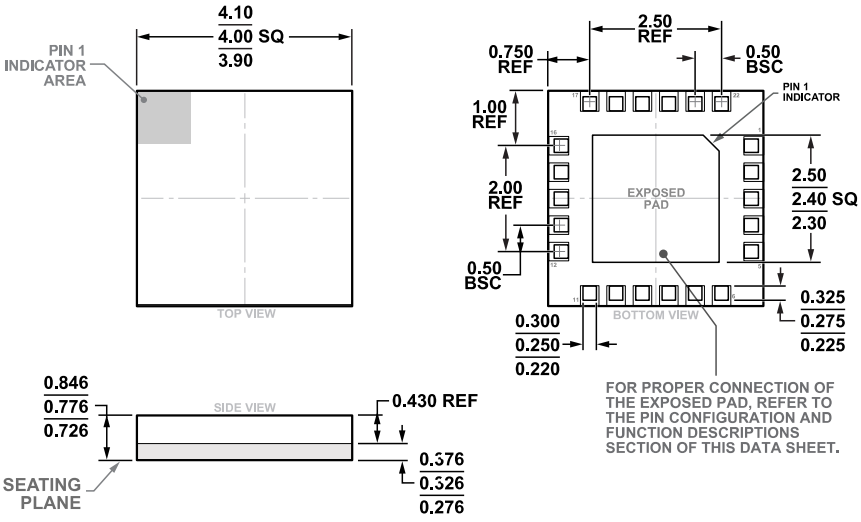

Figure 25. 22-Terminal Land Grid Array [LGA]
4 mm × 4 mm Body and 0.776 mm Package Height
(CC-22-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Information	Package Option
ADRF5345BCCZN	–40°C to +105°C	22-Terminal Land Grid Array [LGA]	Cut Tape, 1	CC-22-2
ADRF5345BCCZN-R7	–40°C to +105°C	22-Terminal Land Grid Array [LGA]	7" Tape and Reel, 1500	CC-22-2
ADRF5345BCCZN-RL	–40°C to +105°C	22-Terminal Land Grid Array [LGA]	13" Tape and Reel, 5000	CC-22-2

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADRF5345-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.