Die on Carrier, Silicon Digital Attenuator, 0.5 dB LSB, 6-Bit, 100 MHz to 40 GHz

FEATURES

- Ultrawideband frequency range: 100 MHz to 40 GHz
- Attenuation range: 31.5 dB with 0.5 dB steps
- Bond pads for wire bond and ribbon bond
- Low insertion loss
  - 1.7 dB typical up to 18 GHz
  - 2.2 dB typical up to 26 GHz
  - 3.2 dB typical up to 40 GHz
- Attenuation accuracy
  - ±(0.10 + 2.0% of attenuation state) typical up to 26 GHz
  - ±(0.13 + 1.5% of attenuation state) typical up to 35 GHz
  - ±(0.30 + 1.5% of attenuation state) typical up to 40 GHz
- Typical step error
  - ±0.12 dB typical up to 26 GHz
  - ±0.30 dB typical up to 35 GHz
  - ±0.60 dB typical up to 40 GHz
- High input linearity
  - P0.1dB insertion loss state: 31 dBm typical
  - P0.1dB other attenuation states: 28 dBm typical
  - IP3: 50 dBm typical
- High RF power handling
  - 26 dBm steady state average
  - 31 dBm steady state peak
- Tight distribution in relative phase
- No low frequency spurious signals
- SPI and parallel mode control, CMOS/LVTTL compatible
- RF amplitude settling time (0.1 dB of final RF output): 250 ns
- 18-pad, 3.171 mm × 1.616 mm, die on carrier [CHIP]

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

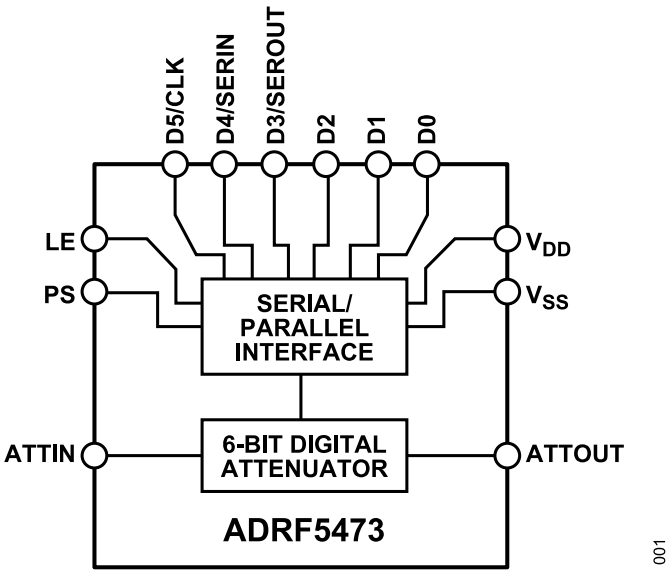

Figure 1.

GENERAL DESCRIPTION

The ADRF5473 is a 6-bit digital attenuator with a 31.5 dB attenuation range in 0.5 dB steps manufactured in a silicon process attached on a gallium arsenide (GaAs) carrier substrate. The substrate incorporates the bond pads for chip and wire assembly, and the bottom of the device is metalized and connected to ground.

This device operates from 100 MHz to 40 GHz with better than 3.2 dB of insertion loss and excellent attenuation accuracy. The ADRF5473 has an RF input power handling capability of 26 dBm average and 31 dBm peak for all states.

The ADRF5473 requires a dual-supply voltage of +3.3 V and −3.3 V. The device features serial peripheral interface (SPI), parallel mode control, and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5473 is designed to match a characteristic impedance of 50 Ω.

Note that when referring to a single function of a multifunction pad in this data sheet, only the portion of the pad name that is relevant is mentioned. For full pad names of the multifunction pads, refer to the section.

TABLE OF CONTENTS

REVISION HISTORY

12/2021—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = +3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and 50 Ω system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 3 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are deembedded. See Applications Information section for assembly details.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		40,000	MHz
INSERTION LOSS	100 MHz to 10 GHz		1.3		dB
	10 GHz to 18 GHz		1.7		dB
	18 GHz to 26 GHz		2.2		dB
	26 GHz to 35 GHz		2.8		dB
	35 GHz to 40 GHz		3.2		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	100 MHz to 10 GHz		17		dB
	10 GHz to 18 GHz		18		dB
	18 GHz to 26 GHz		17		dB
	26 GHz to 35 GHz		15		dB
	35 GHz to 40 GHz		15		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		31.5		dB
Step Size	Between any successive attenuation states		0.5		dB
Accuracy	Referenced to insertion loss				
	100 MHz to 10 GHz		±(0.05 + 1.5% of state)		dB
	10 GHz to 18 GHz		±(0.07 + 2.0% of state)		dB
	18 GHz to 26 GHz		±(0.10 + 2.0% of state)		dB
	26 GHz to 35 GHz		±(0.13 + 1.5% of state)		dB
	35 GHz to 40 GHz		±(0.30 + 1.5% of state)		dB
Step Error	Between any successive state				
	100 MHz to 10 GHz		±0.11		dB
	10 GHz to 18 GHz		±0.12		dB
	18 GHz to 26 GHz		±0.12		dB
	26 GHz to 35 GHz		±0.30		dB
	35 GHz to 40 GHz		±0.60		dB
RELATIVE PHASE	Referenced to insertion loss				
	10 GHz		18		Degrees
	18 GHz		33		Degrees
	26 GHz		50		Degrees
	35 GHz		75		Degrees
	40 GHz		80		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power (P_{IN}) = 10 dBm				
Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		35		ns
On and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF output		125		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered control to 0.1 dB of final RF output		250		ns
0.05 dB	50% triggered control to 0.05 dB of final RF output		350		ns
Overshoot			1		dB
Undershoot			−2.5		dB

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF Phase Settling Time	Frequency = 5 GHz				
5°	50% triggered control to 5° of final RF output		160		ns
1°	50% triggered control to 1° of final RF output		180		ns
INPUT LINEARITY[1]	Frequency = 100 MHz to 30 GHz				
0.1 dB Power Compression (P0.1dB)					
Insertion Loss State			31		dBm
Other Attenuation States			28		dBm
Third-Order Intercept (IP3)	Two-tone P_{IN} = 14 dBm per tone, Δf = 1 MHz, all attenuation states		50		dBm
DIGITAL CONTROL INPUTS	LE, PS, D0, D1, D2, D3/SEROUT[2], D4/SERIN, and D5/CLK				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			<1		µA
High (I_{INH})	D0, D1, D2		33		µA
	LE, PS, D3/SEROUT[2], D4/SERIN, and D5/CLK		<1		µA
DIGITAL CONTROL OUTPUT	D3/SEROUT[2]				
Voltage					
Low (V_{OUTL})			0 ± 0.3		V
High (V_{OUTH})			V_{DD} ± 0.3		V
Low and High Current (I_{OUTL} and I_{OUTH})				0.5	mA
SUPPLY CURRENT	V_{DD} and V_{SS}				
Positive Supply Current			117		µA
Negative Supply Current			−117		µA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
Positive (V_{DD})		3.15		3.45	V
Negative (V_{SS})		−3.45		−3.15	V
Digital Control Voltage		0		V_{DD}	V
RF Power Handling[3]	Frequency = 100 MHz to 30 GHz, T_{DIE}[4] = 85°C[5], all attenuation states				
Input at ATTIN	Steady state average			26	dBm
	Steady state peak			31	dBm
	Hot switching average			23	dBm
	Hot switching peak			27	dBm
Input at ATTOUT	Steady state average			17	dBm
	Steady state peak			21	dBm
	Hot switching average			14	dBm
	Hot switching peak			18	dBm
Die Temperature (T_{DIE})[4]		−40		+105	°C

[1] Input linearity performance degrades over frequency, see Figure 20 to Figure 23.

[2] D3/SEROUT is an input in parallel control mode and an output in serial control mode. See Table 6 for the pad function descriptions.

[3] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[4] T_{DIE} refers to the bottom of the die on carrier.

[5] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specifications by 3 dB.

SPECIFICATIONS

TIMING SPECIFICATIONS

See Figure 25, Figure 26, and Figure 27 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period, see Figure 25	70			ns
t_{CS}	Control setup time, see Figure 25	15			ns
t_{CH}	Control hold time, see Figure 25		3	5	ns
t_{LN}	LE setup time, see Figure 25	15			ns
t_{LEW}	Minimum LE pulse width, see Figure 25 and Figure 27		10		ns
t_{LES}	Minimum LE pulse spacing, see Figure 25		630		ns
t_{CKN}	Serial clock hold time from LE, see Figure 25		0		ns
t_{PH}	Hold time, see Figure 27		10		ns
t_{PS}	Setup time, see Figure 27		2		ns
t_{CO}	Clock to output (SEROUT) time, see Figure 26	15	20	25	ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Inputs	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power[1] (f = 100 MHz to 30 GHz, T_{DIE} = 85°C[2])	
ATTIN	
Steady State Average	27 dBm
Steady State Peak	32 dBm
Hot Switching Average	24 dBm
Hot Switching Peak	28 dBm
ATTOUT	
Steady State Average	18 dBm
Steady State Peak	22 dBm
Hot Switching Average	15 dBm
Hot Switching Peak	19 dBm
RF Power Under Unbiased Condition (V_{DD} and V_{SS} = 0 V)	
Input at ATTIN	21 dBm
Input at ATTOUT	15 dBm
Temperature	
Junction (T_J)	135°C
Storage	−55°C to +150°C
Processing	170°C
Continuous Power Dissipation (P_{DISS})	0.4 W

[1] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[2] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specifications by 3 dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to carrier bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
C-18-1	125	°C/W

POWER DERATING CURVES

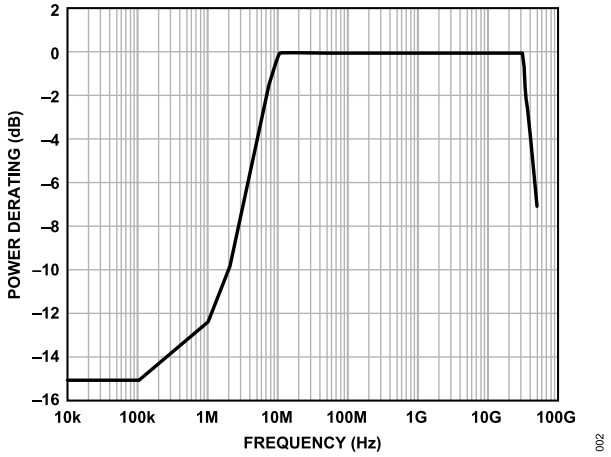

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{DIE} = 85°C

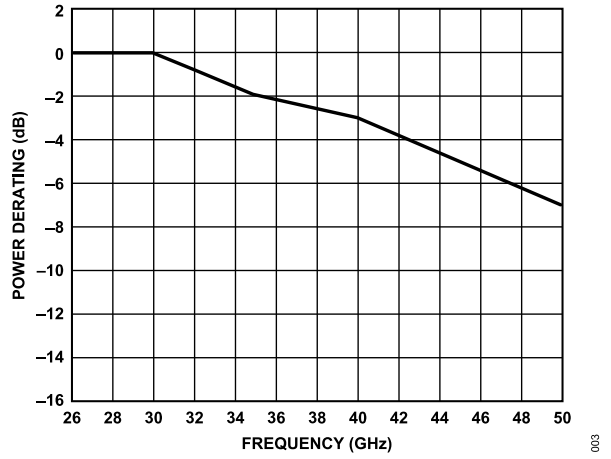

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{DIE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADRF5473

Table 5. ADRF5473, 18-Pad Die on Carrier [CHIP]

ESD Model	Withstand Threshold (V)
Human Body Model (HBM)	
ATTIN and ATTOUT Pads	±500
Supply and Control Pads	±2000

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

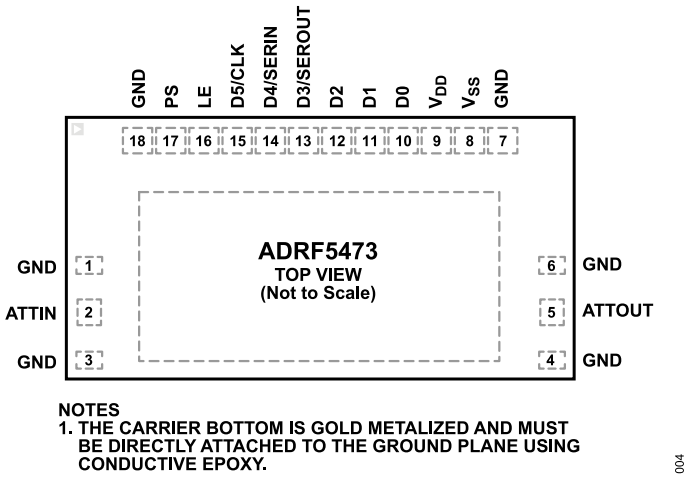

Figure 4. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 7, 18	GND	Ground. Bonding of these GND pads are optional. See the Applications Information section.
2	ATTIN	Attenuator Input. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 7 for the interface schematic.
5	ATTOUT	Attenuator Output. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 7 for the interface schematic.
8	V_{SS}	Negative Supply Input. See Figure 9 for the interface schematic.
9	V_{DD}	Positive Supply Input. See Figure 8 for the interface schematic.
10	D0	Parallel Control Input for 0.5 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
11	D1	Parallel Control Input for 1 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
12	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
13	D3/SEROUT	Parallel Control Input for 4 dB Attenuator Bit (D3). Serial Data Output (SEROUT). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
14	D4/SERIN	Parallel Control Input for 8 dB Attenuator Bit (D4). Serial Data Input (SERIN). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
15	D5/CLK	Parallel Control Input for 16 dB Attenuator Bit (D5). Serial Clock Input (CLK). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
16	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
17	PS	Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
	Carrier Bottom	The carrier bottom is gold metalized and must be directly attached to the ground plane using conductive epoxy.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

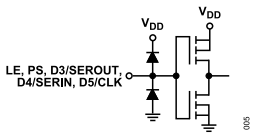

Figure 5. Digital Input Interface Schematic (LE, PS, D3/SEROUT, D4/SERIN, and D5/CLK)

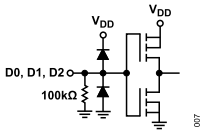

Figure 6. Digital Input Interface Schematic (D0, D1, and D2)

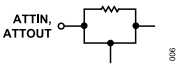

Figure 7. ATTIN and ATTOUT Interface Schematic

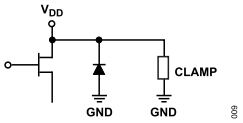

Figure 8. V_{DD} Interface Schematic

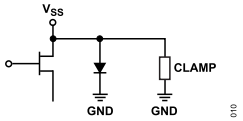

Figure 9. V_{SS} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

V_{DD} = +3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 3 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are deembedded. See Applications Information section for assembly details.

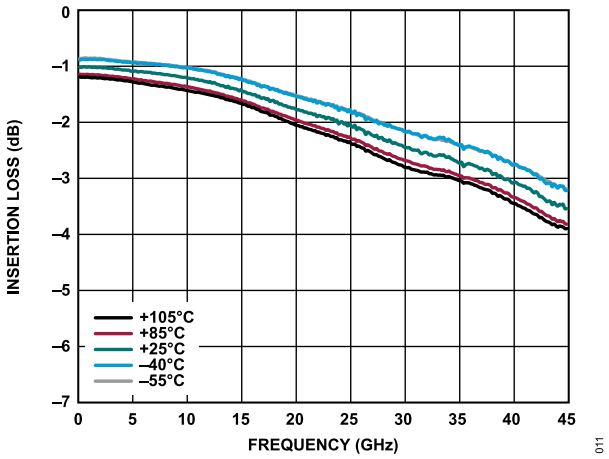

Figure 10. Insertion Loss vs. Frequency over Temperature

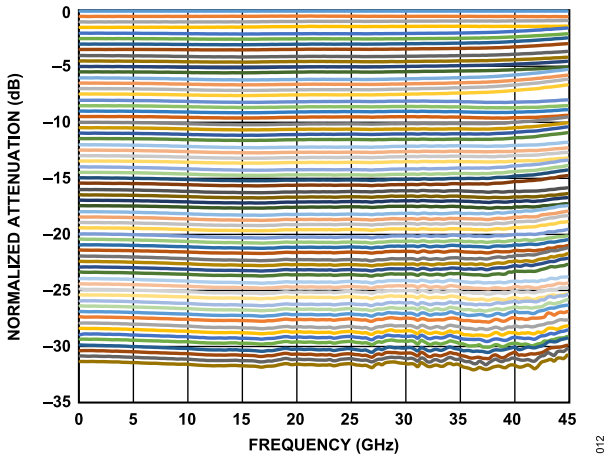

Figure 12. Normalized Attenuation vs. Frequency for All States

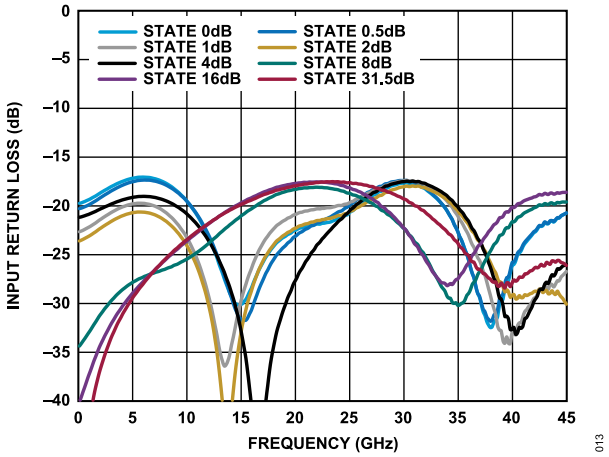

Figure 11. Input Return Loss vs. Frequency

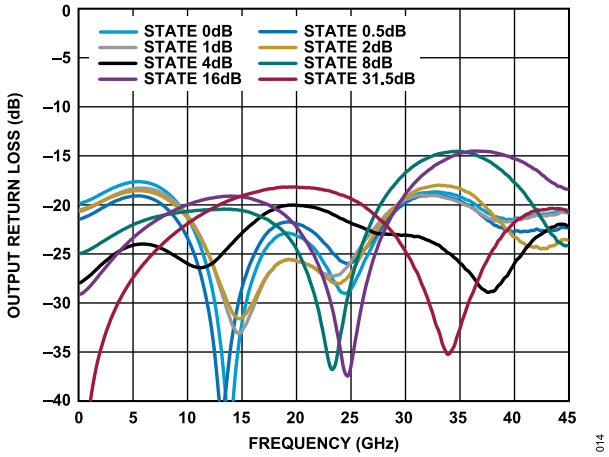

Figure 13. Output Return Loss vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

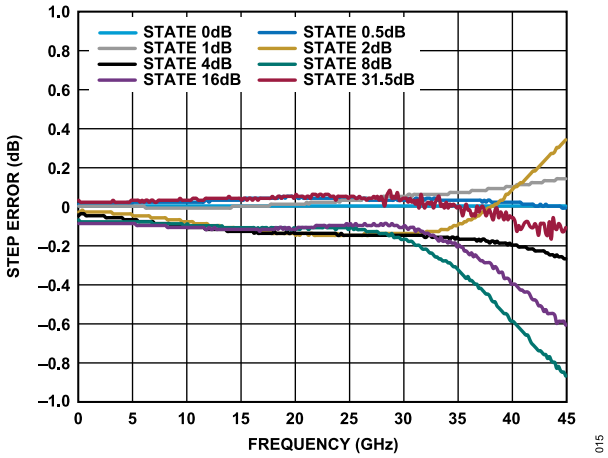

Figure 14. Step Error vs. Frequency

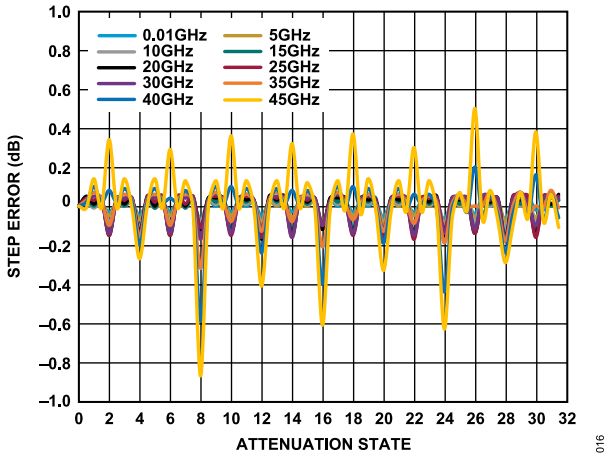

Figure 17. Step Error vs. Attenuation State over Frequency

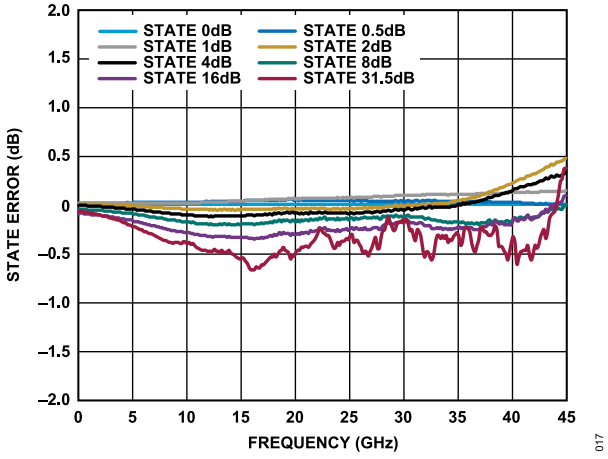

Figure 15. State Error vs. Frequency

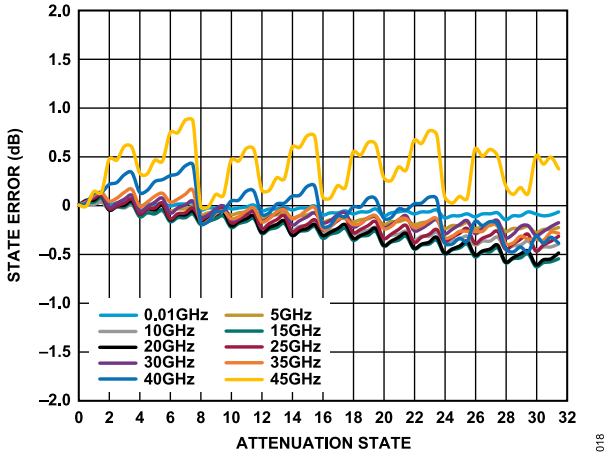

Figure 18. State Error vs. Attenuation State over Frequency

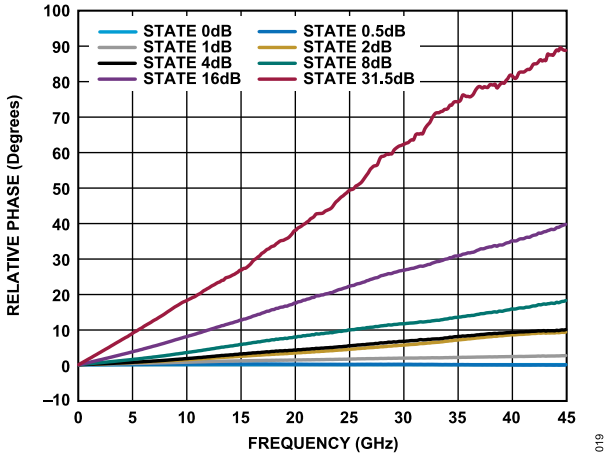

Figure 16. Relative Phase vs. Frequency

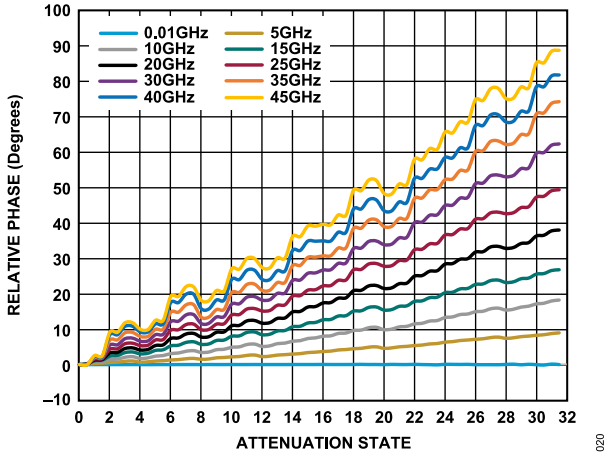

Figure 19. Relative Phase vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = +3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

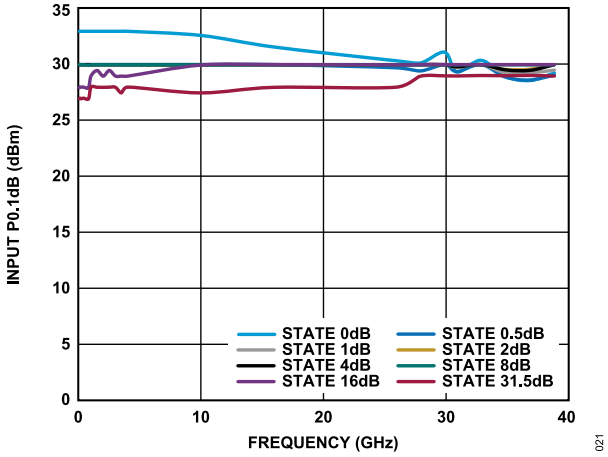

Figure 20. Input P0.1dB vs. Frequency

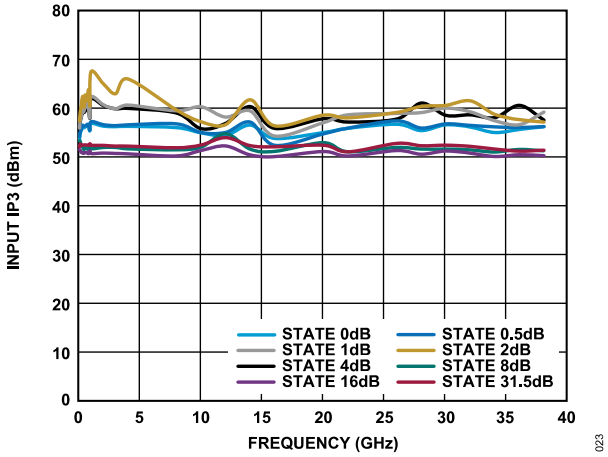

Figure 21. Input IP3 vs. Frequency

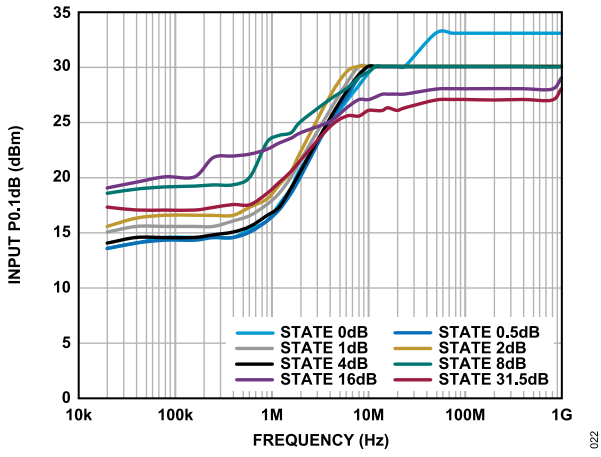

Figure 22. Input P0.1dB vs. Frequency, Low Frequency Detail

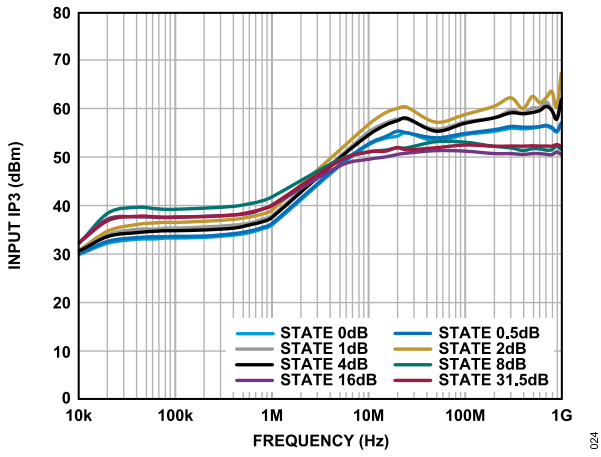

Figure 23. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5473 incorporates a 6-bit fixed attenuator array that offers an attenuation range of 31.5 dB in 0.5 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 24).

Note that when referring to a single function of a multifunction pad in this data sheet, only the portion of the pad name that is relevant is mentioned. For full pad names of the multifunction pads, refer to the Pin Configuration and Function Descriptions section.

POWER SUPPLY

The ADRF5473 requires a positive supply voltage applied to the V_{DD} pad and a negative supply voltage applied to the V_{SS} pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the V_{DD} voltage is powered up and the control pads are not driven to a valid logic state.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5473 has internal power-on-reset circuitry. This circuitry sets the attenuator to the maximum attenuation state (31.5 dB) when V_{DD} and V_{SS} voltages are applied, and LE is set to low.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. No dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The ADRF5473 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

Table 7. Truth Table

Digital Control Input[1]						
D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	High	0.5
Low	Low	Low	Low	High	Low	1.0
Low	Low	Low	High	Low	Low	2.0
Low	Low	High	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	31.5

[1] Any combination of the control voltage input states shown in this table provides an attenuation equal to the sum of the bits selected.

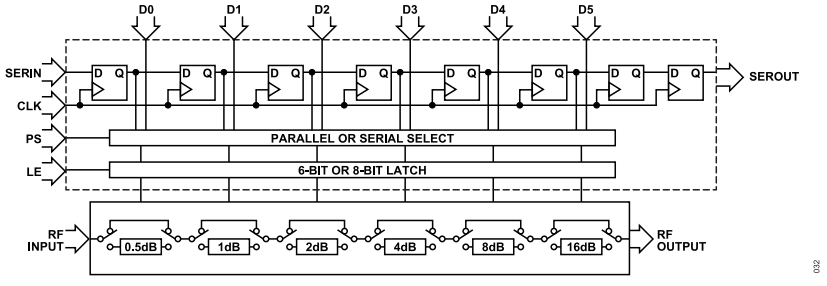

Figure 24. Simplified Circuit Diagram

THEORY OF OPERATION

SERIAL OR PARALLEL MODE SELECTION

The ADRF5473 can be controlled in either serial or parallel mode by setting the PS pad to high or low, respectively (see Table 8).

Table 8. Mode Selection

PS	Control Mode
Low	Parallel
High	Serial

SERIAL MODE INTERFACE

The ADRF5473 supports a 4-wire SPI: serial data input (SERIN), clock (CLK), serial data output (SEROUT), and latch enable (LE). The serial control interface is activated when PS is set to high.

The ADRF5473 attenuation states can be controlled using 6-bit or 8-bit SERIN data. If an 8-bit word is used to control the state of the attenuator, the first two bits, D7 and D6, are don't care bits. It does not matter if these two bits are held low or high, or if they are omitted altogether. Only Bits[D0:D5] set the state of the attenuator.

In serial mode, the SERIN data is clocked MSB first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new SERIN data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 25, Table 2, and Table 7 for additional information.

Using SEROUT

The ADRF5473 also features a serial data output (SEROUT). SEROUT outputs the serial input data at the 8th clock cycle and can control a cascaded attenuator using a single SPI bus. Figure 26 shows the serial out timing diagram.

When using the attenuator in a daisy-chain operation, 8-bit SERIN data must be used due to the eight clock cycle delay between SERIN and SEROUT. The SEROUT pad does not support high impedance mode. A tristate buffer can be used to interface a shared bus.

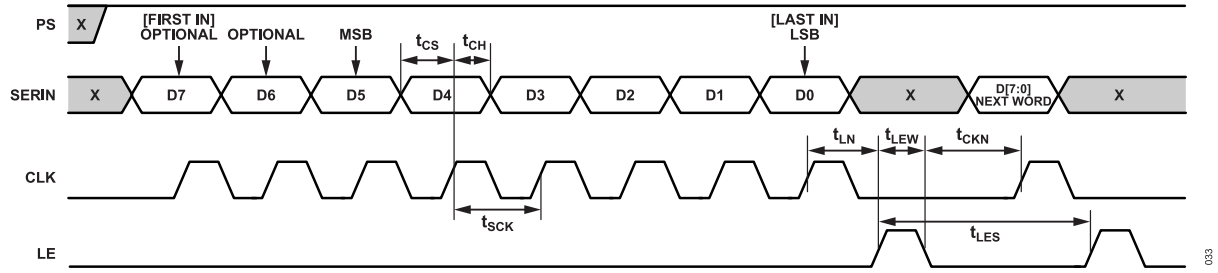

Figure 25. Serial Control Timing Diagram

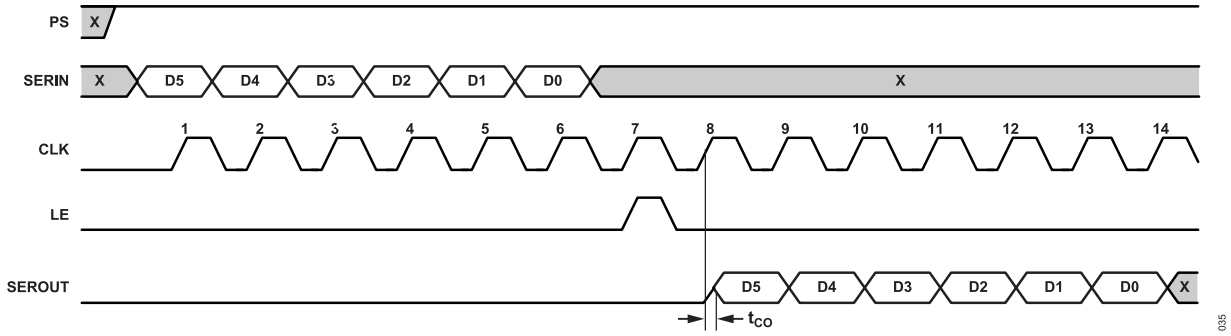

Figure 26. Serial Output Timing Diagram

THEORY OF OPERATION

PARALLEL MODE INTERFACE

The ADRF5473 has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 7. The parallel control interface is activated when PS is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, the LE pad must be kept high. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, keep the LE pad low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 27 and Table 2 for additional information).

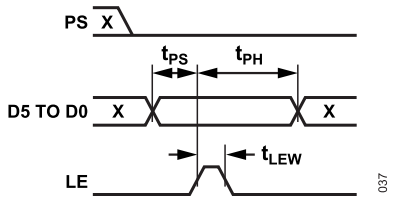

Figure 27. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

DIE ASSEMBLY

An assembly diagram of the ADRF5473 is shown in Figure 28.

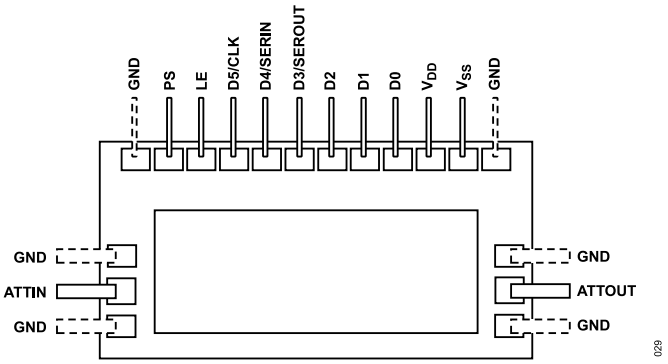

Figure 28. Die Assembly Diagram

The ADRF5473 is designed to have the optimum RF input and output impedance match with 3 mil × 0.5 mil gold ribbon wire and 3 mil loop height typical. The bonding diagrams are shown in Figure 29 and Figure 30. Alternatively, using multiple wire bonds with equivalent inductance yields similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad because the device is designed to match internally to the recommended ribbon bond. A spacing of 3 mils from the RF transmission line to the device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The dc pads are large enough to accommodate ribbon bonds, if preferred.

All bonds must be thermosonically bonded at a nominal stage temperature of 150°C, and a minimum amount of ultrasonic energy must be applied to achieve reliable bonds.

The device is metalized on the backside, and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

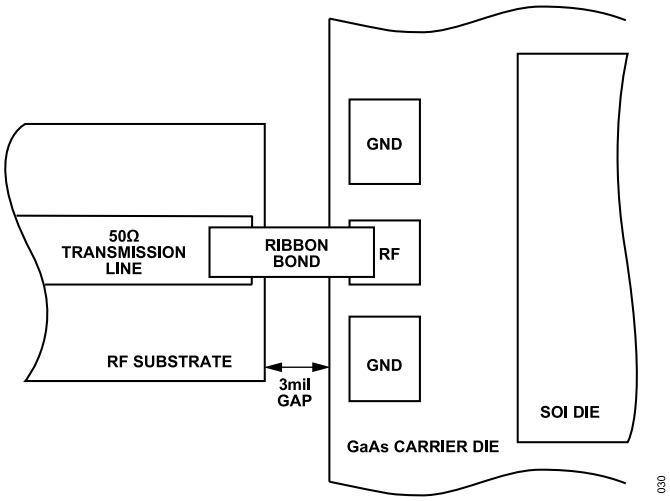

Figure 29. Bonding Diagram Top View

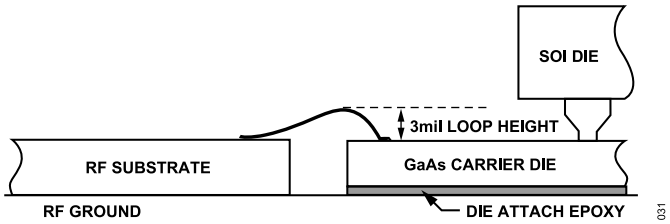

Figure 30. Bonding Diagram Side View

HANDLING, MOUNTING, AND EPOXY DIE ATTACH

Keep devices in ESD protective sealed bags for shipment, and store all bare die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs devices. However, for die on carrier devices, the use of a vacuum tool is recommended to avoid any damage on the device substrate. Handle these devices in a clean environment.

To attach the die with epoxy, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Set epoxy cure temperatures per the recommendations of the manufacturer and the maximum ratings of the device to minimize accumulated mechanical stress after assembly.

Because both dies are attached with solder joints, users must follow best practices for the thermomechanical design of their module assemblies. The temperature expansion coefficient of the substrate material must match the thermal expansion coefficient of the GaAs and silicon (Si) die. Do not allow warpage or other mechanical deformation on the substrate. Set the die attach process and the epoxy cure temperatures to lower the accumulated stress after assembly.

OUTLINE DIMENSIONS

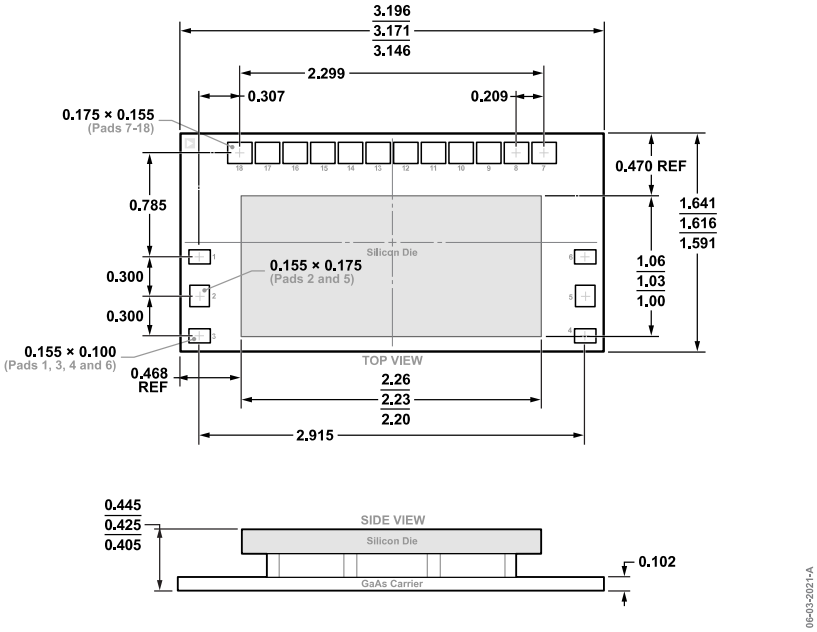

Figure 31. 18-Pad Die on Carrier [CHIP],
(C-18-1),
Dimensions Shown in Millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Information	Package Option
ADRF5473BCZ	–40°C to +105°C	18-Pad Die on Carrier [CHIP]	Waffle Pack, 50	C-18-1
ADRF5473BCZ-GP	–40°C to +105°C	18-Pad Die on Carrier [CHIP]	Gel Pack, 50	C-18-1
ADRF5473BCZ-SX	–40°C to +105°C	18-Pad Die on Carrier [CHIP]	Waffle Pack, 2	C-18-1

[1] Z = RoHS Compliant Part.